EXTRINSIC SILICON MONOLITHIC FOCAL PLANE ARRAY TECHNOLOGY AND APPLICATIONS*

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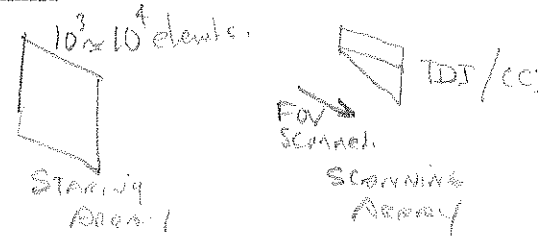

ABSTRACT. The purpose of developing extrinsic silicon monolithic infrared focal plane arrays is to improve the performance and reduce the cost of electro-optical sensors. The technology for making 1024-element mosaic arrays is discussed.

Data on quantum efficiency and detectivity (D^*) as a function of wavelength and temperature is presented for gallium- and indium-doped silicon. The effect of compensation on detector responsivity is reviewed. The results of measuring the crosstalk of 1 x 2 mil^2 and 4 x 4 mil^2 monolithic detectors are also presented. Low-temperature ($<20^oK$) CCD operation has been demonstrated, and a relative transfer loss of less than 4×10^{-5} has been observed. Various chip designs are shown and discussed.

INTRODUCTION

Most current high-performance infrared electro-optical sensors consist of infrared telescopes, mechanical azimuth (and elevation) scanners, and linear (or small, two-dimensional) infrared-sensitive arrays with their associated detector preamplifiers and video multiplexers. The performance of well designed infrared sensors is close to that theoretically predicted[1]. Performance is usually expressed as noise equivalent temperature difference (NETD), minimum resolvable temperature difference (MRTD), or noise equivalent target (NET) for point sources.

By using the standard performance equations one can trade off signal-to-noise ratio (SNR) and resolution against the diameter of the optics, the field of view (FOV), scan rates, number of detector elements, etc. Such tradeoffs are usually made in order to optimize a sensor for a specific application. The principal limitations on sensor performance are the diffraction limit of the optics in the infrared spectral region and the number N of infrared-sensitive detector elements, which for state-of-the-art sensors is less than 1000.

In order to improve infrared sensor performance without increasing the diameter of the optics beyond a typical value, the number of detector elements in the FOV must be increased. For a given FOV and angle subtended by one detector element, the value of SNR increases with the number of such elements as $\sqrt{N}$. For a given value of SNR and angle subtended by one detector element, the sensor FOV increases linearly with the number of such elements within the limits imposed by the properties of geometrical optics.

The purpose of developing extrinsic silicon monolithic focal plane arrays[2] (MFPAs) or infrared charge coupled devices (IRCCDs) is to improve performance beyond that of current electro-optical sensors without increasing the number of components and therefore the cost of such sensors. A realistic goal is to develop MFPAs

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containing 32 x 32 or 1024 detector elements per chip. Such arrays are illustrated in this paper. By stacking these chipsin the focal plane in the same way as detector elements are now stacked, it appears reasonable to assume that an order-of-magnitude improvement in performance can be achieved in the near future.

Several hybrid and monolithic IRCCD devices have been previously discussed[2,3,4-7]. These devices are classified as hybrid or monolithic infrared CCDs, respectively, depending on whether they consist of infrared detector materials, such as InSb, HgCdTe, PbSnTe, PbS, etc. combined with silicon CCDs, or whether these detector elements and the CCD readout registers are processed in the same material. The emphasis in this paper is on monolithic extrinsic silicon focal plane arrays which have the obvious advantage of being based on the highly developed "standard" silicon processing technology.

QUANTUM EFFICIENCY OF EXTRINSIC SILICON MFPAs

Extrinsic silicon MFPAs use the CCD substrate as the infrared-sensitive detector. Such a detector is operated in the photoconductive mode. Other structures, such as diffused junctions, photocapacitive devices, MOS junctions, and Schottky barrier junctions, have been considered[5] for use in IRCCDs.

The photoconductive detector is the only detector having an absorption thickness that is large enough to provide an acceptable detector quantum efficiency with the weak transitions[8,9] characteristic of extrinsic silicon. A typical absorption cross section σ for gallium-doped silicon at 10 μm, for example, is $\sigma = 4 \times 10^{-16}$ cm^2. An acceptable quantum efficiency ($\geq$50 percent) is obtained if $\sigma (N_A - N_D) \ell \geq 1$, where $N_A - N_D$ is the acceptor minus the donor concentration (3×10^{16} cm^{-3}) and d is the thickness of the sample in the direction of the incident radiation. On the basis of these values, one finds that the required thickness is $\ell \geq 0.8$ mm.

Figure 1 shows the theoretical and measured values of quantum efficiencies of Si:Ga arrays for doping concentrations in the range as a function of wavelength,

$$10^{16} < N_{Ga} < 10^{17} \text{ gallium ions/cm}^3$$

The calculation is based on the wavelength dependence[8] of σ and the classical expression for the external quantum efficiency, i.e.,

$$\eta = \frac{(1 - R)(1 - e^{-N\sigma\ell})}{(1 - Re^{-N\sigma\ell})}$$

where

- R = single-surface reflection coefficient
- N = density of absorbing centers
- σ = absorption cross section
- ℓ = thickness of detector

This relation holds for a transverse detector and it approaches a maximum value of 1 - R ($\approx$0.5 for silicon) for large values of $N\sigma\ell$. In MFPA structures, such as those discussed here, the current flows parallel to the direction of the incident radiation. In this case the expression is slightly modified.

The main considerations in regard to the expected quantum efficiency of extrinsic silicon detectors are (1) the maximum solid solubility of the impurity in silicon and (2) the way in which impurity banding affects detector performance when the detector is doped near the solid solubility limit.

The photoconductive gain of extrinsic silicon is directly proportional to the product of mobility and lifetime $\mu\tau$ and to a frequency response factor $g(f, Q_B)$ which derives from the space charge relaxation near the injecting contacts. The 3-db cutoff frequency f_{3db} (Q_B) is a function of the average background photon flux density Q_B (photons/cm^2-sec) incident on the detector. The transient response of extrinsic silicon detectors also depends on the space charge relaxation near the contacts.

The photoconductive lifetime of extrinsic silicon is inversely proportional to the

In (Cross-section) $\tau \leq 4 \times 10^{17}$ cm^{-2} from 3 to 5 μm.
Si

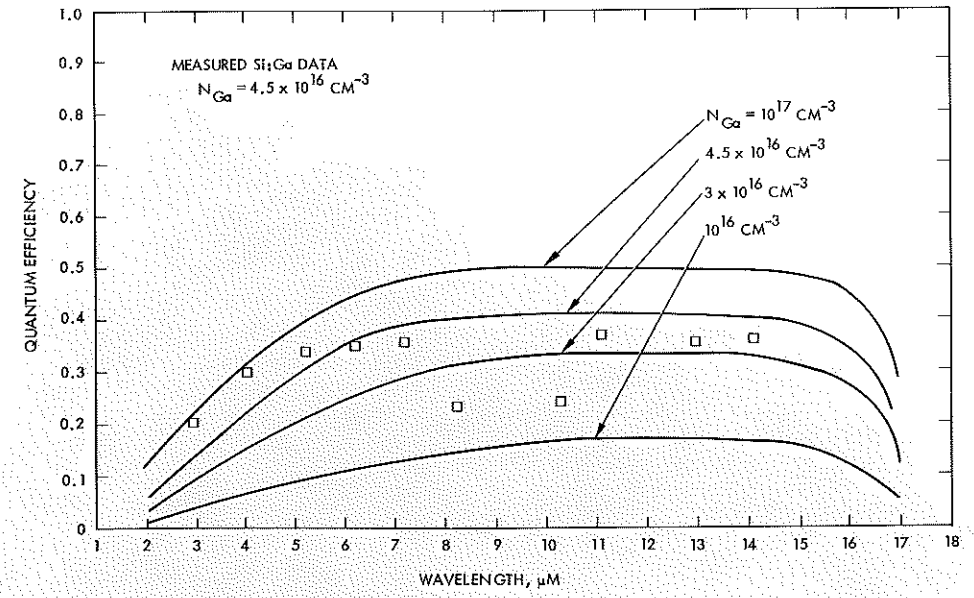

Figure 1. Theoretical and measured quantum efficiency of Si:Ga MFPAs

number of compensating impurities in this material. In gallium-doped silicon, these impurities are phosphorous having a concentration of about 2×10^{13} cm^{-3}. Such impurities (donors) are introduced into the crystal in order to compensate for the residual boron (acceptor) impurities that are always present in the polycrystalline silicon starting material with a concentration of about 10^{13} cm^{-3}. In typical extrinsic silicon materials, the lifetimes range from 10 to 100 nsec, depending on the details of the particular crystal parameters.

The hole mobility of gallium-doped silicon from $5^{\circ}K < T < 25^{\circ}K$ is approximately 1×10^4 cm^2/volt-sec for $N_{Ga} = 3 \times 10^{16}$ cm^{-3}.

Selected values of the product $\mu\tau$ or photoconductive gains have been presented for extrinsic silicon detectors for different values of background photon flux density and temperature for both gallium- and indium-doped crystals[10]. Hall effect data on the crystals shows that the carrier concentration is a function of 1/T and that the activation energy for the various levels (gallium, boron, etc.) appears as the slopes of the curves expressing this function.[9].

The relaxation time due to space charge effects can be approximated by

$$\tau_s = 2G\tau_\rho$$

where

$G = \mu\tau E/d$ = photoconductive gain

E = bias field, volts/cm

d = detector thickness, cm

$\tau_\rho = \epsilon\epsilon_o d(q\mu\tau Q_B)^{-1}$ = dielectric relaxation time, sec.

ϵ = relative dielectric constant (12 for silicon)

ϵ_o = dielectric constant of free space

q = electronic charge, coulombs

Q_B = background photon flux at focal plane, photons/cm^2-sec

Note that the term $\mu\tau/d$ is cancelled out in the expression for τ_s; hence $\tau_s = \tau_s(E, Q_B) = 2\epsilon\epsilon_o E/(qQ_B)$

The relaxation time of holes due to bulk effects can be approximated by the classical expression

$$\tau = (BN_p)^{-1}$$

where

B = recombination coefficient, cm^3/sec

N_p = number of negatively ionized trapping centers per cm^3. (compensating phosphorous centers N_p in p-type gallium-doped silicon)

This approximation is generally valid for $N_p > 10^{11}$ phosphorous centers per cm^3 and for typical background photon flux levels Q_B that are less than 10^{16} photons/cm^2-sec.

Typical values of τ are $10 < \tau < 100$ nsec and $\tau_s = 1.35 \times 10^7 E/Q_B$. For a typical bias field E of 200 v/cm and for a background photon flux Q_B of 10^{14} photons/cm^2-sec, τ_s = 27 μsec. Except for very high values of Q_B, the dominant time constant is the space charge relaxation time constant.

The static responsivity $R_\lambda = 0.804 \lambda \eta G$ amperes/watt (where λ is measured in μm and η is the quantum efficiency) can be measured directly and compared with the calculated value of responsivity based on known parameters of the material.

Several lots of the 2096 MFPAs (see below) have been processed on both Czochralski-grown (CZ) and float-zone grown (FZ) materials. This has provided an opportunity for measuring the expected increase in responsivity because of the greater purity of the FZ silicon. Table 1 shows values of MFPA responsivity for four device lots at $\lambda = 4$ μm.

In this table, calculated and measured values of responsivity for the FZ material are in good agreement for an assumed recombination coefficient B of 6.4×10^{-6} cm^3/sec and a quantum efficiency η of 0.25.

EXTRINSIC SILICON MFPA

Figure 2 shows a portion of an extrinsic silicon MFPA array on the Hughes CCD 2063 test chip. This chip has several linear arrays with integral CCD readout. The performance of this test chip has been previously reported.(11) Crosstalk characteristics have recently been investigated and are described here.

Figure 3 shows the measured and calculated spot scan of a detector in the 32-element MFPA on CCD 2063. The calculated response is the convolution of the effective detector width and the blur spot size. The effective detector width is larger than the detector contact size because of the distribution of the biasing electric field lines between adjacent detector elements in the structure. The structure between the

Table 1. MFPA responsivity

Lot No.	Material	Compensation (total donors), cm^{-3}	Responsivity, amperes/watt	
			Predicted (E=200 v/cm)	Measured
2063-20	CZ	10^{14}	0.26	0.185
2096-2	CZ	10^{14}	0.26	0.04 to 0.11
2096-10	FZ	9.9×10^{12}	2.5	2.48

$\tau = \frac{1}{BN_p} = \frac{1}{9.9\times10^{12}\times6.4\times10^{-6}} \simeq 20$ nsec

$G = \frac{\mu\tau E}{d} = \frac{10^4\times20\times10^{-9}\times200}{20\times10^{-3}\times2.54} \simeq 0.8$ (photoconductive gain)

Crosstalk $\left(\frac{\text{adj.}}{\text{4 adj.}}\right) \simeq 4(11.5\%) + 11.5\% \simeq 58\%$

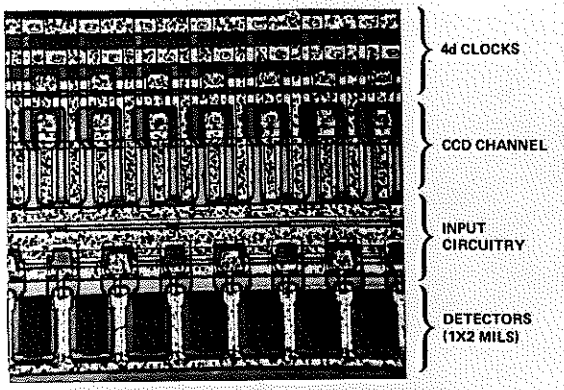

Figure 2. Extrinsic silicon MFPA test chip

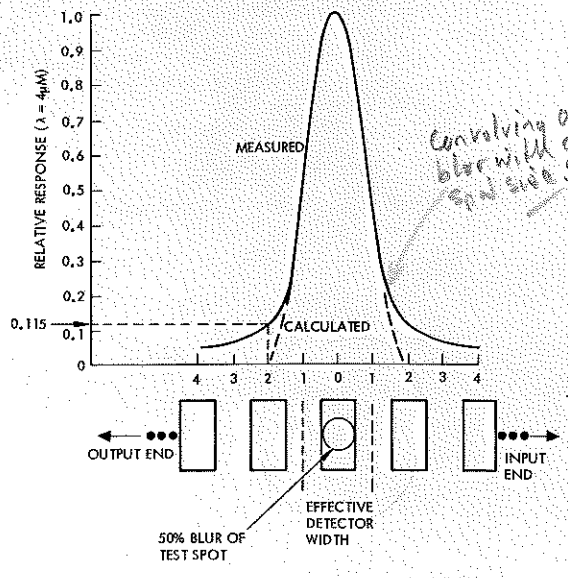

Figure 3. Spot scan of 1 x 2 mil detector on CCD 2063

contacts is transparent to infrared radiation. The measured spot scan shows 11.5-percent crosstalk at the center of the adjacent detector element when an f/1.5 optical system is used to generate the test spot. The MFPA was 0.020-inch thick with a Si:Ga substrate. As shown in Figure 4, the response is linear with detector bias.

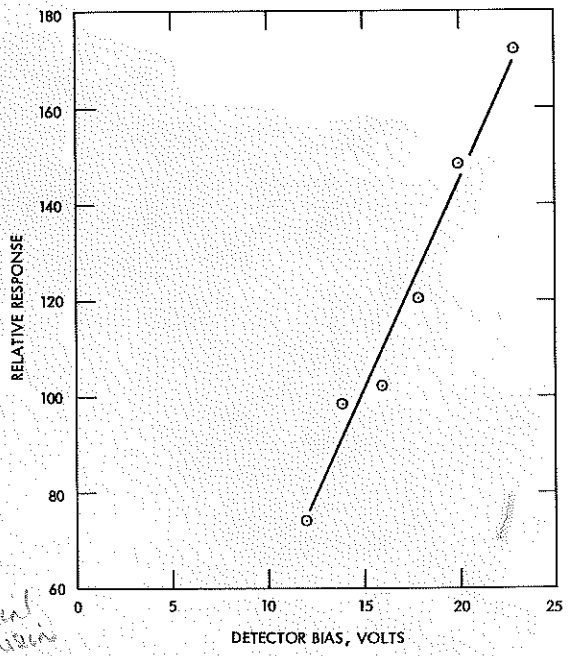

Figure 4. 2063 MFPA output as a function of chip bias

Crosstalk in the MFPA structure is due to bulk optical effects, including reflection from the back surface (see Figure 5). The electrical crosstalk is negligible because the lateral diffusion of the carriers is on the order of 1 μm. In addition, shunting surface conductance paths between adjacent detector contacts due to dopant impurity pile-up at the processed surface do not occur in this structure.

As shown in Figure 5, the incoming optical cone converges in the silicon substrate because of the change in the index of refraction. Crosstalk is therefore a function of f/number, quantum efficiency η, and backside reflectivity ρ. The measured crosstalk indicated in Figure 3 is shown as a point on the calculated curves in Figure 6. In the calculated curves, the detector geometry shown in Figure 3 was assumed. The second curve in Figure 6 shows the projected crosstalk with greater quantum efficiency (dopant concentration) and the elimination of backside reflectivity. If this reflectivity is small, crosstalk can be further reduced

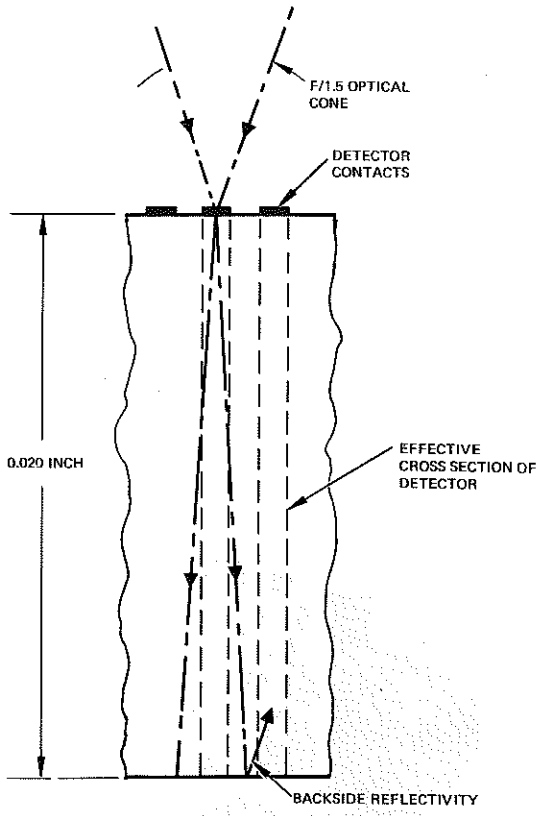

Figure 5. Cross section of extrinsic silicon MFPA

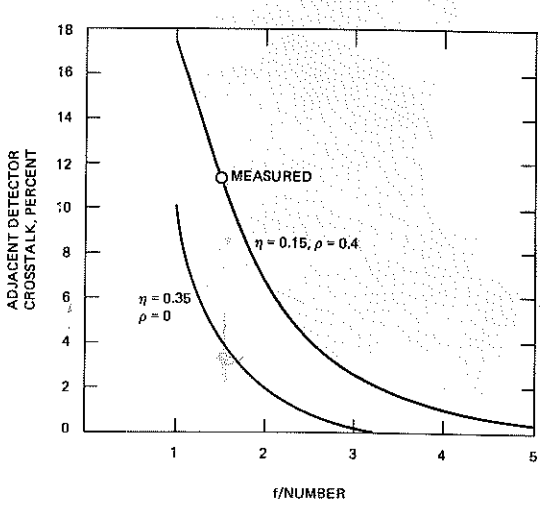

Figure 6. Si:X MFPA crosstalk as a function of optical f/number

by reducing the MFPA thickness. At higher f/numbers, crosstalk approaches zero because the rays entering the silicon are refracted to an angle that is almost perpendicular to the front surface of the MFPA.

The temperature at which an extrinsic silicon MFPA (or any extrinsic detector) must operate in order to achieve BLIP performance depends on the focal plane photon background and on the energy level (spectral cutoff) of the dopant used. Figures 7 and 8, which show $D^*_{\lambda pk}$ as a function of temperature, define the operating temperatures required for two popular extrinsic detector materials (Si:In and Si:Ga), respectively. In Figure 7, the theoretical BLIP operating temperatures for Si:In range from 5° to 10° lower. In a similar fashion, in Figure 8, the predicted operating temperatures for Si:Ga range from 21° to 32°K. For present materials the operating temperatures must be 3° to 5° lower.

PERFORMANCE OF CCDs AT LOW TEMPERATURES

In the extrinsic silicon MFPA configuration, CCDs must operate at the same low temperature that the detectors need for

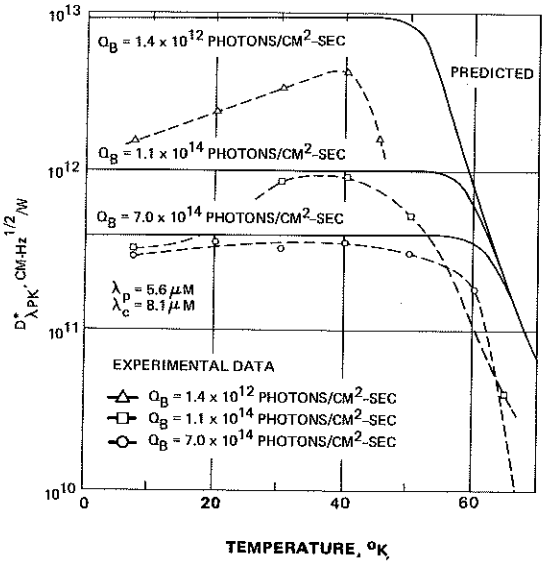

Figure 7. $D^*_{\lambda pk}$ of Si:In as a function of temperature

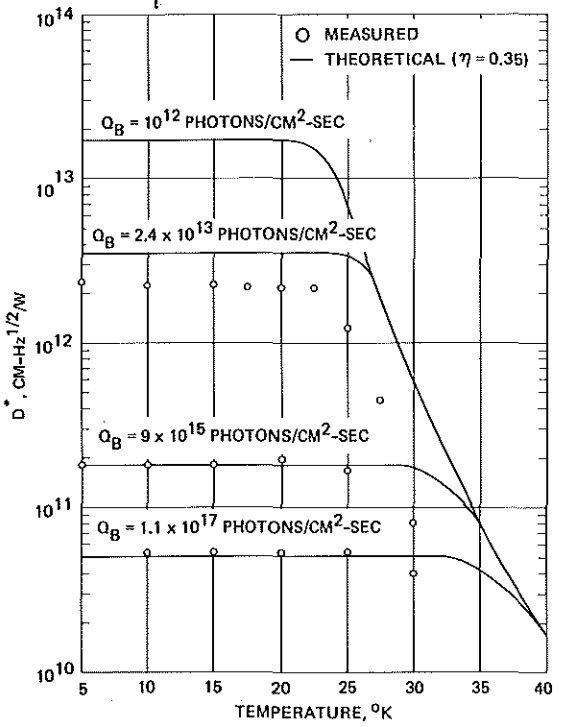

Figure 8, $D^*\lambda_{pk}$ of Si:Ga as a function of temperature

BLIP operation. These operating temperatures can be lower than the temperature at which the onset of thermal carrier freeze-out begins for the CCD. Current understanding of the low-temperature operation of MOS devices suggests that greater noise and poor transfer efficiency may result in this case. Since it is important to the success of an extrinsic silicon MFPA, it is appropriate to review some low-temperature CCD test results.

Figure 9 shows measured CCD transfer efficiency as a function of clock frequency at four different operating temperatures. The CCD tested was a 150-bit shift register (Hughes CCD 2070) processed as a p-surface channel device. Devices from several different lots were evaluated. Dewar test leads limited the test setup to clock frequencies of less than 200 kHz. This figure shows that transfer efficiency increases below room temperature and that at temperatures from 80° to 13°K, the transfer loss $\epsilon = 1 - \alpha$, has an average value of less than 4×10^{-5} (corresponding to a transfer efficiency α of 0.99996).

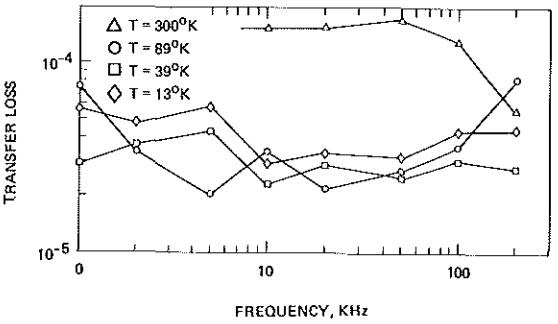

Figure 9. CCD transfer of a function of clock frequency

To help establish a criterion for acceptable values of transfer efficiency for MFPAs, the CCD output pulse height as a function of number of transfers was plotted (See Figure 10). The relative amplitudes of the first, second, and third output pulse are shown for an input pulse having an amplitude of unity. The value of transfer efficiency α is assumed to be 0.9999 ($\epsilon = 10^{-4}$).

For most applications, maintaining a pulse fidelity within 1 percent is adequate. Figure 10 shows that if all bits of the CCD convey a signal, the number of transfers

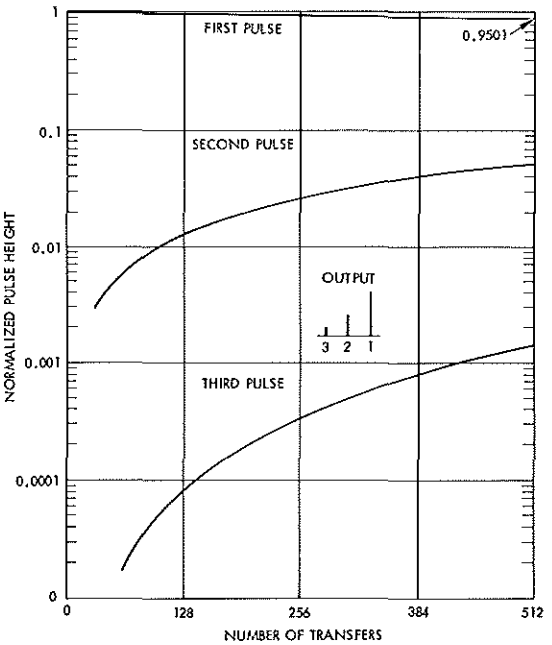

Figure 10. CCD pulse height as a function of number of transfers for $\alpha = 0.9999$

is limited (for 1-percent fidelity) to approximately 100 because of second-pulse spillover. In the more typical case in which the signal is conveyed in alternate bits, this figure shows that even after 512 transfers, fidelity as limited by third-pulse spillover is greater than 0.12 percent. It is therefore concluded that a CCD transfer efficiency of 0.9999, which is easily achievable at the detector operating temperatures, is adequate for most applications.

Figure 11 shows the noise spectral density measured with the same CCD as that used in the transfer efficiency tests (see Figure 9). Measurements were also made at the same four operating temperatures. In Figure 11, the average midband noise is approximately 2.5 noise carriers/$\sqrt{\text{Hz}}$, which is equivalent to a total integrated noise of 30 noise carriers/bit normalized to an 0.001-inch channel width. For a surface channel CCD, this level of noise is normally considered to be lower than average.

In summary, it appears that the low-temperature transfer efficiency and noise characteristics of surface channel CCDs display no anomalous behavior at low temperatures and that they in fact improve somewhat at low temperatures. Measurements show that transfer efficiency and noise level are acceptable for most applications.

Figure 12 shows a second-generation extrinsic silicon MFPA test chip; it contains a family of test devices, including three new basic concepts for CCD detector readout in monolithic format. Two test devices, the 4 x 4 array and the 32 x 2 array, are being evaluated as part of the development of a complete 32 x 32 staring array. These devices employ almost identical detector elements measuring 0.004 x 0.004 inch, as shown in Figure 13.

Spot scans of a detector element are shown in Figures 14 and 15. The calculated responses shown in these figures were obtained as in Figure 3 with an assumed detector aperture 4 mils square.

The geometry of the integrated detector contact is responsible for the departure from the calculated curves, but these scans do indicate that an effective detector area that is 80 percent of the detector element area can be achieved.

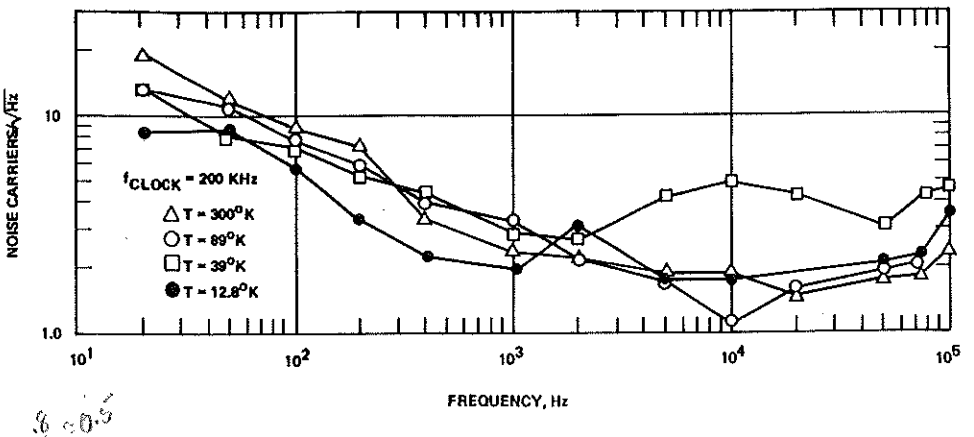

Figure 11. CCD noise as a function of frequency

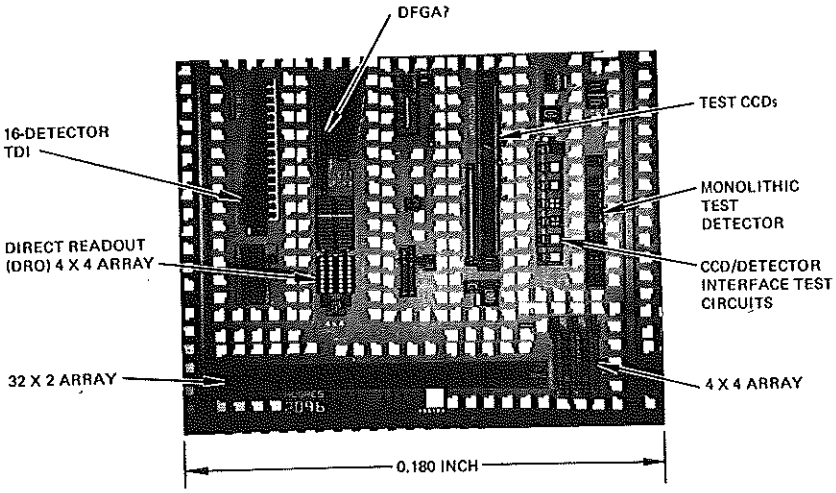

Figure 12. Extrinsic silicon test chip CCD 2096

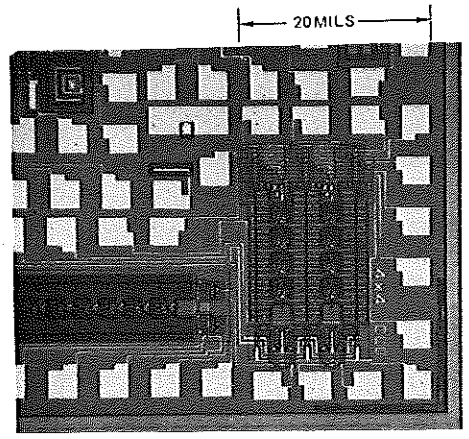

Figure 13. MFPA 4 x 4 array

Figure 16 shows the two output pulse trains from the 2 x 32 array. The integrated detector signals are transferred to the readout CCDs by pulsing the transfer electrode (the transfer pulse shown in this figure) and then read out serially. The uniformity of response is approxi - mately ±15 percent. At present, it is limited by the variation in the concentration of gallium in the detector volume.

This amount of variation is acceptable for certain staring sensors used for "change detection". More sophisticated differ - ential encoding techniques can be used when variations in array response must be com - pensated for, as in imaging applications.

32 x 32 MFPA

A layout of a 32 x 32 detector MFPA is illustrated in Figure 17. The overall chip dimensions are 184 x 187 mils. The total active area is 128 x 128 mils. Each detector element (4 x 4 mils) contains input circuitry, a storage bucket, an over - load protection device, a transfer gate, and four bits of CCD readout. Each row of the array consists of 32 detector ele - ments and 128 CCD bits. A 128-bit multi - plexing CCD (at the left in this figure) reads the charge out columnwise from the array.

POWER DISSIPATION ON FOCAL PLANE

In systems which will utilize a large number of MFPA chips, power dissipation on the focal plane becomes an important design factor. The sources of electrical power dissipation are briefly discussed below.

Electrical power dissipation on the focal plane chip originates from (1) the

Question: Optical crosstalk? By modification of chip design and geometry.

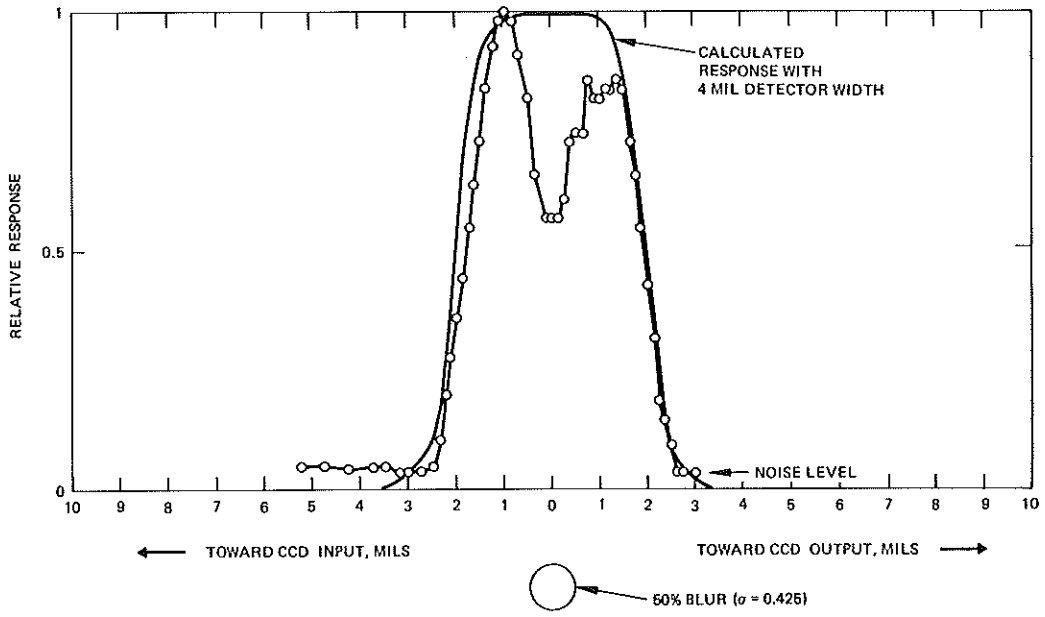

Figure 14. Parallel scan (along array) by a detector element of the Hughes 2096 2 x 32 MFPA

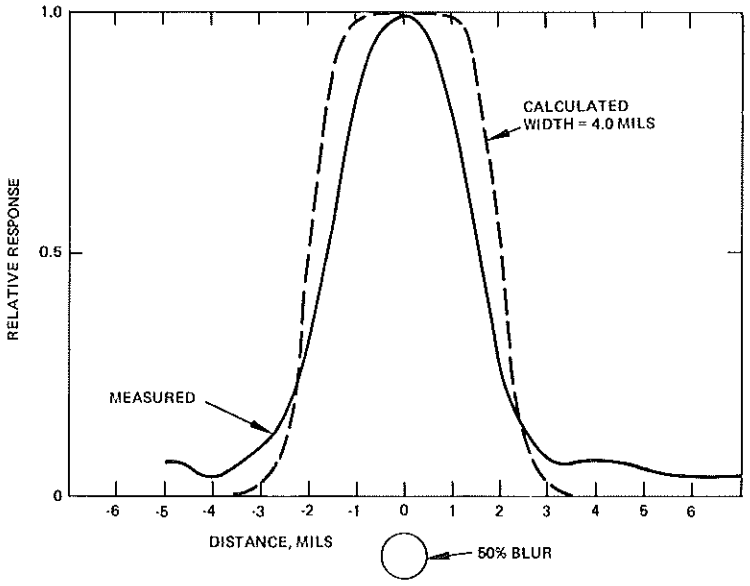

Figure 15. Perpendicular scan by a detector element of the Hughes 2096 2 x 32 MFPA

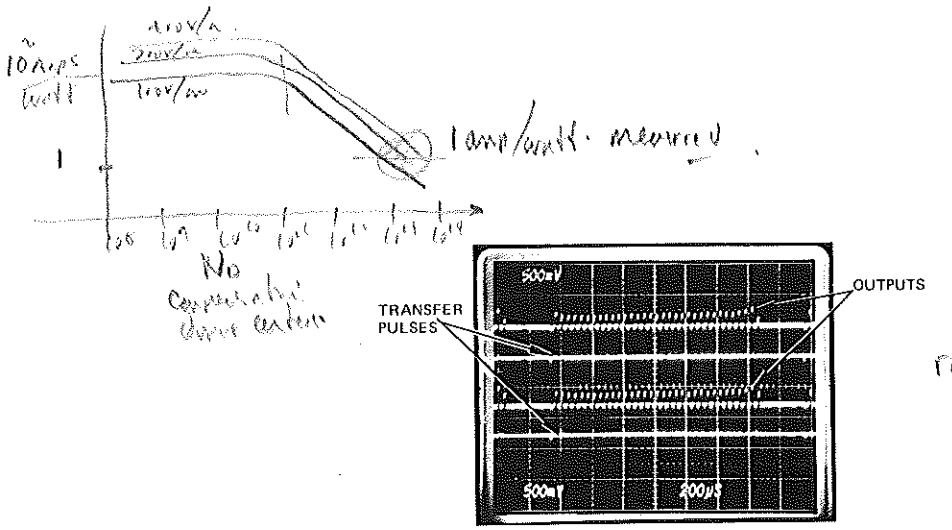

Figure 16. Outputs from 2 x 32 array

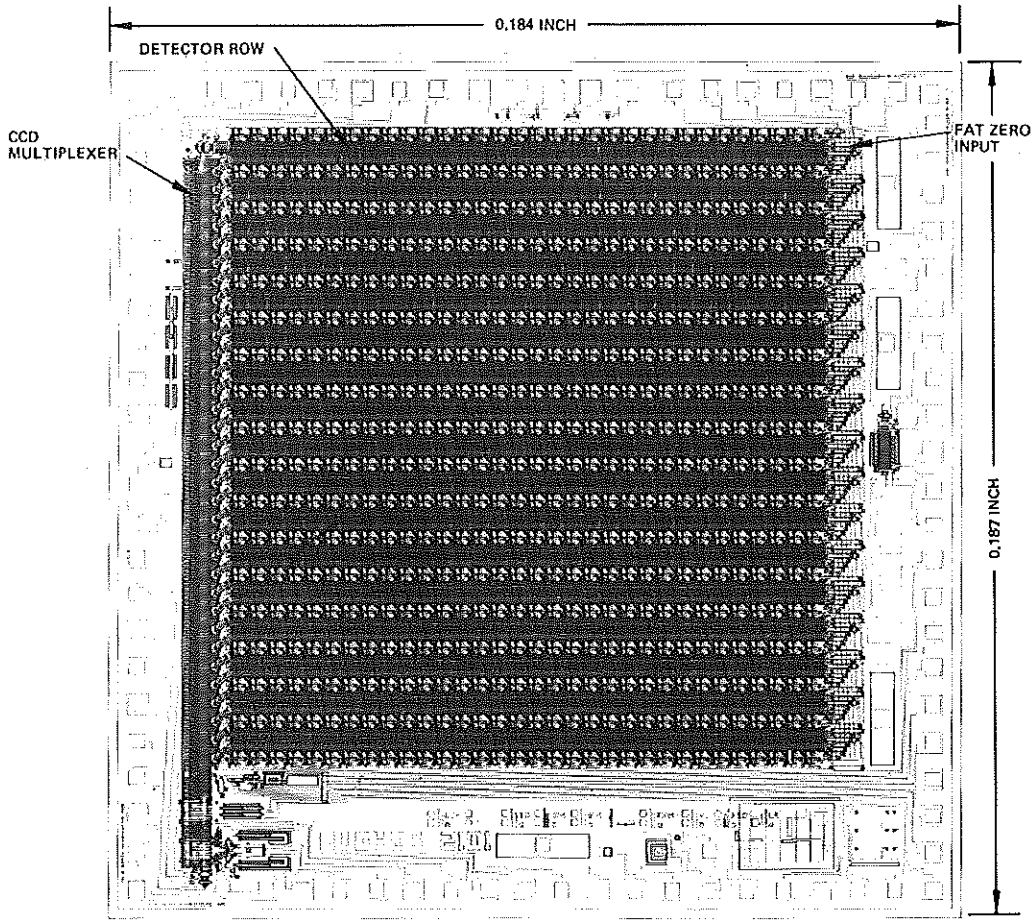

Figure 17. Layout of 32 x 32 MFPA (Hughes CCD 2101)

detectors, (2) the CCD readout registers, and (3) the output circuitry. The power dissipated by this circuitry is expected to dominate and depends primarily on the bandwidth. At clock rates of 200 kHz, bias currents of at least 0.1 ma and a drain voltage of about 6 volts, output MOS devices dissipate about 0.6 mw. This amount of power combined with that dissipated by the detectors brings the total power dissipated to less than 1 mw/chip.

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