BIPOLAR PERIPHERAL CIRCUITRY FOR CCD'S

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ABSTRACT

High performance bipolar transistors have been fabricated on the same chip as buried channel CCD's with one additional photoengraving and ion implantation. The bipolar transistors occupy less area and have greater drive capability than peripheral MOS transistors. f_T's of around 500 MHz have been achieved, thus extending the frequency range for peripheral circuitry above the 10 MHz limit imposed by MOST's.

Design studies for CCD peripheral circuitry using the bipolar process are presented. A comparison of on-chip MOS and Bipolar clock drivers is made for high frequency applications. Single stage bipolar amplifiers have been fabricated previously (ref. 1) but the process described here enables high gain bandwidth amplifiers to be considered for a wide range of on-chip signal processing applications. The technique described by MacLennan and Mavor (ref. 4) for obtaining a low harmonic-distortion transfer function could readily be integrated with the CCD using this process.

INTRODUCTION

Although buried channel CCD's are capable of operating at frequencies in excess of 100 MHz, the problems involved in feeding clocking waveforms onto the chip and taking signals off the chip are considerable. MOST amplifiers have limited drive capability at frequencies above a few MHz. A moderate performance bipolar transistor with an f_T in the range 200 MHz to 1 GHz would solve many of these problems of interfacing if it could be included on the CCD chip. In addition the bipolar device would give greater flexibility for on-chip signal processing, and allows on-chip CCD clock drivers to be considered for frequencies above 5 MHz.

A CCD compatible bipolar process is described whereby high performance npn transistors can be fabricated with the minimum of additional processing. The performance of these devices is presented and used as the basis of a design study for several possible applications where the high gain and wide bandwidth offered by the bipolar process should have significant advantages over MOS circuits. An evaluation of a test mask incorporating bipolar amplifiers is in progress and it is hoped that preliminary results will be available.

THE CCD COMPATIBLE BIPOLAR PROCESS

The fabrication of a bipolar transistor on the CCD chip requires only one additional photoengraving and ion implantation stage which form the collector region. The existing boron (channel stop) and phosphorus doped regions (input and output diodes, source and drain) can readily be modified to form the base and emitter of an npn transistor. Ion implantation is used throughout and results in good process control. The device structure is shown schematically in Figure 1 in cross-section. Figure 2

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shows the plan view of a minimum geometry npn transistor cell which has a ring collector diffusion to minimise the collector series resistance.

Typical parameters for a large geometry test transistor are given in Table 1. The collector series resistance R_{cs} and cut off frequency f_T should both be improved on the minimum geometry device. In particular a value of R_{cs} = 120 ohm per cell should be achieved and the effective series resistance can be reduced by connecting several cells in parallel.

TABLE 1

Parameter		Value
Emitter size		12 x 20 μm
h_{fe} npn	(100 μA	20
	(1 mA	28
	(10 mA	25
R_{cs}	ohms	400
f_T	MHz	360
BV_{CEO}	volts	12

DESIGN STUDY FOR ON-CHIP CLOCK DRIVERS

Both MOS and bipolar clock driver circuits have been considered for on-chip fabrication. MOS does not require additional processing but is limited to applications where the clock frequency is below 5 MHz. As described above, the on-chip bipolar process requires additional processing stages but it does give transistors capable of driving at around 25 MHz. No improvement in CCD performance is expected from the incorporation of clock drivers on-chip; in fact the power dissipated by the drivers at high frequencies will degrade the CCD performance. However, on-chip clock generation and driving does offer a more marketable product and there may even be package cost savings if the number of pins can be reduced.

A comparison of MOS and bipolar transistors for clock driving will now be made.

MOS DRIVER TRANSISTOR

Consider an MOS transistor with an aspect ratio A = 100 which will occupy an area = 1.6 x 10^4 μm^2. The on resistance of this device is given by

$$R_{ON} = \frac{1}{\beta_o A V_E}$$

where $V_E = V_G - V_S$ is the effective gate voltage and β_o is the figure of merit

Inserting typical values, say $\beta_o = 20\ \mu A/V^2$ and V_E = 7 volt, then

$$R_{ON} = \frac{1}{20 \times 10^{-6} \times 100 \times 7} = 70 \text{ ohms}$$

With a 100 pF load C_L corresponding to one CCD clock phase,

$$\tau = R_{ON} C_L = 7 \text{ nSec}$$

However, if this transistor is pulling the clock phase towards the high level V_R the effective gate voltage V_E will be decreasing and typically after 10τ the load will have reached 0.8 V_R. Hence a time period of close to 200 nS will be required to complete one 3 phase clock cycle, and the maximum clock frequency $f_{max} = 5$ MHz.

BIPOLAR DRIVER TRANSISTOR

Consider the bipolar transistor cell shown in Figure 2 which occupies an area of 40 x 58 μm^2. Seven of these cells can be grouped in the area occupied by the MOS transistor described previously. The collector series resistance of the bipolar device will be

$$R_{CS} = \frac{120}{7} \text{ ohm} = 17 \text{ ohm}$$

Hence for a 100 pF load

$$\tau = R_{CS} C_L = 1.7 \text{ nSec.}$$

The high frequency gain of the transistor will be adequate to ensure active pull up of the load towards the high level V_R. If the pull up rate is limited by the collector series resistance then in a time period of 3τ the load will have reached 0.95 V_R. If a similar transistor is used in totem pole configuration to pull the load to the low level then the three phase clock waveforms will be as shown in Figure 3 and the total clock period will be approximately 40 nSec. The maximum clock frequency will thus be $f_{max} = 25$ MHz. In the range of clock frequency between 5 MHz and 25 MHz it appears that bipolar on-chip clock drivers for CCD's are feasible. However, the effect of the power dissipated by clock drivers on the performance of the CCD must be considered.

POWER DISSIPATION

The power dissipated by an ideal driver stage is given by

$$P = CV_c^2 f$$

A more realistic figure for a practical driver stage will be closer to $2CV_c^2 f$ (ref. 2).

$$C = 3N C_{BIT} \text{ for a three phase device}$$

N is the number of bits and C_{BIT} is the capacitance per bit. The maximum number of bits is given by

$$N_{max} = \frac{\text{Storage time}}{10 \text{ x transfer period}} = \frac{\tau_s f_c}{10}$$

assuming that leakage currents are the limiting factor and that a 10% level of leakage current is tolerable. If the leakage current doubles

for every 10°C temperature rise ΔT then

$$\tau_S = \frac{\tau_{SA}}{(2)^{0.1\Delta T}}$$ where τ_{SA} is the storage time at ambient temperature

$$\Delta T = \theta P$$ where θ is the thermal resistance

Hence,

$$N_{max} = \frac{\tau_{SA} f_c}{10 \times (2)^{0.6\theta N_{max} C_{BIT} V_c^2 f_c}}$$

$$N_{max} \times (2)^{N(0.6\theta C_{BIT} V_c^2 f_c)} = \tau_{SA} f_c / 10$$

This expression can be used to calculate the maximum number of bits for a given clock rate or, alternatively, the maximum clock rate for a given number of bits.

Taking typical values V_C = 10 volt, C_{BIT} = 1 pF, θ = 80°C per watt, and τ_{SA} = 1 second at 30°C Table 2 shows the calculated values of power dissipation, temperature rise and N_{max} for two values of ambient temperature, and two values of clock frequency.

TABLE 2

Clock Frequency	5 MHz		25 MHz	
Ambient Temperature	30°C	70°C	30°C	70°C
N_{max}	420	280	120	90
Power Dissipation	1.28W	0.84W	1.8W	1.35W
Temperature Rise	102°C	66°C	144°C	108°C

For a 1k bit device at 30°C we find that the maximum clock frequency f_c = 3.1 MHz. From Table 2 we can see that the maximum number of bits is severely limited by the power dissipated by on-chip clock drivers.

APPLICATION OF HIGH GAIN/WIDE BANDWIDTH AMPLIFIERS TO CCD TRANSVERSAL FILTERS

CCD transversal filters are capable of high performance in a variety of filter applications, but complex peripheral circuits are needed and it is a great advantage if these can be integrated with the CCD (ref. 3). In many applications, but by no means all, high gain/bandwidth products ($>10^6$) are required. For gain/bandwidth products below this value MOS peripheral circuits are satisfactory. The precise requirements for the on-chip amplifiers depend on whether floating gate voltage sensing or charge sensitive amplifiers are used to detect the CCD tapped output.

(a) FLOATING GATE TECHNIQUE

Figure 4 shows the output configuration used in the floating gate method of sensing the output from the split electrode taps. The clock phase electrodes ($C\phi\pm$) and integrating capacitor can be preset to a DC level and then allowed to float during the arrival of the signal charge. The other terminals (point z on Figure 4) of the integrating capacitors $C_i\pm$ can be connected to ground or, alternatively, driven by the appropriate CCD clock phase. Although the latter technique increases the signal handling capacity by a factor of two, it requires a high common mode rejection by the following differential amplifier. The common mode signal may be of the order of 10 volt while the difference signal is around 100 mV.

The difference voltage V_d is inversely proportional to $C_i + C\phi$ Although a smaller integrating capacitor C_i increases the gain, this is at the cost of poorer linearity as $C\phi$ is a depletion capacitance which changes with the size of CCD signal charge. This non-linearity is much worse for buried channel CCD's and in practice means that the floating gate technique is normally only used with surface channel devices. However, the introduction of feedback linearisation on chip (ref. 4) would reduce this problem considerably.

The resetting of $C\phi$ and C_i introduces an equivalent noise voltage of $\sqrt{\frac{kT}{C\phi + C_i}}$ at the input of the differential amplifier. For 300 pF this contribution to the noise is 3.5 μV which is quite significant as the total noise level for the CCD filter at this point has been estimated as 10 μV (ref. 2). The wideband noise introduced by the differential amplifier should be less than this figure if the dynamic range of the CCD is not to be degraded. However, this is a difficult target to reach and the practical amplifier reported in ref. 2 had an equivalent noise voltage referred to its input of 45 μV.

The voltage gain of the differential amplifier does not need to be high as the amplifier's main function is to remove the common mode signal and buffer the output so it can be taken off chip.

(b) CHARGE SENSITIVE AMPLIFIER

Figure 5 shows the arrangement of charge sensitive amplifiers before the differential output stage. If the charge sensitive amplifier has a high gain then the split electrode taps are held at virtual earth. Thus the potential of the electrodes changes very little as signal charge arrives, which improves linearity and reduces cross coupling between the gates.

The output voltage of the charge sensitive amplifier is given by $v_o = \frac{C\phi}{C_F} v_{in}$. Typical values might be $C\phi$ = 100 pF, C_F = 50 pF and v_{in} = 2 volt so that v_o will be of the order of 4 volts and the amplifier will need a fairly high dynamic range. The gain A of the charge sensitive amplifier should be high enough that the change in potential on the gate electrodes $V_\phi = \frac{v_o}{A}$ is a few 10's of millivolts. Hence A > 100. The linearity of the amplifier is not critical and so overall the requirements for the charge sensitive amplifier should be easier to meet than for the floating gate differential amplifier. The output impedance of the charge

sensitive amplifiers should be low enough to drive off-chip, but the following differential amplifier could also be integrated on-chip.

Both output techniques (a) and (b) require amplifiers with a wide bandwidth so the filters can be used up to a few MHz. Conventional MOS amplifiers are usually inadequate. The amplifiers should also have low power dissipation so that the storage time of the CCD is not degraded for low frequency applications.

APPLICATION OF HIGH GAIN/WIDE BANDWIDTH AMPLIFIERS TO FEEDBACK LINEARISATION OF THE CCD OUTPUT

MacLennan and Mavor (ref. 4) have described the specification for an on-chip amplifier to provide feedback linearisation of the CCD output. The output voltage V_{out} is related to the input voltage V_{in} by $V_{out} = V_{in}/(1 + 1/A_1A_2)$ when feedback is applied, where A_1 is the gain of the differential amplifier and A_2 is the variable loss between the voltage applied to the input diode and the sense amplifier output. A_2 is usually about 0.25 over most of the range of signal charge, so that a value of $A_1 \geq 100$ will give much improved linearity.

The differential amplifier should have low input drift and wide bandwidth. Although these requirements are difficult to achieve MOS amplifiers might be adequate up to a few MHz. However, it is much easier to meet the requirements with an on-chip bipolar amplifier.

DESIGN OF A BIPOLAR AMPLIFIER FOR ON-CHIP CCD APPLICATIONS

Figure 6 shows the circuit diagram of two amplifiers for evaluating the capability of the CCD compatible bipolar process. The pre-amplifier is a single-ended input voltage amplifier with series feedback. It is designed to be used with a junction FET input to produce a low noise buffer stage. It also has low input impedance, high gain and high input impedance, low gain options. It is proposed that the junction FET should be integrated with the amplifier using the bipolar process, and a design study is in progress at present. The main amplifier consists of a transresistance amplifier with an internal feedback resistor followed by an emitter follower output stage. The target specification for the amplifier is given in Table 3.

TABLE 3

Pre-Amplifier

Frequency response flat to	>2 MHz
O/P impedance	300 ohm
I/P impedance (dependent upon external resistor) max.	1Mohm
Gain	up to 200
Dynamic range input voltage	1V p-p to noise level
Input noise with a source resistance $\approx$ 50 ohm	7 μV

Main Amplifier

Frequency response flat to ≈ 100 KHz

Gain (dependent on source resistance) 1000 max.

Further development of the amplifier design is necessary to meet the requirements of the applications discussed previously. For the feedback linearisation technique a differential input is needed but the dynamic range, gain and frequency response of the preamplifier appear to be adequate for this application. With the addition of a low noise junction FET it appears that the preamplifier would be ideal for the charge sensitive amplifier application.

CONCLUSIONS

The on-chip bipolar process for CCD peripheral circuitry offers increased flexibility and improved performance over conventional MOS peripherals at a cost of only one additional photoengraving and ion implantation stage. For clock driver applications it appears that there is a very limited range of frequency over which the bipolar drivers would be useful because of the power dissipation problem. For applications where a high gain/wide bandwidth amplifier is needed on-chip, the bipolar process offers significant improvements over conventional MOS circuitry.

ACKNOWLEDGEMENTS

The authors would like to thank the Plessey Company Limited for permission to publish this article. Part of this work has been carried out with the support of the Procurement Executive Ministry of Defence, sponsored by DCVD.

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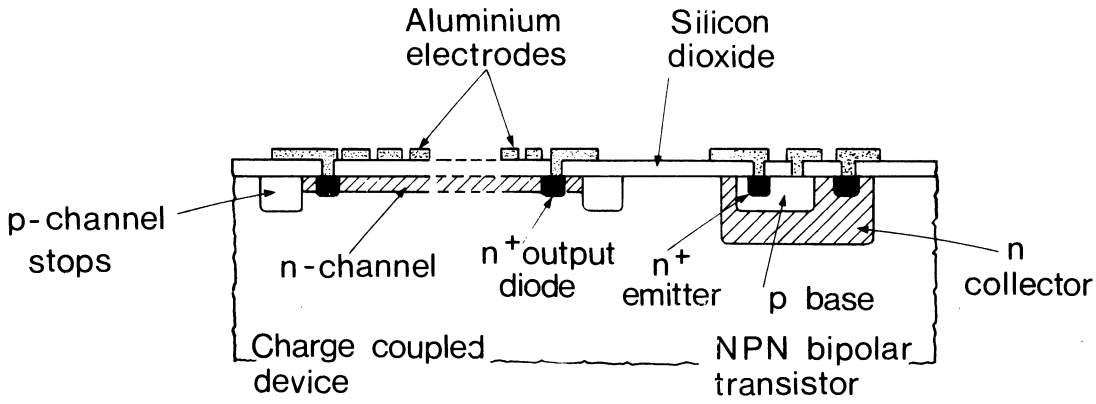

FIG.1. CROSS-SECTION THROUGH DEVICE STRUCTURE

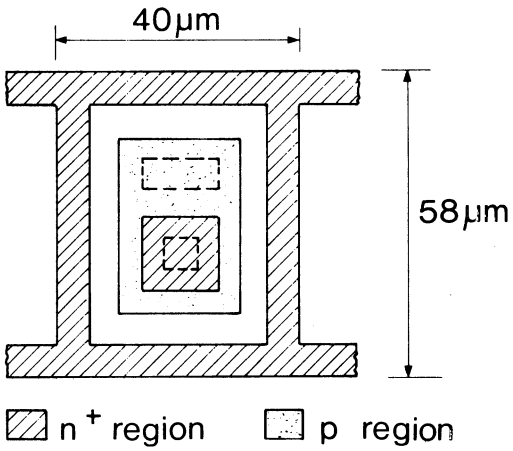

FIG.2. BIPOLAR TRANSISTOR CELL

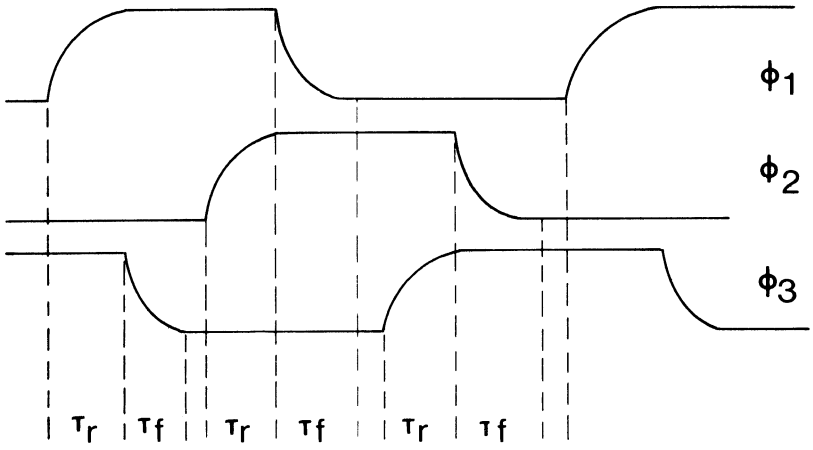

FIG.3. TIMING DIAGRAM FOR 3 PHASE CLOCKS

100pf
ON CHIP CLOCK DRIVERS
25 MHZ
—
FEEDBACK LINEAR

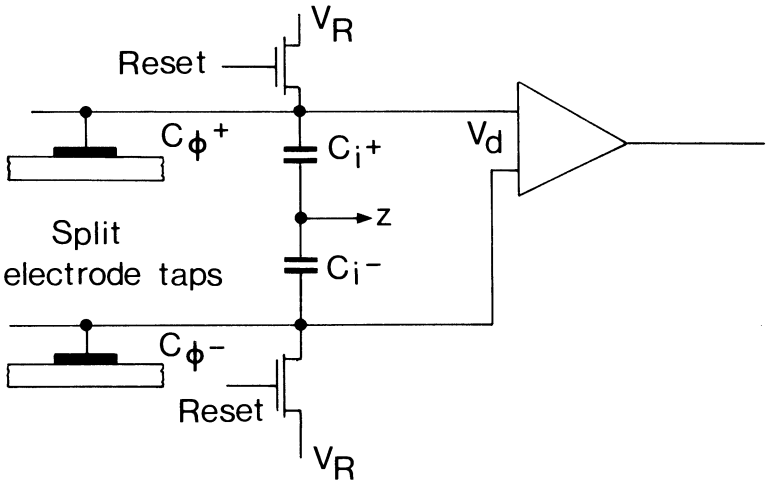

FIG.4. FLOATING GATE TECHNIQUE

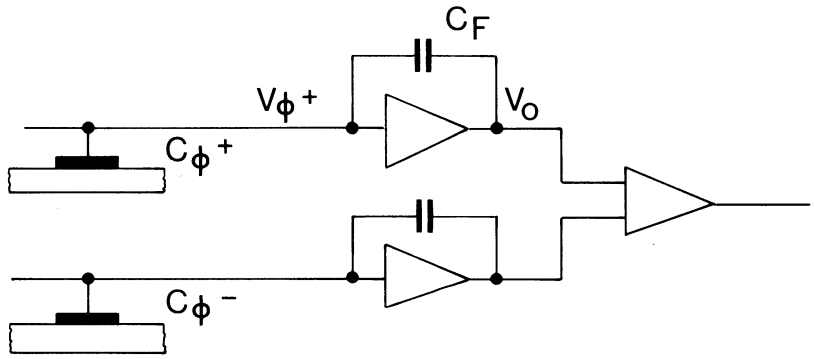

FIG.5. CHARGE SENSITIVE AMPLIFIER OUTPUT

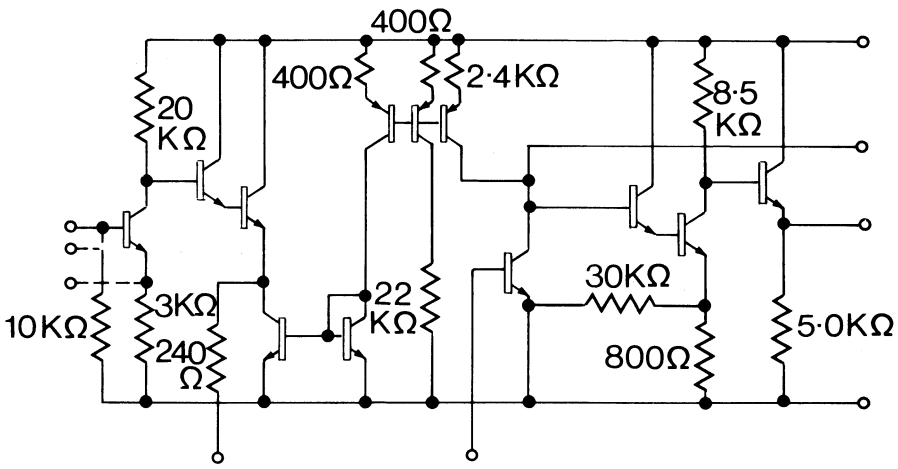

FIG.6. CIRCUIT DIAGRAM