CANCELLATION OF ALIASING IN A CCD LOW-PASS FILTER

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ABSTRACT

The spurious frequencies caused by aliasing in a CCD low-pass filter can be cancelled in the passband by designing a prefilter into the CCD's input stage. In this paper, we describe how single and multiple-stage prefilters can be used, the rejection band and attenuation being set by the number of stages.

INTRODUCTION

Because the input stage of a CCD is also a sampling stage, any input signal whose frequency F_i is close to the sampling or clock frequency F_c will give $(F_c - F_i)$ and $(F_c + F_i)$ components by aliasing.

If the CCD in question is a low-pass filter, the $(F_c - F_i)$ component may fall inside the passband limited to F_b; the spurious frequency will then appear at the filter's output.

Because a CCD transversal filter has not just a single passband, but has one for each multiple of the clock frequency, F_i and alias components derived from F_i and the harmonics of F_c will also be found at the output.

To cancel these spurious frequencies, the bandwidth of the input signal can be limited by a filter that rejects all frequencies above $(F_c - F_b)$. Although this could be done by a simple RC filter, the attenuation obtained would not be sufficient in most cases.

The filter should preferably have the longest impulse response possible (ref 1) or, in other words, it should have a large N/F_c ratio where N is the number of taps. For technological reasons among others, a large value of N is undesirable, so the lowest possible clock frequency should be used (ref 1). This gives a fairly low value for the F_c/F_b ratio, so the anti-alias prefilter must have a fairly sharp cutoff.

Having the prefilter on the same chip as the CCD filter presents many advantages. It has already been shown that, for small signals, the input techniques known as "floating diffusion input" and "potential equilibration input" have an anti-alias filtering effect with a frequency response closely resembling the $\sin x/x$ of an ideal integrator (ref 2). In this paper we explain another way of resolving the problem and of integrating a prefilter into the input stage of the CCD.

PRINCIPLE

The basic prefilter cell is a cosine filter, obtained by delaying the input signal and then adding it to a non-delayed input. The delay used is $T_c/2$ where $T_c = 1/F_c$ is the clock period.

In practice, the input signal is sampled twice with a π phase difference between the two sampling signals. One sampled signal is then delayed by half a sampling period, after which it is added in phase to the other signal in the CCD channel (see Figure 1).

If e(t) is the input signal, after ideal sampling we have:

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$$e_1(t) = e(t) \sum_{k=-\infty}^{+\infty} \delta (t - kT_c)$$

$$e_2(t) = e(t) \sum_{k=-\infty}^{+\infty} \delta (t - kT_c - \frac{T_c}{2})$$

and the output signal is given by:

$$S(t) = e_1(t - \frac{T_c}{2}) + e_2(t)$$

The modulus of the spectrum of the output signal is:

$$\left| S(f) \right| = 2 \left| \sum_{k=-\infty}^{+\infty} E(f - kF_c) \cos(\frac{\pi T_c f}{2} - k \frac{\pi}{2}) \right|$$

where E(f) is the spectrum of the input signal.

In this equation we see that the input spectrum is rendered periodic by the sampling, this being called aliasing. But each alias spectrum for each value of k is multiplied by a sine or cosine function centered around multiples of the clock frequency, this being a filtering effect.

Figure 2 shows the output spectrum for an input spectrum of width B centered on the clock frequency.

The sampling signal is not an ideal δ function. In general, "sample and hold"during half the clock period is used in CCD's. Thus, the output spectrum is multiplied by a sin x/x function whose zeros fall on multiple values of $2F_c$ (see Figure 3).

Because this single-stage filter design does not give adequate rejection of all of the band of width $2F_b$ centered on F_c, two or three stages may be connected in series.

It can be shown that, for n stages in series, the output spectrum is given by:

$$\left| S(f) \right| = 2^n \left| \sum_{k=-\infty}^{+\infty} E(f - kF_c) \cos^n (\frac{\pi T_c f}{2} - k \frac{\pi}{2}) \right|$$

The alias components around zero frequency (k = -1) are thus filtered by $(\sin \frac{\pi f T_c}{2})^n$.

Figure 4 shows the attenuation around clock frequency obtained with one, two, and three-stage prefilters.

Examples

- With a two-stage prefilter, and a low-pass filter of passband F_b and clock frequency $8F_b$, the attenuation of alias components is more than 28 dB with an attenuation at the edge of the passband of 0.3 dB;

- For the same arrangement but using a clock frequency of $16F_b$, the attenuations are more than 40 dB for alias components and 0.08 dB at the edge of the passband;

- With a three-stage prefilter and a clock frequency of $8F_b$, the attenuations are more than 42 dB for alias components and 0.5 dB at the edge of the passband.

Of course, passband attenuation by the prefilter can be compensated for in the design of the low-pass filter.

Instead of connecting several stages in series, the equivalence:

$$2^n \left| \cos \frac{\pi f T_c}{2} \right|^n \equiv \left| 1 + \exp (- j\pi f T_c) \right|^n$$

can be used. Having expanded this expression by the binomial theorum, the filter can be obtained by splitting the CCD channel into several parallel parts. The width of a subdivision corresponds to the coefficient of a binomial term and the delay is proportional to the power of the term. The filter will be said to be of order n.

Figure 5 compares a two-stage filter and a second-order "binomial" filter.

Figure 6 shows a third-order binomial filter.

Thus, for a second-order prefilter, the output signal is obtained from the non-delayed input added to the $T_c/2$ delayed input tap-weighted by 2 and the T_c delayed input tap-weighted by 1.

DESIGNING THE PREFILTER INTO A CCD

This description concerns a two-phase CCD. The basic design is shown in Figure 7. The beginning of the CCD channel is split into two parts, each having its own input stage. The input diodes are connected together and are held at a reference potential. The first gates are driven by two short sampling signals ϕ_{s1} and ϕ_{s2}, respectively in phase with ϕ_1 and ϕ_2. Thus, there is a phase difference of π between ϕ_{s1} and ϕ_{s2}.

The input signal is applied to a second gate, common to the two channels. In one channel the signal is transferred in two steps whereas in the other it is transferred in one step. So, the signal is delayed by $T_c/2$ in the first channel.

The signals are then added under a common electrode where the two channels have joined to form a single channel.

The split electrodes of the CCD filter start in the next stage.

Figures 8 and 9 show two ways in which the prefilter designs of Figure 5 can be realized on the CCD chip.

The first method (Figure 8) uses two stages of the type shown in Figure 7, connected in parallel and having a phase difference between the inputs. The channel is initially split into four parts which eventually join to form two parts. In one of the two parts the signal is delayed again by a two-step transfer, and the signals are then added under a common electrode where the two parts have rejoined to form a single channel.

The second method (Figure 9) employs the binomial expansion. The channel is divided into three parts with three parallel input stages.

The middle channel being of double width, the charge injected into it is twice that injected into the others. The signal has a one-step transfer in the first channel, a two-step transfer (delay $T_c/2$) in the second, and a three-step transfer (delay T_c) in the third. The three signals are then added under a common electrode where the channels have joined.

For a third-order prefilter, the channel must be split into four parts, the width of the inner ones being three times that of the outer ones.

The number of transfer steps are respectively 1, 2, 3, and 4, giving delays of 0, $T_c/2$, T_c, and 3 $T_c/2$.

The four signals are then added under a common electrode.

CONCLUSIONS

We have explained that an anti-alias prefilter can be integrated into the input stage of a CCD low-pass filter.

In most cases, a two or three-stage prefilter gives adequate rejection of the spurious frequencies caused by aliasing. But using the principles given in this paper, a more complex, non-recursive prefilter could be designed into the input stage. The technique is to split the channel into several parts; the width of each part determines the tap weighting and the number of steps in it is determined by the delay required. The signals are then added under a summing electrode which is the first stage of the CCD filter. A prefilter with a sharper cutoff frequency than $(\text{cosine})^n$ can be obtained in this way.

A low-pass CCD filter incorporating a second-order prefilter of this type has been designed and built, and is presently being tested.

ACKNOWLEDGEMENTS

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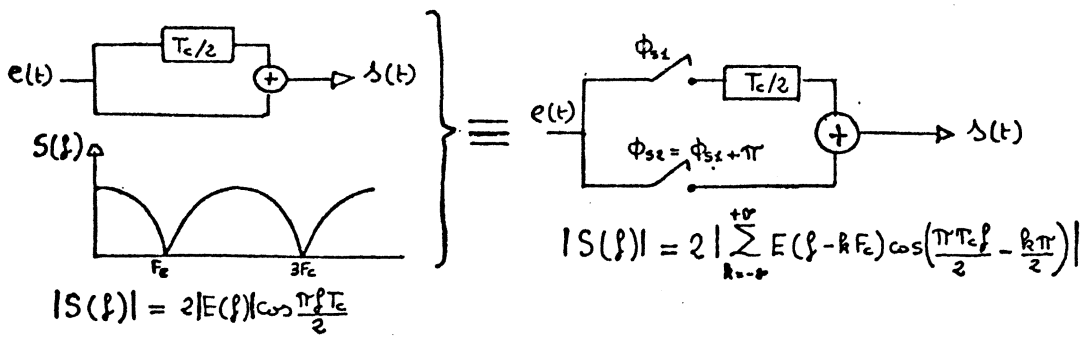

Fig. 1

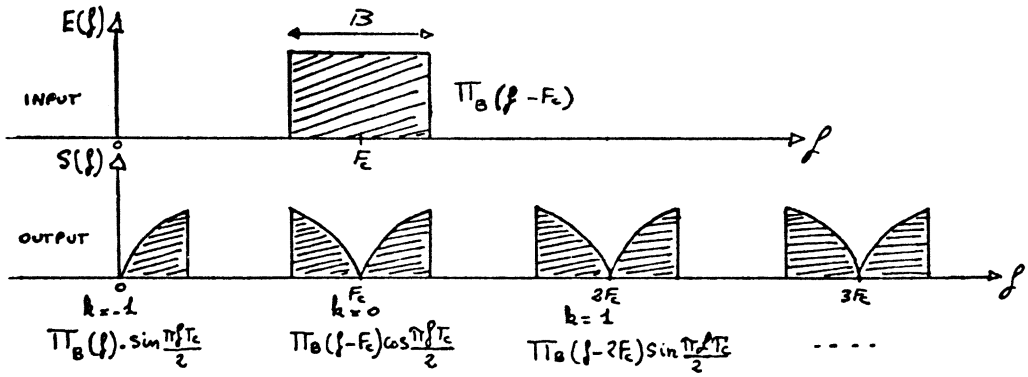

Fig. 2

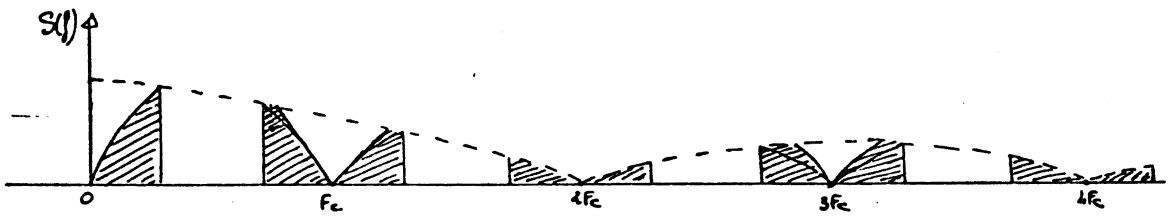

Fig. 3

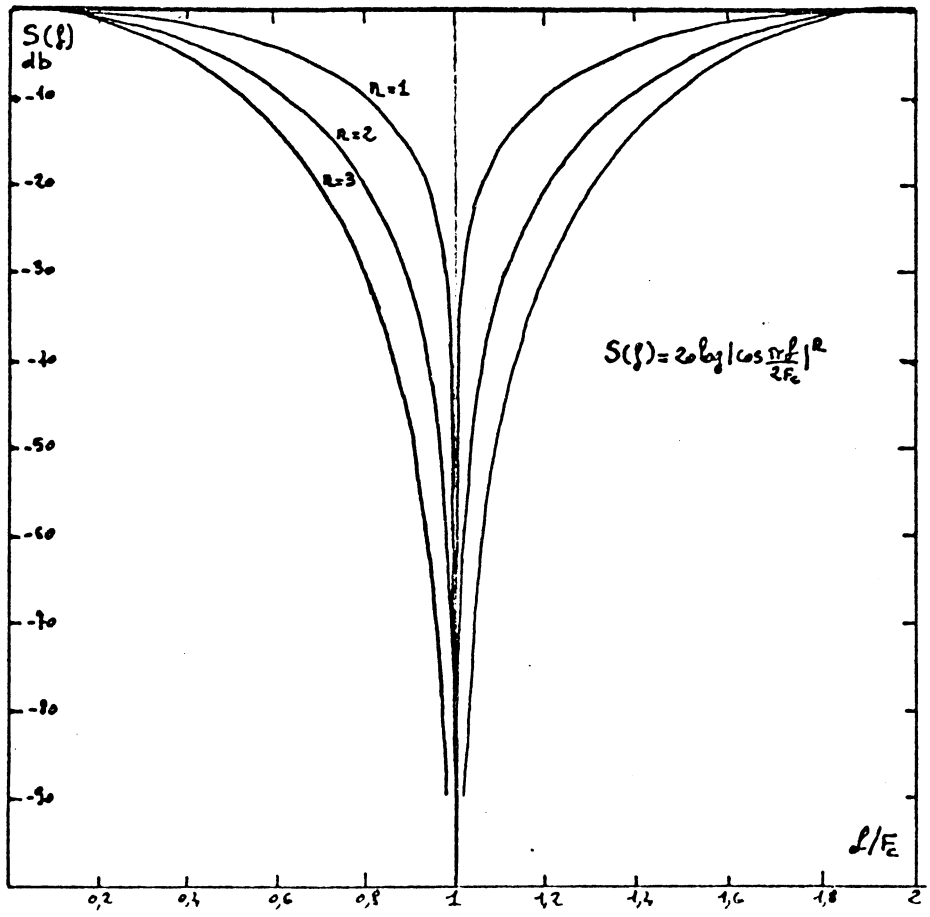

Fig. 4

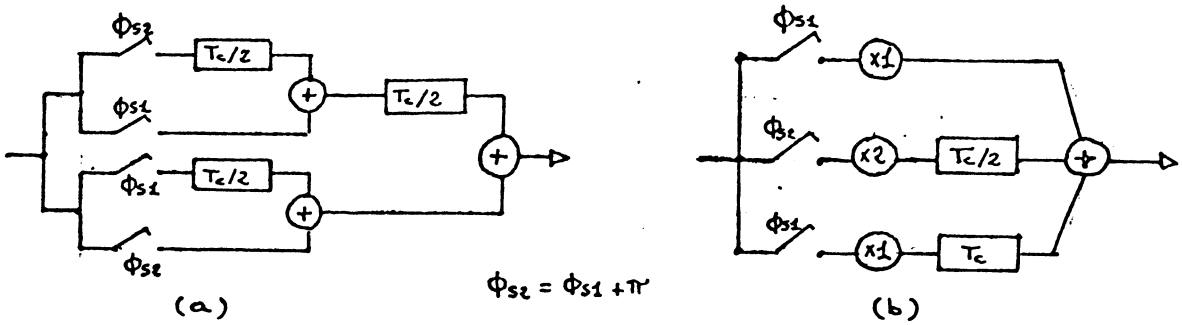

Fig. 5

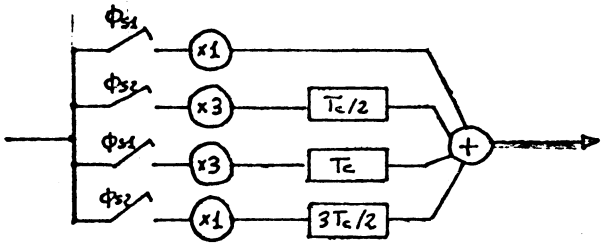

Fig. 6

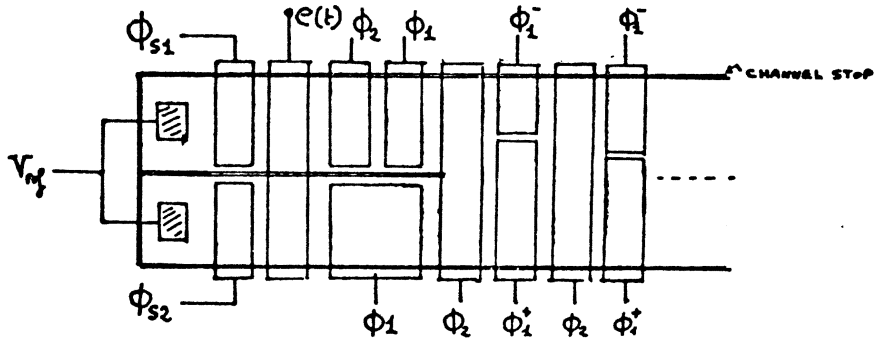

Fig. 7

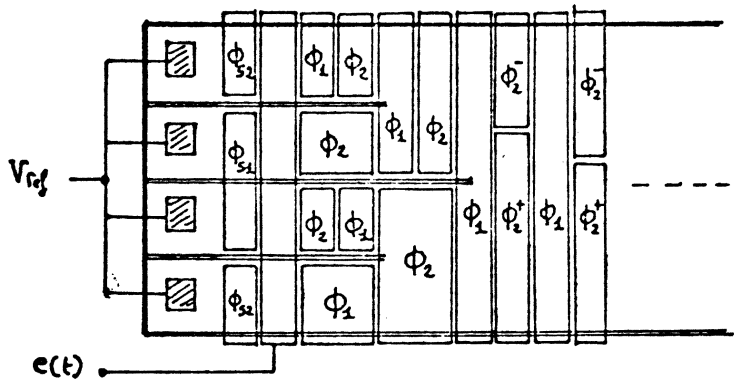

Fig. 8

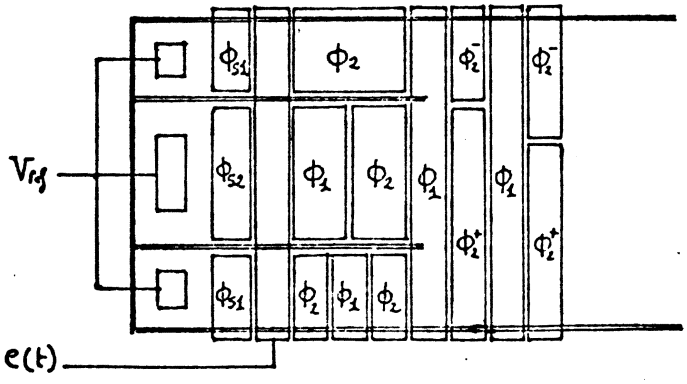

Fig. 9