SIGNAL PROCESSORS INCORPORATING CCD SHIFT REGISTER TIME COMPRESSORS

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ABSTRACT

The paper reports two distinctly different approaches to the design of signal processors which are based on time compression techniques implemented with Charge-Coupled Device (CCD) shift registers. In the recirculating correlator, 1024 samples of the input waveform are stored in a digital CCD memory. High speed serial processing, where the stored data is non-destructively recirculated at 1025 times the input sample rate, is subsequently employed to implement an infinitely programmable matched filter. Conversely the analogue time compressor loads 100 samples of the input signal into a CCD analogue shift register. The stored information is accessed by increasing the clock rate by a factor of 100-1000 to time compress and bandspread the signal for subsequent processing in a Surface Acoustic Wave (SAW) correlator. These time compressors are attractive for multiplexing many narrow band inputs into a single sophisticated wideband SAW Signal processor. The design of the two modules is reported and their operation is demonstrated correlating both linear FM and PN-PSK input waveforms.

INTRODUCTION

A requirement exists for cheap, lightweight, high performance, analogue matched filters and correlators for sonar, vibration analysis and other relatively low data rate signal processing applications. This paper recognises the recent development of the potentially attractive Charge-Coupled Device (refs. 1,2) (CCD) but notes that, high time-bandwidth (TB) product, programmable, tapped, CCD shift registers are difficult to obtain commercially. This has resulted in our focussing attention on processors which use relatively standard shift register memories. The two modules reported here utilise bandwidth expansion techniques employing CCD shift register time compressors.

CCD SHIFT REGISTERS

Central to any time compressor is the requirement for a memory whose contents may require to be non-destructively recirculated. CCD shift registers can be designed for either analogue or digital operation. When storing and recirculating large amounts of information, it is necessary to periodically refresh or regenerate the signal charge. Regeneration stages must establish the "fat zero", compensate for signal attenuation, and shift the d.c. voltage levels appropriately. In digital CCD's on-chip refresh, recirculate and switching operations can be incorporated at will, but they are usually located at corners of the memory.

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With a serial, analogue CCD memory the information must be sampled-and-held and then restored to precisely the appropriate d.c. level at each regeneration stage. When attempting to realise a linear, analogue CCD memory it is preferable to design it in one complete section for memories up to 1 Kbit length without refresh. Conversely digital CCD's may be refreshed every 128 bits if required. In recirculating stores, the gain of analogue CCD's must be held accurately and stabilised against variations in temperature. Feedback linearisation (ref. 3) could be employed but when the loop is closed, instabilities occur due to charge transfer inefficiency. These are compounded after many recirculations at unity gain.

Possible techniques for improving the performance of CCD analogue recirculators include: (a) precoding the input data, to cancel the major effects of charge transfer inefficiency, followed by decoding (ref. 4), (b) operating the recirculator with a closed loop gain of less than unity, followed by the required compensation, and (c) using alternative organisations of CCD registers which reduce the number of transfers. For example the serial-parallel-serial (SPS) organisation improves the overall transfer efficiency. However as the signal charge moves in different parts of the silicon chip fixed-pattern noise can result.

The digital, recirculating shift register, whilst not being susceptible to the stability problems of the analogue system, does require an associated A-to-D converter. However, high precision (12 bit) converters for low data rates are not expensive. The digital CCD requires many parallel channels which would appear to consume far more chip area than a single, analogue channel. However, a wider channel is required in the analogue CCD to achieve adequate SNR, resulting in both approaches requiring comparable chip area. Table 1 summarises the main features of analogue and digital CCD registers.

TIME COMPRESSION

The first signal processor module, Figure 1, combines an Automatic (ref.5) Recycling Multiple Sampler (ARMS) processor with a high speed serial multiply and integrate correlator. This recirculating correlator comprises an N x M stage digital CCD shift register memory. N samples of the input baseband signal are taken at a slow sample rate. Each sample is A-to-D converted into an M bit word and stored in the memory. The memory contents are continuously recirculated at a rate many times the input sample rate, with one new sample added each recirculation, Figure 2(a), displacing the oldest memory sample. Thus in the time interval between samples the memory recirculates all N samples to provide a non-destructive history of the input data, time compressed by the factor N + 1, Figure 2(a). For an input sample rate of R Hz the memory clock rate must be (N + 1)R Hz.

Matched filtering is achieved by storing N samples of the required reference waveforms in the associated reference store, Figure 1. Correlation is obtained by multiplying each of the high speed recirculating input samples with the corresponding stored reference sample and integrating over all N samples. This yields one point of the cross correlation function between the signal and reference. The adjacent point is obtained on the next memory recirculation after updating the memory with a new input sample. Thus we have implemented a real-time matched filter for narrow band signals at the expense of high speed multiplication and integration. Infinite programmability is achieved when a Random Access Memory (RAM) is used for reference storage.

The operation of the alternative analogue time compressor is demonstrated in Figure 2(b). On the read cycle the input signal is again sampled at a slow rate but here the N samples are simply stored as analogue voltage levels in an N stage CCD shift register. The sample rate, R Hz, is controlled by the CCD clock rate. When full, the time compressor is changed to the write cycle increasing the clock rate by S, the time compression ratio. The stored samples are then destructively read out at a rate S x R Hz. If the time taken for the read cycle is Tsec then the write cycle duration is only T/S sec. Thus the output signal bandwidth is expanded with respect to the input signal by S, the time compression ratio. The attraction of CCD's is that they are clock programmable which permits the design of a widely variable time compressor.

This CCD time compressor has considerable application in sophisticated signal processors (ref. 6) when interfaced with Surface Acoustic Wave (SAW) devices. SAW components such as correlators and matched filters (ref. 7), which are readily available for pseudo noise (PN), phase shift keyed (PSK) and linear frequency modulated (FM) chirp waveforms, have demonstrated high performance. However, they are generally limited to fixed signal bandwidths. The development of the programmable analogue time compressor now permits long duration (> 50 μsec) narrow band signals to be time compressed for subsequent processing in SAW devices. The complementary nature of the technologies (ref. 8) ensures that the maximum CCD bandwidth overlaps with SAW capabilities. The use of simple CCD shift registers overcomes the requirement for tapping and the short duration write cycle permits many analogue CCD time compressors to be multiplexed into a single SAW processor.

RECIRCULATING CORRELATOR MODULE

Here we report the operation of a prototype recirculating correlator, Figure 6(a) based on a digital Fairchild 450 CCD shift register memory (ref. 9). The memory holds N = 1024 input samples as M = 9 bit words. The maximum memory clock rate is 3 MHz but the module currently operates at just greater than ½ MHz recirculation rate to give a 500 Hz correlator input sample rate. The reference store also holds 1024 8 bit binary samples which are loaded through the input A-to-D converter. Multiplication is performed in a DATEL MI 10B multiplying D-to-A converter with subsequent integration within operational amplifiers. In many instances it may be adequate to use only one bit reference quantisation. This reduces the multiplication to a simple sign change permitting the integration to be simply performed digitally.

The performance of the module with three different input baseband signals is shown in Figure 3. Firstly, an unmodulated 992 msec pulse burst at 15 Hz is used as signal and reference. Figure 3(a) shows the auto-correlation function output from the correlator. In Figure 3(b) a linear FM waveform is used which sweeps from 10 Hz to 100 Hz in 992 msec. The Figure again shows the autocorrelation function, which was built up by many separate exposures, each representing a different input signal phase. Since the signal is at baseband all traces lie within the (sinx)/x envelope shown. Figure 3(c) shows the correlation of a baseband 31 bit PN sequence. The sequence clock rate is 500/16 Hz resulting in a sequence duration of 992 msec. As the input sample rate is 500 Hz there are only 32 sampling points in the correlation peak.

This recirculating correlator module is limited to low (< 1 kHz) sample rates by the memory length clock rate and the multiplying D-to-A converter

settling time. Increased sampling rates can be achieved by using parallel channels operating on shorter data blocks. However, the parallel approach is ultimately limited by the operating speed of the multiplying D-to-A converter, unless a digital multiplier is used.

ANALOGUE TIME COMPRESSOR MODULE

This section reports the results obtained with several analogue time compressors based on CCD shift registers.

Experimental results for the first baseband time compressor, constructed with a single 3-phase GEC CD100 100 stage CCD register, are shown in Figure 5(a). This compressor reads in analogue samples of a 1.2 kHz sinewave, upper trace Figure 5(a), at a 20 kHz sample rate. The 60 kHz read cycle clock rate for the three phase CCD is obtained by dividing the output from a 6 MHz master oscillator in an S = 100 stage counter. A separate 100 stage counter controls the number of sample points N. It automatically inhibits the input and switches the master oscillator directly onto the CCD clock drivers during the write cycle. This outputs the time compressed 120 kHz sinewave, lower trace of Figure 5(a), at a 2 MHz sample rate.

The second time compressor, Figure 6(b), which is shown schematically in the solid lines of Figure 4, is designed to operate directly with a modulated IF input. It is based on two, 100 stage, 3-phase GEC MA 318 CCD shift registers. The input signal is mixed with sin and cos samples of an IF reference frequency, ω_1, which sets the time compressor input centre frequency. The bandwidth is controlled by the CCD sampling frequency. The provision of phase and quadrature channels with separate CCD shift registers permits the time compressor to operate asynchronously on complex inputs at any desired frequency.

Roberts (refs. 2,6) has combined a similar CCD time compressor with a SAW spectrum analyser for radar doppler processing. In principle the time compressor can also be combined with a SAW Fourier Analyser extending the capabilities of SAW real time network analysers (ref. 10) to narrower bandwidth and finer resolutions.

This paper reports the performance of a programmable CCD/SAW correlator module. Firstly, we examine operation with a phase modulated IF input. Here a degenerate acoustic convolver, see Reeder (ref. 7), was selected for the SAW matched filter. This required the time compressor output to be modulated onto an IF carrier (ω_2, Figure 4) at the convolver centre frequency. The reference was obtained by wideband phase modulating the same IF with the appropriate time reversed code, dotted lines Figure 4. The selected input test waveform was a 40 MHz IF, phase modulated at 10 kHz rate by a 15 bit PN sequence. The sequence duration of 1.5 msec matched closely the 2 ms time compressor read cycle (50 KHz sample rate).

The input is demodulated against a ω_1 = 40 MHz reference, sampled every 20 μsec and read into the time compressor. After compression by 100 the output baseband waveform, upper trace Figure 5(b), is phase modulated on to an ω_2 = 120 MHz carrier and input to the SAW convolver. The reference, a time reversed 15 bit PN code is modulated at 1 MHz rate onto a separate sample of the same 120 MHz carrier. The lower trace of Figure 5(b) shows the output from the SAW convolver at 240 MHz. Discrepancies from theory in the displayed autocorrelation function are attributable both to band-limiting in the CCD, Figure 5(b), due to charge transfer loss, and

degradations in the performance of this SAW convolver, arising from acoustic reflections and electromagnetic effects.

Secondly, the module was tested with a linear FM input. Although this waveform could also be correlated in the SAW convolver it was replaced by a SAW chirp filter, see Paige (ref. 7), possessing superior performance. The selected filter, which operated at 17 MHz had 2 MHz bandwidth and 20 μsec dispersive delay. The input to the module was a 2 msec duration baseband sweep from DC to 15 kHz. After time compression by 100, upper trace Figure 5(c), the output was mixed with a 16.25 MHz carrier and input to the SAW chirp filter. The final autocorrelation function is shown in the lower trace of Figure 5(c). The distortions from theoretical (sinx)/x response are due primarily to non-linearities in the baseband FM input. Apart from minor degradations, Figure 5 clearly demonstrates the potential of this sophisticated signal processor to sequentially correlate many low data rate inputs in a single wideband SAW matched filter.

MODULE COMPARISON

These prototype modules have demonstrated the performance capabilities of CCD-based time compressor signal processors. A brief comparison with the competing matched filters based on tapped CCD shift registers is provided in Table 2, illustrating the projected bounds on bandwidth and TB product for these correlators.

The prime advantage of the recirculating correlator arises from the use of digital CCD's. With regeneration they can store signals for long periods (>1 sec) without suffering from dark current effects. However, the recirculating correlator is limited in maximum speed by the multiplying D-to-A converter and the number of sampling points, unless digital multiplication and integration is used. Thus it is best suited for processing narrow band, long duration signals.

The analogue time compressor, which can in principle be followed by either a CCD or SAW transversal filter, is attractive for both its relative simplicity and multiplex capability (ref. 6). Analogue sampling reduces the number of memory stages but charge transfer inefficiency still limits untapped CCD shift registers to <1000 stages. Thermally generated dark currents restrict the storage time setting consequent limits on the minimum bandwidth, time compression ratio and number of sample points Table 2. In comparison individual CCD correlators based on tapped transversal filters are limited to ~ 500 taps when fixed coded, Buss (ref. 2), and ~ 50 when programmable, see Herrman this conference. Cascading may be employed to improve these figures. Although the performance capabilities of CCD analogue time compressors and tapped transversal filters are broadly similar, the availability of untapped CCD's coupled with the capability of multiplexing many time compressors into one signal processor are powerful advantages for the simple analogue time compressor.

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	Analogue CCD	Digital CCD
Advantages	Direct Analogue Charge Storage	Recirculation Easy — Potentially Dense Memory
Disadvantages	Recirculation Difficult	A-to-D Conversion Requires Additional Memory

TABLE 1

COMPARISON OF ANALOGUE AND DIGITAL CCD SHIFT REGISTERS

Recirculating Correlator	Analogue Time Compressor (Plus SAW Matched Filter)	Tapped CCD Matched Filter
Digital CCD	Analogue CCD	Analogue CCD
High Clock Rate For Low Data Rate	Dual Speed Clock	Low Speed Clock
Untapped CCD	Untapped CCD	Tapped CCD
Infinitely Programmable Through Memory and Sample Rate	Bandwidth Prog. in CCD - Code Prog. Through SAW Convolver Reference	Bandwidth Prog. Via. CCD Clock — Fixed Coded Or Programmable
TB = 100 - 100,000 B = 10^{-2} - 10^{4} Hz	TB < 1,000 B = 1 - 100 kHz	TB < 500 B = 1 kHz - 5 MHz
Here Today	Development Equipment	Not Readily Available

TABLE 2

COMPARISON OF CCD BASED PROGRAMMABLE MATCHED FILTERS

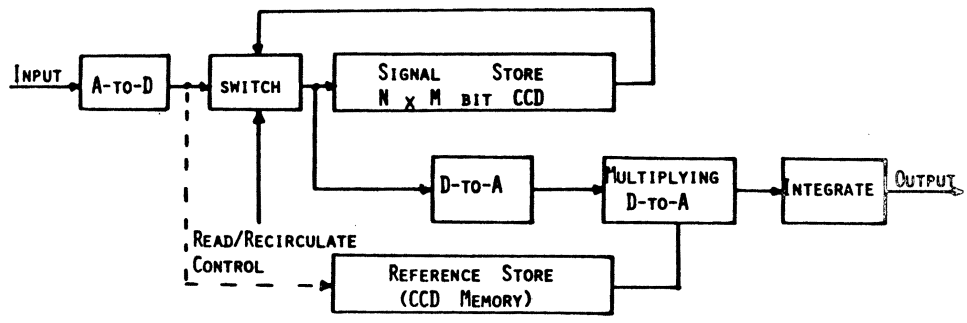
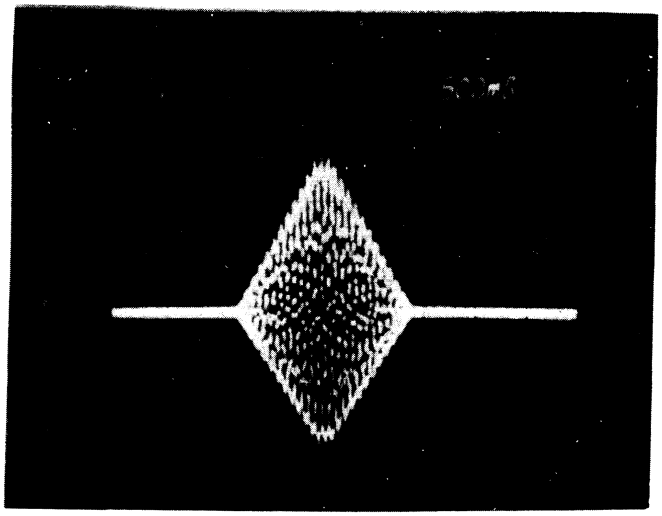


FIGURE 1 CCD RECIRCULATING CORRELATOR



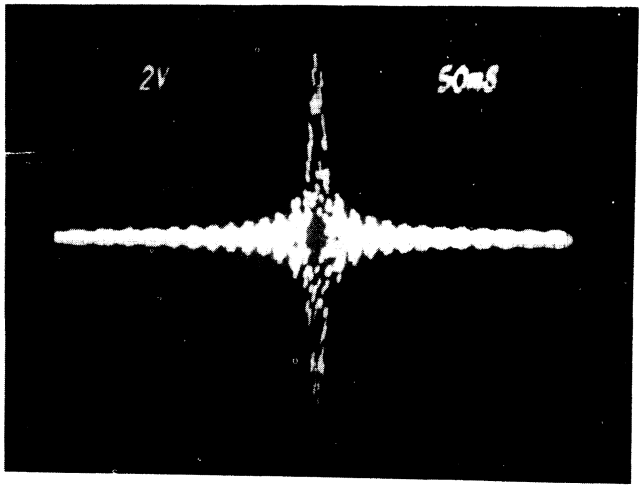
INPUT

992 mSec pulse burst at 15 Hz

OUTPUT

Single shot

(a)



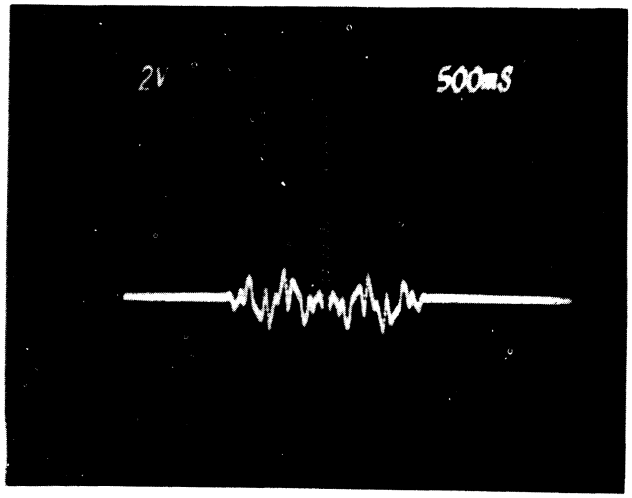
INPUT

992 mSec pulse burst of 10 Hz - 100 Hz linear FM, TB = 89

OUTPUT

Multiple exposure

(b)



INPUT

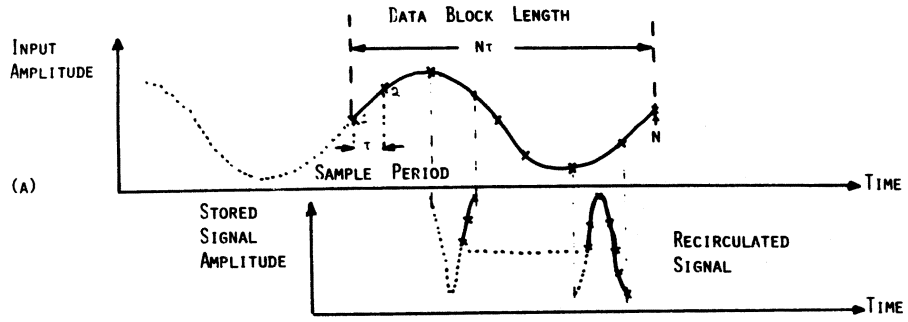
992 mSec burst modulated with 31 bit PN code. TB = 31

OUTPUT

Single shot

(c)

FIGURE 3 CORRELATION OF CODED WAVEFORMS WITH THE PROGRAMMABLE CCD RECIRCULATING CORRELATOR



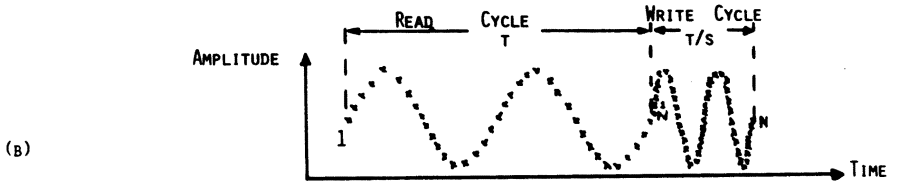


FIGURE 2 PRINCIPLES OF TIME COMPRESSION

(A) RECIRCULATING CORRELATOR
(B) ANALOGUE TIME COMPRESSOR

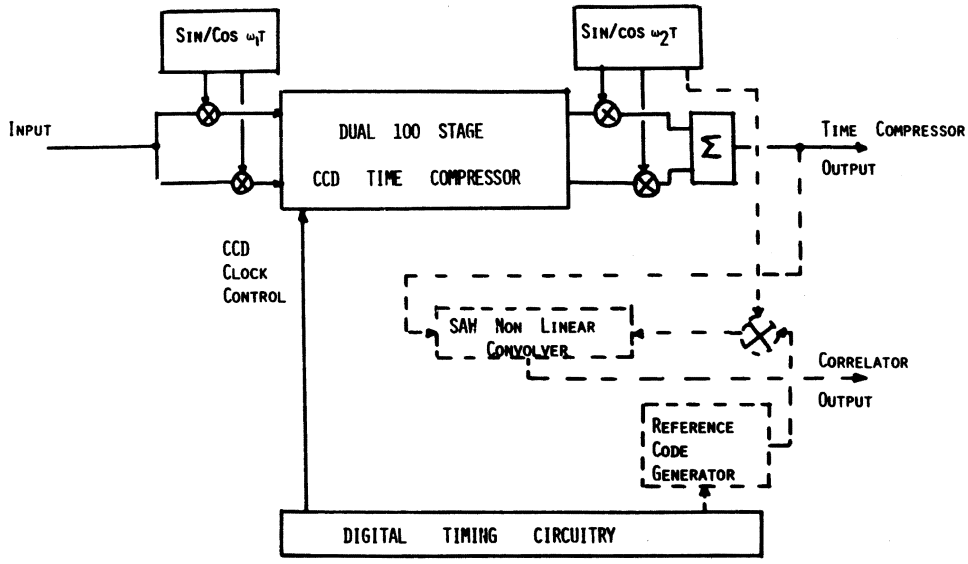
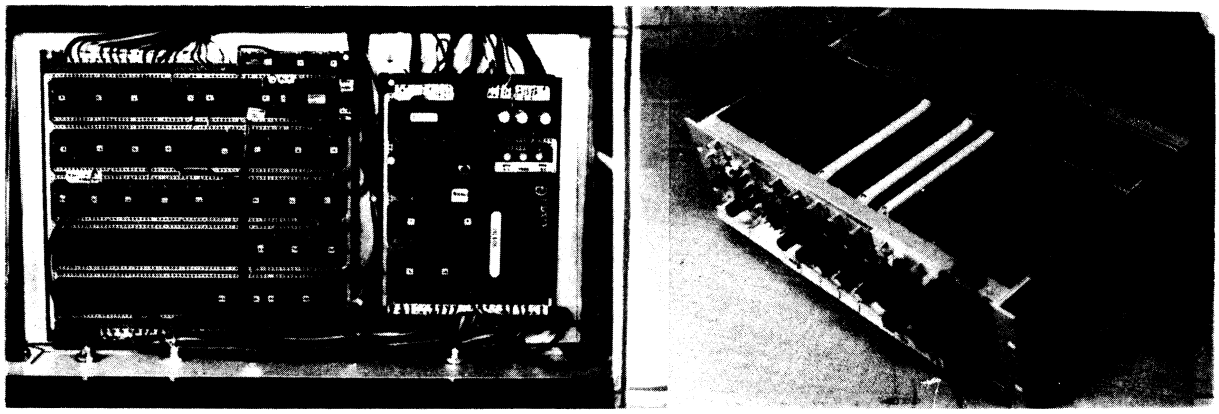
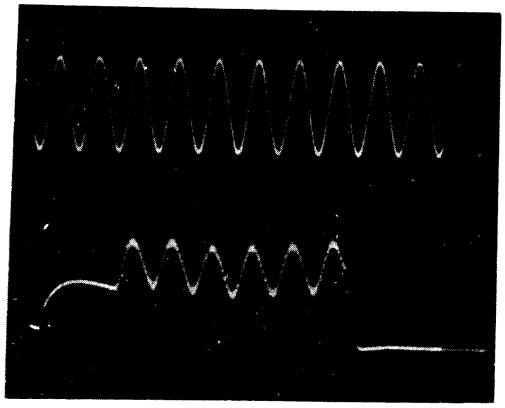


FIGURE 4 CCD ANALOGUE TIME COMPRESSOR PLUS SAW CORRELATOR



(a) (b)

FIGURE 6 CCD TIME COMPRESSOR MODULES



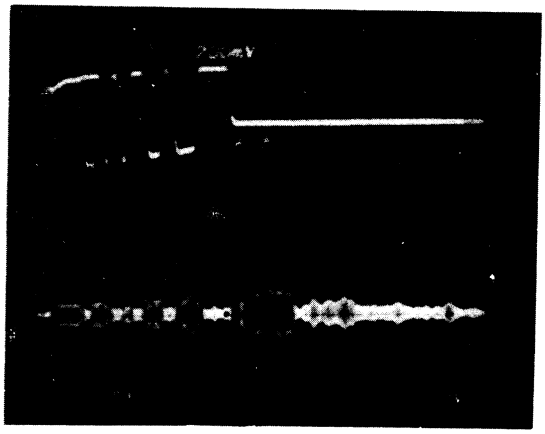
Input at 1.2 KHz

Output at 120 KHz after 100 times compression

(a)

SINGLE CHANNEL COMPRESSOR

(Courtesy E.W. Patterson)

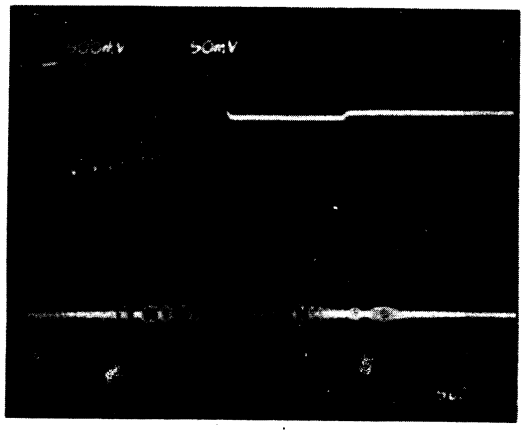


Baseband compressed output

Autocorrelation function of 15 bit PN code at 240 MHz

(b)

TIME COMPRESSOR PLUS SAW CONVOLVER



Baseband compressed output

Autocorrelation function of linear FM input at 17 MHz

(c)

TIME COMPRESSOR PLUS SAW CHIRP FILTER

FIGURE 5 CCD ANALOGUE TIME COMPRESSOR - SAW SIGNAL PROCESSOR OPERATION