CCD ACCUMULATORS IN SPREAD SPECTRUM SIGNAL IDENTIFICATION

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ABSTRACT

This paper presents the evolution of a new charge transfer method for performing the averaging or smoothing function required in a spread spectrum communications system. This charge transfer device combines the accuracy of the nonrecursive method with the small component count and simplicity of the recursive filter approach. The new method also permits variation of the time constant by purely electrical means.

In the original system, a digital implementation, using high speed A/D's plus the requisite logic, was selected to perform this operation on the basis that a straightforward CTD delay line recursive filter would suffer from excessive cumulative error. As a result, this portion of the system occupied a major portion of the overall assembly.

A description of the chip operation is given, and the new accumulator chip implementation is contrasted with a digital approach. Hardware built around the new accumulator chip resulted in a fourfold parts reduction for this function.

INTRODUCTION

In an existing spread spectrum communications system, using Surface Charge Correlators (ref 1, 2), a recursive filter is used as part of a signal identification and tracking function. The filter provides an estimate of a repetitive signal by smoothing or averaging.

Direct sequence spread spectrum systems (ref 3) provide processing gain which is useful in a noisy environment. After detection of a signal through correlation of the received sequence, noise due to correlation side lobes or noise produced by extraneous emitters may produce undesired responses.

The purpose of the signal identifier in the communication system is to provide an estimate of a repetitive signal by smoothing the detected correlation output in a recursive filter such that the output does not reflect the random noise of any particular waveform specimen, but can vary slowly in case the signal itself is not exactly repetitive (i.e., has amplitude modulation). This smoothed function is then used in an adaptive loop to make a decision on the presence or absence of a signal.

With the proper signal modulation, the information obtained can also be used to produce a degree of frequency drift compensation between the sending and receiving set.

The recursive filter shown in Figure 1 can be implemented in both a digital and analog format. It has long been appreciated that charge transfer techniques can provide the function of the analog delay line shown in Figure 1, and that a recursive filter can be implemented using a charge transfer delay line (ref 4, 5). However, as the number of recirculations of the analog data or the number of stages of the delay line increase, this method becomes limited by charge transfer inefficiency. The origin of this problem is the transfer losses of the charge transfer delay line and the fact that these losses are cumulative for all trips around the loop. Thus, if the averaging time constant corresponds to one hundred waveform specimens, the transfer losses will be magnified by one hundred times in comparison with the losses after a single pass. This limitation has precluded the use of charge transfer techniques in a number of applications, and originally prompted the use of a digital implementation in the signal identifier.

This paper will describe a new method for performing averaging or smoothing which combines the accuracy of the nonrecursive method with the small component count and simplicity of the recursive approach. It will also contrast the digital implementation to the charge transfer accumulator mechanization.

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DEVICE DESCRIPTION

The method for achieving the smoothing in the new device uses a relatively large storage region called an accumulator, shown schematically in Figure 2. During each cycle, a new charge sample is added to the accumulator and a fraction α of the stored charge is removed. The new charge samples are added to the accumulator which already holds charge samples from previous cycles.

The fraction α is determined by the ratio of the area of the output electrode to the area of the accumulator electrode. This operation leads to a smoothing function that is identical to that of the recursive filter implementation, but since charge samples are not repeatedly transferred, the method does not require exceptionally high transfer efficiencies.

A surface charge implementation of this new method is shown in Figure 3. One key idea is that the packet of surface charge in the accumulator may be split into two portions of predetermined ratio by the action of a parallel transfer gate. When the parallel transfer gate ϕ_P is closed, a fraction of the total charge will be isolated in the output section ϕ_D. This fraction is given by the ratio of the area under the ϕ_D electrode to the total area under ϕ_D, T_1, T_2, and T_3. By adjusting the active area of the accumulator, the fraction of the charge removed α and therefore the time constant of the filter may be controlled. This may be accomplished conveniently by turning off some of the electrodes labeled T_1 - T_3. The various sections of the accumulator can be coupled either with a diffusion or an overlapping gate.

The structure of Figure 3 can be generalized to more than one sample in order to average an extended waveform. This is accomplished by delivering each of the sequential (corresponding) samples to separate structures of the type shown. A serial transfer analog shift register which has the capability of emptying charge to the side as well as for transferring it along its length is used to deliver the charge samples. The same analog shift register can be used to output the averaged charge samples. Thus, the ϕ_D electrode shown in Figure 3 which is one stage of the serial analog shift register serves as both input and output for charge samples. In operation, a number of charge samples are transferred sequentially down the analog shift register until the charge samples have reached the appropriate cells. The parallel transfer gate ϕ_P is then opened and each of the charge samples is permitted to equilibrate with its respective previous samples. The ϕ_P gate is then closed. This isolates a portion of the averaged samples which can then be clocked out the shift register to an output amplifier. A photomicrograph of a 64-stage device with controllable α's of 1/64, 1/32, 1/16, 1/8, and 1/4 is shown in Figure 4.

DIGITAL AND CTD ACCUMULATOR SIGNAL IDENTIFIERS

The digital recursive filter portion of the signal identifier is depicted by the functional block diagram of Figure 5. Normally the received RF signal is synchronously demodulated to baseband in-phase (I) and quadrature (Q) channels. For purposes of simplicity, only a single recursive filter is shown; a duplicate would be required in the system to preserve both phase and amplitude information. The component parts consist of the following:

Analog-to-Digital Converter, 8 bits, 2 MHz

MOS Shift Register Memories, 8 x 64 words, 20 x 64 words

Subtractor, Scaler, Adder, Buffers

About 150 standard integrated circuits are required to accomplish the I and Q recursive filter function.

Operation is as follows: The output of the correlator (C_i) is A/D converted to an 8-bit, 2's complement number. This 8-bit number, C_i, becomes the input to the adaptive filter. Static MOS shift registers are used to store C_i and the 20-bit smoothed correlation function, R_i. These two binary numbers then become the previous correlator output sample, C_{i-1}, and the previous recursive filter output sample, R_{i-1}, after going through the 64-bit MOS shift registers. C_{i-1} and R_{i-1} are then sent to an algebraic summer which either adds R_{i-1} to C_{i-1} or subtracts R_{i-1} from C_{i-1}. Additions or subtractions of these two functions are controlled by the previously detected output. The 9-bit output from the algebraic summer represents the error between R_{i-1} and C_{i-1} which is then scaled and algebraically added back to R_{i-1} to form R_i. The error can be scaled from 1/2048 to unity in power of two increments. The six most significant bits (MSB) of R_i are then compared in magnitude to a threshold value. If the magnitude of the six MSBs of R_i exceed the threshold, they are gated through and used by the 8 x 6 bit multiplier to form the product C_iR_i where

$$R_i = R_{i-1} + K\left[C_{i-1} - R_{i-1}\right]$$

A functional block diagram of the signal identifier using the CTD accumulator is displayed in Figure 6. Note that in this case, both an I and Q channel are shown along with circuitry that in essence puts a Costas phase lock loop (ref 6) around each real detected signal. In this case, the recursive filter consists of four multiplexed 64-bit ACC-10 chips to allow the system to operate on 256 data points at a time. For comparison purposes with the previous approach, the equivalent digital portion would occupy the upper right-hand corner marked ACC-10 Recursive Filter plus the analog multiplier. This requires 4 ACC-10s for the I channel and 4 for the Q channel, to which must be added 32 overhead ICs. Even allowing for a growth in MOS memory chip capability, a four-to-one reduction in hardware has been accomplished.

Figure 7 displays a signal inundated in noise going into the accumulator and the smoothed output. This loop has some doppler correction capability by operating on the in-phase (I) and quadrature (Q) early and late correlator output signals. There are two identical channels, I and Q. In each channel, the sum of early and late is multiplied by the estimate of C $\cos\theta$ and C $\sin\theta$, respectively, from the recursive filter. The sum of the products is M.

$$M = 2C^2p\cos^2\theta + 2C^2p\sin^2\theta \qquad \text{or} \qquad M = 2C^2p$$

where

C = correlator peak level
p = modulation index
θ = IF phase

This signal is dependent only on the modulation index and not the carrier phase. As indicated, the recursive filter output is used to open a detection gate only when a signal is present, allowing clear communication.

CONCLUSION

It was found possible to process the output of Surface Charge Correlators in a post-processing signal identifier without resorting to a translation to the digital domain. This was accomplished by developing a new CTD smoothing filter that does not suffer from the cumulative inaccuracies caused by standard CTD recursive filter implementations. A further benefit was a fourfold hardware reduction for this function compared to a digital implementation in a previous system.

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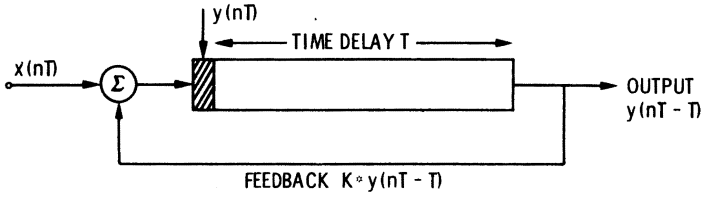
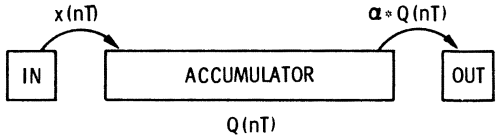


$$y(nT) = x(nT) + K * y(nT - T)$$

Fig. 1. Basic Recursive Filter



$$Q(nT) = Q(nT - T) - \alpha * Q(nT - T) + x(nT)$$

$$= (1 - \alpha) * Q(nT - T) + x(nT)$$

$$K = (1 - \alpha)$$

Fig. 2 Accumulator

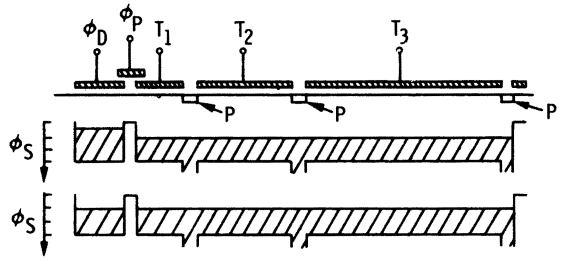


Fig. 3. Cross Section of One Stage of the Device Showing the Surface Potentials before and after Equilibration

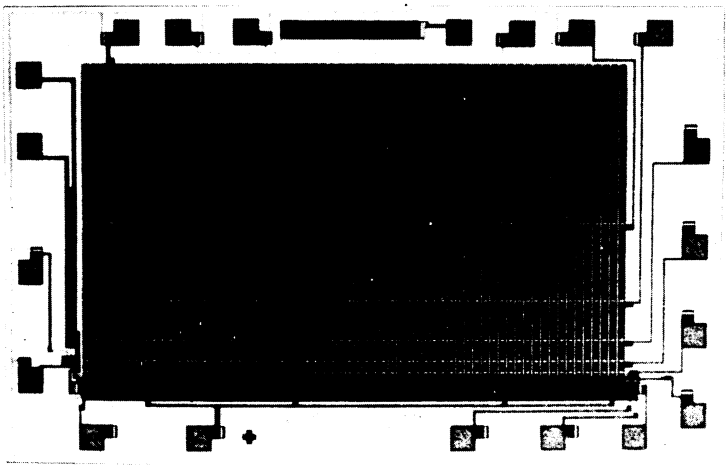


Fig. 4. Photomicrograph of 64-Stage Device

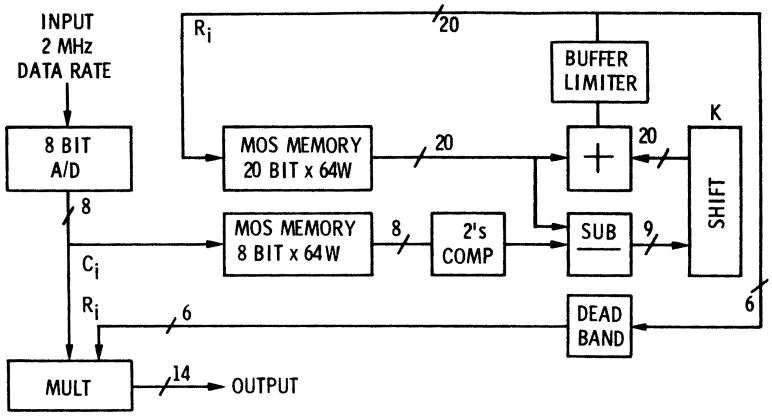


Fig. 5. Digital Recursive Filter

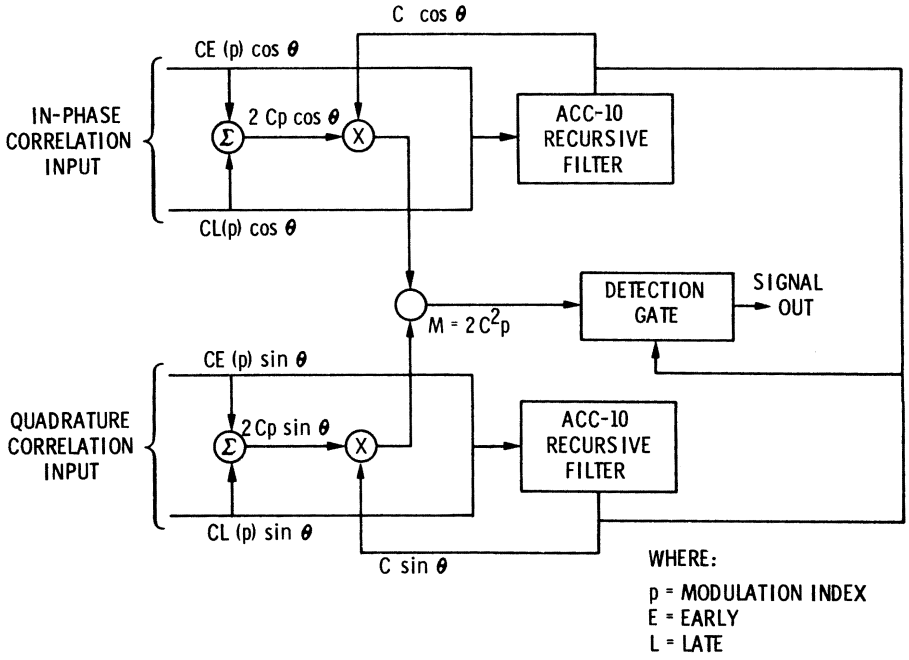
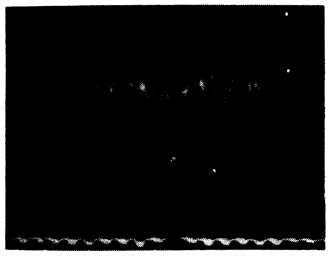


Fig. 6. Signal Identifier Simplifed Functional Diagram



ACC-10 INPUT
CORRELATED
SIGNAL INUNDATED
IN NOISE

ACC-10 OUTPUT
RECOVERED
SMOOTHED SIGNAL

Fig. 7. ACC-10 Accumulator Performance