ERRORS IN PROGRAMMABLE CCD TRANSVERSAL FILTERS AND CORRELATORS

D.J. MacLennan[†], J. Mavor[*], Y.T. Yeow[††]

ABSTRACT

Experience in the design and evaluation of CCD, transversal filters and correlators incorporating floating-gate reset (FGR) tapping circuits has indicated that the approach is limited to a greater or lesser extent by many factors; some associated with the CCD itself (transfer inefficiency and linearity, for example) and others related to the ancilliary MOS circuitry (involving V_T and gain variations). The CCD/MOST correlator comprises many non-CCD functions; including signal conditioning, signal summation, multiplication, and sample-and-hold. Errors associated with the linearity, dc offsets, noise, sensitivity and stability of these circuits must be understood before properly engineered correlators can be designed.

In this paper, imperfections in prototype, programmable, CCD filter design are reviewed by considering errors arising both in the CCD and peripheral circuitry. Practical correlation is presented in which the errors in FGR tapping circuitry were dependent on the geometry of the MOS transistors used in the design.

INTRODUCTION

Recently reported developments in CCD signal processing have included programmable transversal filters and correlators (refs. 1,2). The design work has involved the MOST implementation of the charge sensing, sample-and-hold, signal summation and multiplier circuitry. Whilst the feasibility of these programmable designs has been demonstrated, errors associated with the operation of the CCD and the related peripheral circuitry must be fully characterised and understood before properly engineered integrated circuits can be produced.

The error contributions can be separated according to their origins; some relating directly to the CCD, others resulting from variations in the ancilliary, MOST-based circuitry. The main causes of errors are:

(a) Linearity error in the CCD input signal to output voltage,

(b) transfer efficiency related errors in the CCD,

(c) tap sensing circuitry errors, and

(d) tap weighting errors.

Linearity problems have been treated elsewhere (refs. 3,4); feedback linearisation (ref. 4) being a particularly effective solution for programmable CCD filters. Other circuitry-based errors arise in

[*]Electrical Engineering Department, University of Edinburgh, Scotland.

[†]Now with GE Corporate Research and Development, Schenectady, U.S.A.

[††]Now with the Electrical Engineering Department, University of Singapore.

correlator implementation, where on-chip MOST multipliers are used.

In this paper, sources of error due to CCD peripheral circuitry are discussed; with no further discussion in areas (a) and (b) above, which have been treated (ref. 5) in the context of non-programmable CCD filters. Design guides relating to the minimisation of these errors are suggested, based on experience in the design and evaluation of CCD signal processing elements.

ERRORS ASSOCIATED WITH FGR TAPPING CIRCUITRY

All charge sensing amplifiers integrated with the CCD are to some extent non-linear in performance. The design of such amplifiers is aimed primarily at reducing their sensitivity to variations in the fabrication process and operating bias. The dynamic range of the amplifiers is designed preferably to be as small as possible to preserve linearity, consistent with adequate signal-to-noise ratio. Fig.1 shows the output voltage variation with signal charge for a typical FGR amplifier design (ref. 6). Note that with this particular design, odd and even taps had different sensitivities owing to poor layout design. Depending upon the acceptable level of linearity an operating range can usually be found. Where this is not achievable, the size (aspect ratio, Z/L) of the sense transistors has to be increased, with a resultant reduction in sensitivity and hence SNR.

A typical sense amplifier used to realise a multiple tap CCD is shown in Fig.2, based on a FGR design (ref. 7). It incorporates a sense (driver) MOST and an associated load MOST forming a source follower circuit. A reset transistor, operated periodically in the 'triode' low resistance region, is used to restore the floating gate potential to a 'no-signal charge' bias potential. This resetting procedure ensures that this potential is independent of the transistor threshold, V_T. However, the sensitivity of the circuit is to some extent dependent on operating conditions and the fabrication process, although care is taken in the design to minimise these contributions. C_g is formed by the input capacitance of the sense circuit, but is often, to a larger extent, dependent on the fixed, interconnection capacitance. In Fig.3 the normalised sensitivity of the FGR tap, dV_{sig}/dQ_{sig}, is plotted as a function of the signal charge, normalised to the maximum charge value, Q_{max}.

There are two basic errors associated with FGR tapping circuitry which are extremely important in the context of programmable transversal filters; errors in (a) tap gain, and in (b) the quiescent output potential. Errors in overall tap gain contribute to a degradation in filter performance. These errors may be visualised as being errors in the applied weighting coefficients and, for a transversal filter, may be evaluated using the equation (ref. 7)

$$v_o = V_{ref} - \sum_{k=1}^{N} \{v_k(G_k + \Delta G_k)\}\, G_f^{-1} \qquad (1)$$

where ΔG_k is the error in the overall gain of the k^{th} tap expressed in terms of conductance:

$$\Delta G_k = \frac{\Delta A_k}{A_k} \times G_k \qquad (2)$$

where A_k and ΔA_k are the gain and error in gain of the k^{th} tap respectively. By obtaining values for ΔA_k the performance of the filters may be further evaluated.

In the CCD implementation of a transversal filter, using FGR sensing structures (see Fig.4), the output of each tap may be considered as being superimposed on a direct voltage pedestal. Since in general the device operates at baseband, this may not be removed by a.c. coupling. Consequently, the output of the transversal filter will appear on a direct voltage pedestal V_{ref}; this may be removed should it remain constant. The operational amplifier is connected in a current-summing configuration with the reference voltage V_{ref} applied to the non-inverting terminal set equal to the voltage at the sense amplifier output for the equivalent of zero signal charge in the tap well. Its output is given by

$$v_o = - \sum_{k=1}^{N} v_k \, (G_k/G_f) \qquad (3)$$

where v_k and G_k are the signal voltage and weighting conductance at the k^{th} tap respectively.

When a temporally constant error in the quiescent output voltage of each tap ΔV_k, in addition to the constant voltage pedestal, is considered, then equation 3 may be written

$$v_o = - \sum_{k=1}^{n} v_k \, (G_k/G_f) - \sum_{k=1}^{n} \Delta V_k \, (G_k/G_f) \qquad (4)$$

Now when each of the G_k is assumed constant, the last term of equation 4 appears as an additional offset and may be removed subsequently in the same manner as the reference voltage. However, where temporally variable weighting coefficients are required, as for example in the correlator discussed in section 3, then the offset will vary with time and the error in quiescent output voltage must be minimised to achieve optimum dynamic range. Such errors may be attributed to several factors:

(a) charge loss or gain during transfer due to recombination or thermal generation,

(b) tap sensitivity variations,

(c) variations in tap reset potential, and

(d) threshold and gain variations in the sense amplifier circuit.

Of these contributions, the first and last tend to dominate in a well designed circuit.

The MOST source follower circuit is frequently used in FGR sensing designs (ref. 1) (Fig.2), and in order to investigate its sensitivity of output voltage to variations in the circuit topology and the CCD/MOS process, an MOS circuit analysis programme has been used. Errors can be introduced into the geometry of the MOST's used in the source followers (Z/L variations) due to (a) sideways diffusion of the MOST junctions, and (b) misalignment in masking in the fabrication of the devices. A process dependent factor is the variation in the threshold voltage of the MOST's; this will vary over the area of a silicon slice. Fig.5 shows the theoretical variation of the d.c. output voltage with the sense circuit a.c. gain for a source follower circuit which has been designed for a tapped, CCD delay line. Line 1 is obtained when error is introduced into the dimensions of the two transistors (see inset on Fig.6). $\Delta L > 0$ indicates a reduction in the source-to-drain spacing, L, $\Delta L < 0$ an increase

Line 2 is obtained by changing the threshold voltage, V_T, of the MOST's. Although in this analysis the effects of the variation in ΔL and V_T were assumed to affect the driver and load MOST's equally, in practice ΔL will not be the same for both the Z and L dimensions of each transistor; nor will the ΔV_T be necessarily the same for each device. Fig.5, however, indicates the typical magnitude of both these effects. Note that an extremely large variation in V_T is plotted in line 2.

Figure 6 shows experimental data for the a.c. circuit gain and d.c. output voltage of source follower circuits, as in Fig.5, measured on a 32-bit n-channel tapped CCD. 'Gain' is defined for experimental convenience as the difference in the output voltage for V_{in} = 7 V and 8 V. There is a clear correlation between these two circuit parameters. The best curve fit that can be achieved is obtained by assuming that the error spread is due, predominantly, to ΔL variations. This is partially confirmed by noting the fact that V_T values measured on the transistors of all the 32 taps, indicate an almost constant threshold of -1.95 V. Fig.5 shows that the V_T spread must be many hundreds of millivolts to account for observed variations in gain and quiescent voltage, and thus confirms this conclusion. Consequently, for low random errors in quiescent output voltage, as large as possible a source-to-drain spacing should be used; and great care taken during the fabrication schedule to ensure uniform diode diffusion and accurate masking alignment.

ERRORS ASSOCIATED WITH CCD CORRELATORS

A block diagram of a CCD, programmable transversal filter, or correlator, is shown in Fig.6. The reference channel is used as a means of storing electronically-variable weighting coefficients. The multiplier circuits are used to perform individual product terms, and can be implemented in MOS technology, monolithically with the CCD (ref. 1). The block diagram for one bit of such a correlator is illustrated in Fig.7.

The basic four-quadrant, linear multiplier used in an experimental correlator is implemented using two MOST's and a current differencing circuit shown in Fig.8. There are clearly certain restrictions that may be placed on the design of such a multiplier circuit, with respect to peak voltages applied to the terminals. These may be summarised by stating that the peak signal applied across the drain-source must be limited to a value such that neither of the transistors are driven into saturation with a peak signal applied to their gates. In addition, thetransistor gain, β, must be minimised to reduce the effects of the parasitic resistances associated with the driving source and diode diffusions; the dominant contributors to non-linearities in the circuit. This is illustrated in Fig.9, where both theoretical and measured results are given for a discrete multiplier circuit. The measured and theoretical results obtained for the circuit with the X input varying between $\pm$ 1 V are in effect identical to those shown and have been omitted for clarity. The source and drain diffusions for the transistors were measured to have a resistance of 300 Ω and this value was used in the theoretical analysis. Clearly, these resistance values contribute greatly to the circuit non-linearity and their effect should be minimised by the use of low gain transistors. Accuracies of the order of 1% may then be predicted for the circuit, with careful design, ignoring the effects of small gain and threshold variations in the transistors. The effect of threshold variations when using a number of multipliers could be eliminated by having independent control over each of the quiescent reference voltages, V_{ref}, but this would defeat the purpose of the integrated multiplier; a

single connection being required to provide all multipliers with this reference. Consequently, threshold variations will appear directly as a random error in the weighting coefficient, V_X, of the transversal filter with an associated reduction in accuracy. The variations in transistor gain results in an effective error in the reference signal, V_X, but this may be minimised by ensuring a long, wide-channel transistor is used, thereby minimising the effects of small variations in sideways diffusion, oxide thickness and substrate doping. The minimisation of these terms also assists greatly in minimising threshold variations and it is expected that errors in transistor gain of the order of 1% or less may be achieved on a CCD process.

The effective error at the multiplier, may be estimated by referring all offsets and gain errors to the floating gate, and evaluating the resultant product, noting that the fluctuations are random. This product may be written (ref. 1):

$$\Delta I \alpha (v_s + v_s \delta A + \Delta V_s/A_s)(v_r + v_r \delta A + \Delta V_s/A_s + \delta A[v_r + v_r \delta A + \Delta V_s/A_s] + [\Delta V_m + \Delta V_i]/A_s A_i) \quad (5)$$

where ΔI is the resultant multiplier current difference, v_s is the signal voltage, v_r the reference voltage, δA the fractional gain error (assumed to be the same for both the inverter and source follower circuits, ΔV_s and ΔV_i are the quiescent output voltage errors for the source follower and inverter circuits respectively, A_s and A_i are the source follower and inverter gains respectively, and ΔV_m is the threshold variation between multiplier transistor pairs. The fractional gain errors for the circuits may be expected to be on the order of 1% for a 13 μm source-to-drain spacing, from the previous measurements. The resultant quiescent output errors may then be computed as approximately 35 and 70 mV for the source follower and inverter circuits respectively; ignoring threshold variations, as they are believed to have a substantially smaller effect than the gain error on the quiescent output level. Equation 5 may now be evaluated to obtain the rms variation in tap outputs, and for maximum input voltages of 1 volt, a 3% error is obtained. This computation has ignored charge loss or gain in the CCD register due to thermal generation and transfer inefficiency. A linear variation in offset of ±10 mV is obtained from input to output due to inefficiency, unless compensation is applied. At the lowest clock rate of 1 kHz, thermal generation could result in a quiescent variation of ±5% between the input and output, assuming 10 nA/cm^2 dark current, unless compensated for. However, at clock frequencies in excess of 10 kHz, dark current effects become negligible.

CONCLUSIONS

The intention of this paper is to indicate some of the errors that occur in CCD programmable filter designs. However, because of the flexibility of circuit design, the relative magnitude, and thus the relative importance of the errors produced, will depend on the particular design and layout, and the CCD process used. Thus it is imperative, before design work commences, that the exact integrated circuit specification is produced and an error analysis undertaken with respect to possible circuit and process variations.

In programmable structures, based on monolithic linear multipliers, the main problems arise in the multiplier circuitry and the associated peripheral circuitry. Tapped, analogue CCD registers can now be designed and fabricated that have adequate characteristics for many signal processing requirements. This is particularly true when feedback linearisation of FGR tapped CCD delay lines is incorporated.

ACKNOWLEDGEMENTS

The authors wish to acknowledge the support of DCVD, (MOD) the SRC and MESL Limited, Scotland, for sponsoring this work.

REFERENCES

1. J.G. Harp, G.F. Vanstone, D.J. MacLennan and J. Mavor. "Analogue Correlators using Charge-Coupled Devices". Proc. CCD-75, Int. Conf. on the Appl. of CCD's, San Diego, CA, 29-31 October, 1975.

2. E.P. Herrman, D.A. Gandolfo, A. Boornard and D.B. Stepps. "CCD Programmable Correlator". Proc. CCD-76, (this Conference).

3. M.F. Tompsett. "Surface Potential Equilibration Method of Setting Charge in Charge-Coupled Devices". IEEE Trans. on Electron Devices, ED-22, June 1975.

4. D.J. MacLennan and J. Mavor. "Novel Technique for the Linearisation of Charge-Coupled Devices". Elect. Lett. 11, No.10, pp.222-223, (1975).

5. D.D. Buss, W.H. Bailey and A.F. Tasch, Jr. "Signal Processing Applications of Charge-Coupled Devices". Proc. CCD-74, Int. Conf. on Appl. of CCD's, Edinburgh, 25-27 September, 1974.

6. D.J. MacLennan, J. Mavor and G.F. Vanstone. "Technique for Realising Transversal Filters using Charge-Coupled Devices". Proc. IEE, Vol.122, No.6, June 1975, pp.615-619.

7. D.J. MacLennan. "Design and Operation of a Programmable Charge-Coupled Device Transversal Filter". Ph.D. Thesis, University of Edinburgh, 1st May 1976.

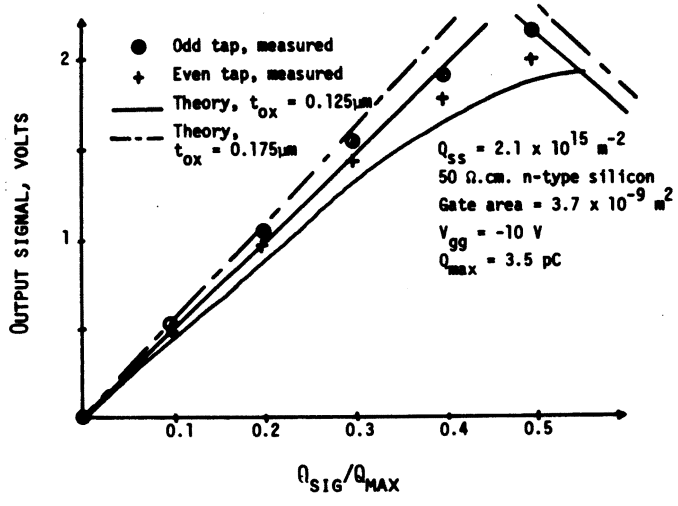

FIG.1. MEASURED AND THEORETICAL SENSITIVITY FOR THE FGR TAP

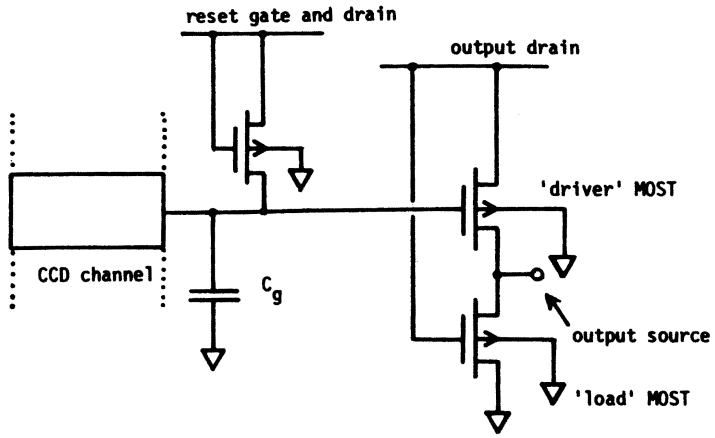

FIG.2. FGR TAP CIRCUIT

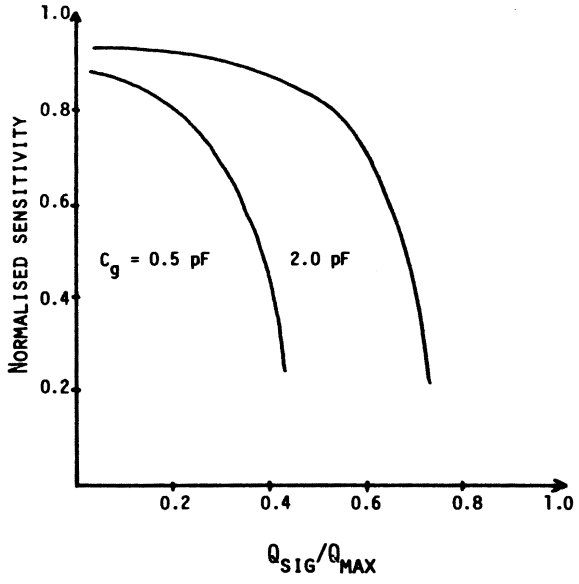

FIG.3. NORMALISED SENSITIVITY VARIATION WITH NORMALISED CHARGE FOR THE FLOATING GATE RESET STRUCTURE AND EXTERNAL GATE CAPACITANCE AS A VARIABLE.

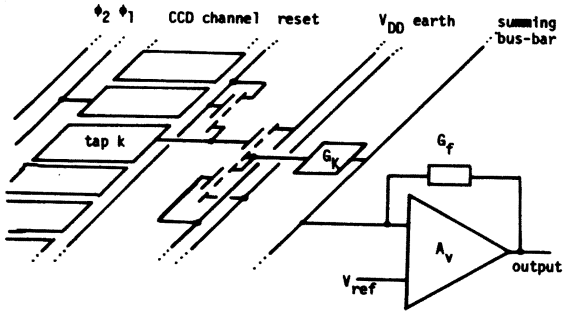

FIG.4. TAP SUMMING CIRCUITRY FOR A CCD TRANSVERSAL FILTER

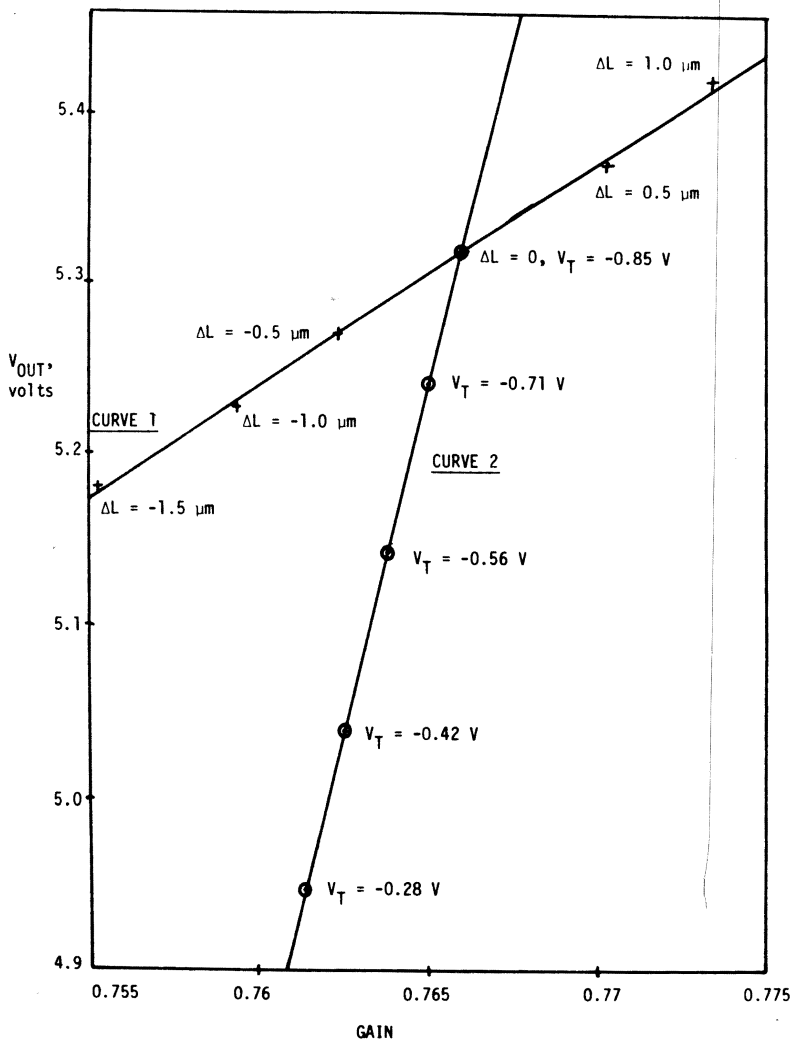

FIG.5. THEORETICAL VARIATION OF DC OUTPUT VOLTAGE AND AC GAIN WITH V_T AND SOURCE-TO-DRAIN SPACING ΔL.
CIRCUIT AND DEVICE CONDITIONS AS FIG.6.

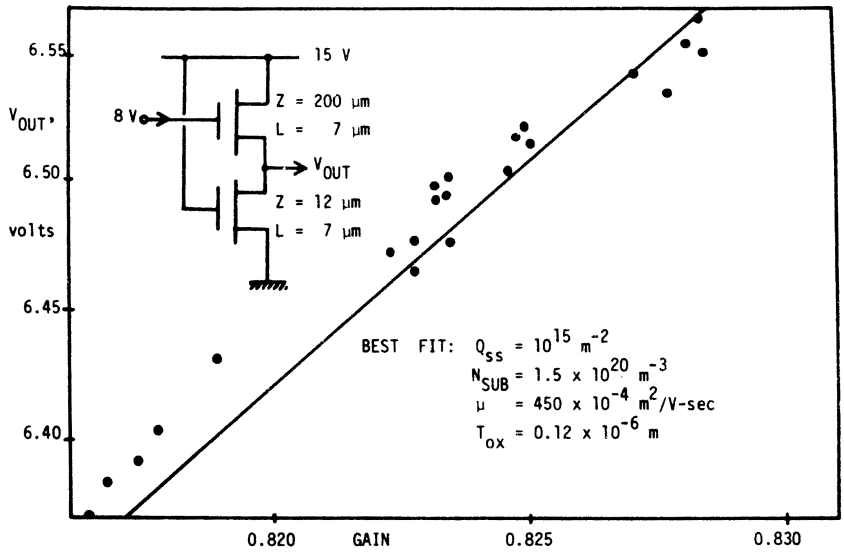

FIG.6. EXPERIMENTAL CORRELATION OF TAP OUTPUT VARIATION WITH OUTPUT CIRCUIT GAIN. (M55-2No.13)

DEVICE CONDITIONS: $Q_{ss} = 5 \times 10^{14}$ M^{-2}, N

$N_{SUB} = 5 \times 10^{20}$ M^{-3} (BORON),

$\mu = 720 \times 10^{-4}$ M^2/V-SEC,

$T_{ox} = 0.12 \times 10^{-6}$ M.

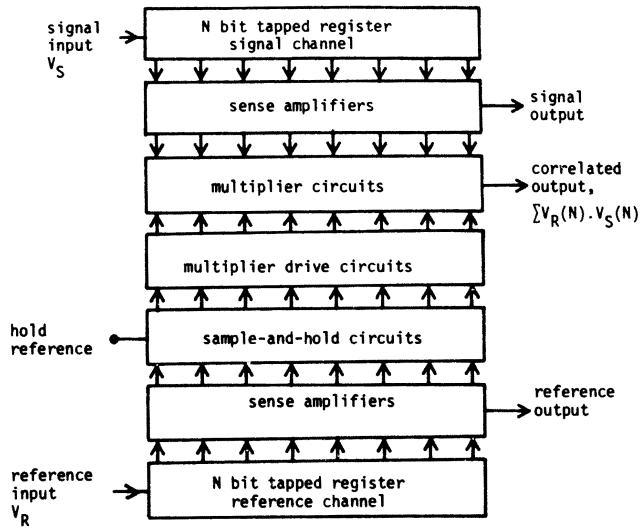

FIG.7. BLOCK DIAGRAM OF A CHARGE-COUPLED DEVICE, PROGRAMMABLE FILTER.

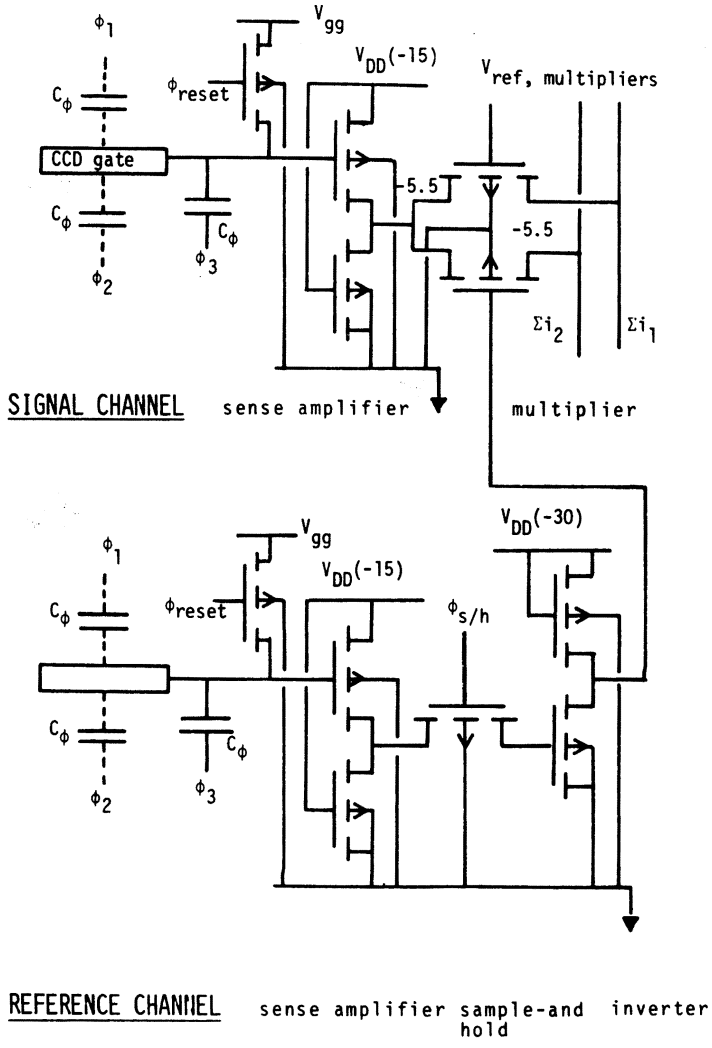

FIG.8. CIRCUIT DIAGRAM FOR ONE BIT OF A CCD PROGRAMMABLE TRANSVERSAL FILTER

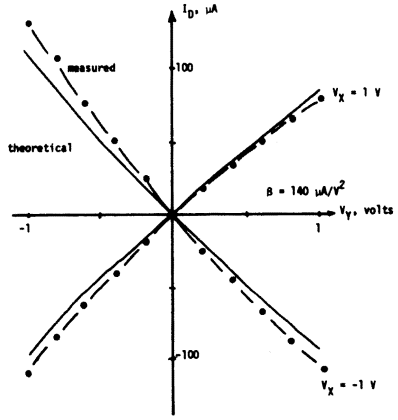

FIG.9. THEORETICAL AND MEASURED DISCRETE MULTIPLIER CHARACTERISTICS FOR 300 Ω SOURCE AND DRAIN PARASITIC RESISTANCES