CCD PROGRAMMABLE CORRELATOR

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ABSTRACT

Experiments with a 64 bit programmable correlator, for use in matched filtering of binary coded waveforms are described. The device consists of a 64 bit CCD tapped at every stage, a static memory for storing a binary code word and a serial input programming register. It is capable of loading a binary code while correlation is being performed with a previously loaded code. This device should find broad usage in radar and spread spectrum communications signal processors.

INTRODUCTION

The programmable correlator for binary codes is an extremely useful device. General classes of applications are: (1) pulse compression in radar systems, (2) synchronization and identification in many-user, spread-spectrum communications systems and (3) data encoding and decoding in spread spectrum systems. In radar systems, a programmable correlator with the capability of changing codes offers anti-jam protection along with the usual advantage of pulse compression, i.e., long range (associated with long pulses) combined with good range resolution (usually associated with short, broadband pulses). In spread spectrum communications systems, it is frequently necessary to synchronize a receiver to a transmitter by means of a code of modest length - up to about 1024 bits - before information can be obtained from a very long, possibly secure, code. In a system with many transmitters and receivers, correlation techniques may be necessary to identify the various users. A programmable correlator will enable a single receiver to recognize and identify many transmitters. Finally, spread spectrum communications, in which data bits are further encoded by means of broadband sequences, may require a correlation receiver capable of changing codes at the data rate in order to achieve greater protection against jamming.

The CCD offers an attractive approach to implementation of the programmable correlator. First, it is capable of operating directly on the analog waveform, thus eliminating the need for analog-to-digital conversion and multiple correlators. Usually, linear signal processing requires an A/D converter (of at least three bits plus sign) in order to quantize a signal with sufficient precision. A correlator is then required for each bit stream (three correlators in the case of the three-bit A/D converter). Systems analyses have shown that linear signal processing may offer about a 3 dB improvement (depending upon code length and other parameters of the specific system) over non-linear (hard clipped or one-bit) signal processing. This 3 dB improvement, translated into a factor of 2 reduction in transmitter power, may be considerable in many systems. The second advantage of the CCD tapped delay line is the

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very small size of an individual tapped stage which permits a very high effective device density. Timing logic and clock drivers may be placed on the same chip as the CCD tapped delay line so that an entire correlator may be realized on a single LSI circuit. The inherently smaller size of the CCD combined with the capability of dealing directly with analog waveforms may lead to an order of magnitude reduction in parts count over other LSI circuit correlators.

DEVICE ARCHITECTURE AND LAYOUT

The device to be described is a high density array with CCD stages and programming logic on 0.036 mm (1.4 mil) centers. The overall chip dimensions are 3.15 mm (124 mils) by 3.35 mm (132 mils). The elements of the chip are shown in the photomicrograph of Fig. 1 and the functions are described below.

(1) The 64 stage CCD tapped delay line (with a tap at each stage) permits non-destructive sensing of the coded waveform. A CCD input structure, consisting of three gates and a source diffusion may be used to input the signal with any of the low-noise techniques in the literature. The signal is sensed by means of a floating gate tap (Fig. 2) at each stage. The sensing elements are clocked electrodes, capacitively coupled to the phase-2 clock line.

(2) The sensing electrodes extend beyond the CCD channel and form the gate of the tap buffer FETs which convert the charge or voltage signals into current signals.

(3) The tap switches, of which there are two for each CCD stage, direct the current signal to either a "one" (+) or a "zero" (-) summing bus, under the control of the reference code.

(4) The static memory is a set of flip-flops which stores the reference code and controls the state of the tap switches.

(5) The isolation switches isolate the static memory from the reference code input register so that the TDL may correlate the incoming signal against the stored reference even while a new reference code is being admitted to the device.

(6) The buffer amplifiers provide sufficient drive to set the flip-flops in the static memory.

(7) The reference code input, a serial-in/parallel-out register, continuously admits a data stream which may serve as a reference code. Upon command, the data in the reference code input register are parallel-transferred through the buffer amplifiers and isolation switches into the static memory to control the setting of the tap switches.

The device was fabricated using a buried n-channel process. The non-CCD sections are NMOS so that a compensating P-type implant was required in these areas to ensure enhancement-type FETs.

DEVICE OPERATION

The CCD programmable correlator has been operated in the experimental setup shown in Fig. 3. A linear shift register generator (LSRG) is used to generate a 63-bit, maximal-length, pseudo-noise (PN) code. This PN code (with one bit added to equalize the numbers of "ones" and "zeroes") is first connected to the reference code input register. When the contents of this register are parallel-transferred to the static memory, the PN code becomes the stored reference code. After the code is stored in the static memory, the LSRG may be disconnected from the reference code input and connected to the CCD TDL input. When this is done, the PN code is correlated with a replica of itself which is the stored reference. The TDL outputs, i.e., the (+) and (-) sum lines must be connected to an off-chip differential amplifier. The photos in Fig. 3 show the waveforms observed in a typical experiment at 1 MHz. Photo A is the PN code generated by the LSRG. After this code has been stored in the device and used to set the tap switches, the impulse response of the TDL should be the identical code, inverted in time, and this is shown in Photo B. Having verified that the reference code was properly stored, one may connect the LSRG to the CCD input and observe the correlation signal. Photo C shows the serial output of the CCD with the PN code as input. Photo D shows the correlation signal observed at the TDL output. The correlation peak as well as the sidelobe structure is seen riding on a steady-state bias current. With some improvements in the differential amplifier circuit to reduce common-mode noise, the correlation signal of Fig. 4 may be observed. The peak-to-sidelobe ratio is very close to the theoretical value of 8:1 expected for this particular code. The CCD correlator has been operated with signals up to 5 megabits/sec (corresponding to a clock frequency of 5 MHz) with no deterioration in peak to sidelobe ratio. The fractional transfer loss is less than 10^{-4} per transfer for clock frequencies from 10 KHz to 10 MHz. Although the device has not been operated as a correlator above 5 megabits/sec because of limitations imposed by the code generator we expect it to perform satisfactorily up to at least 20 megabits/sec. The reference code input register has been operated at 5 MHz so that less than 20 μsec are required to load and store a new reference code. This means that the reference code can be changed at a 50 kilobit/sec data rate. Thus, the 16 kilobit/sec rate which is standard for digital voice communications can easily be accommodated. In radar pulse compression filter applications the code may need to be changed only at rates comparable to the pulse repetition frequency, roughly 1 KHz.

FUTURE WORK

Operation of the correlator at data rates up to at least 20 megabits/sec may be expected. Cascading of many devices to handle codes up to 1024 bits in length should be possible. Finally, a next-generation device may be expected to include: (1) on-chip clocks and drivers, (2) output circuits (differential amplifiers and buffers), and (3) a second CCD tapped delay line so that processing of in-phase and quadrature signals may be accomplished on a single chip. These improvements will further enhance the utility of CCD programmable correlators in radar and spread spectrum signal processors.

CONCLUSION

A CCD programmable correlator for PN codes up to 64 bits long has been developed. Autocorrelation with peak-to-sidelobe ratio of 8:1 (near the theoretical value for the code used) has been observed at input data rates up to 5 megabits/sec.

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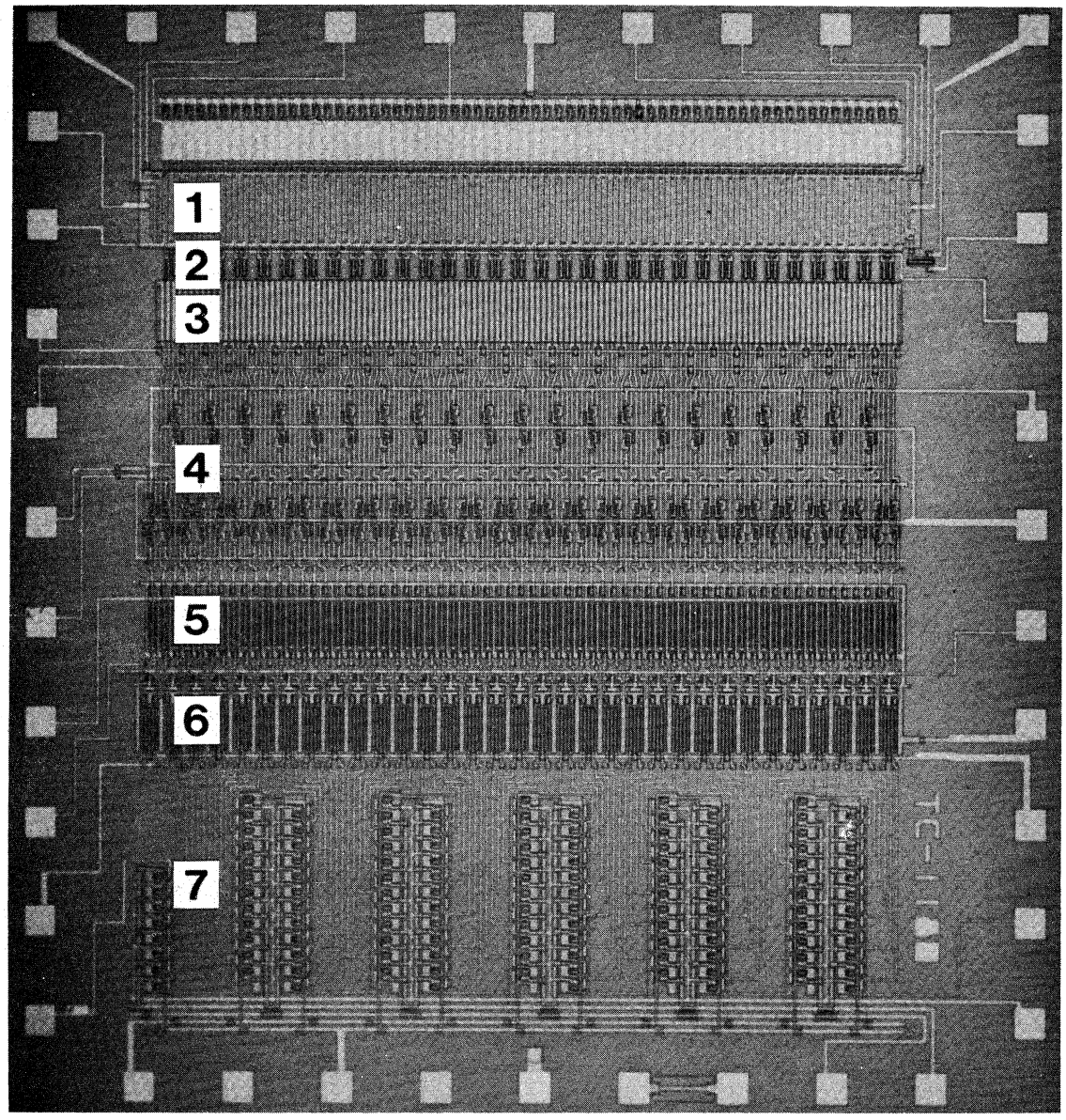

FIG. 1. PHOTOMICROGRAPH OF CCD PROGRAMMABLE CORRELATOR: (1) CCD TAPPED DELAY LINE, (2) TAP BUFFER FETs, (3) TAP SWITCHES, (4) STATIC MEMORY, (5) ISOLATION SWITCHES, (6) BUFFER AMPLIFIERS, (7) REFERENCE CODE INPUT REGISTER.

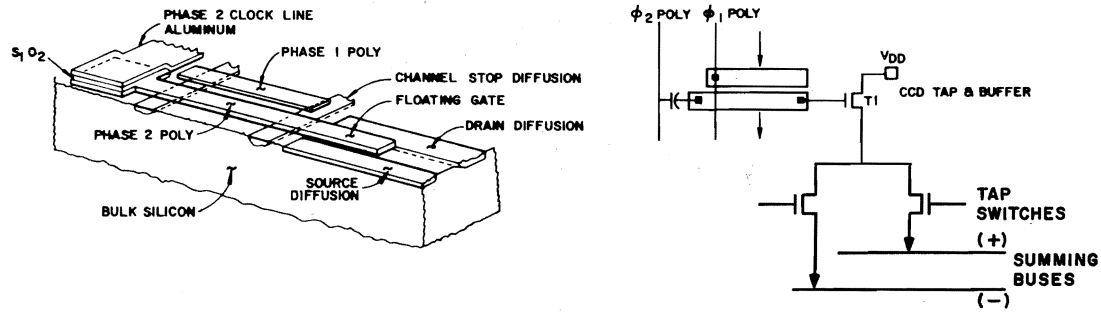

FIG. 2. FLOATING GATE TAP.

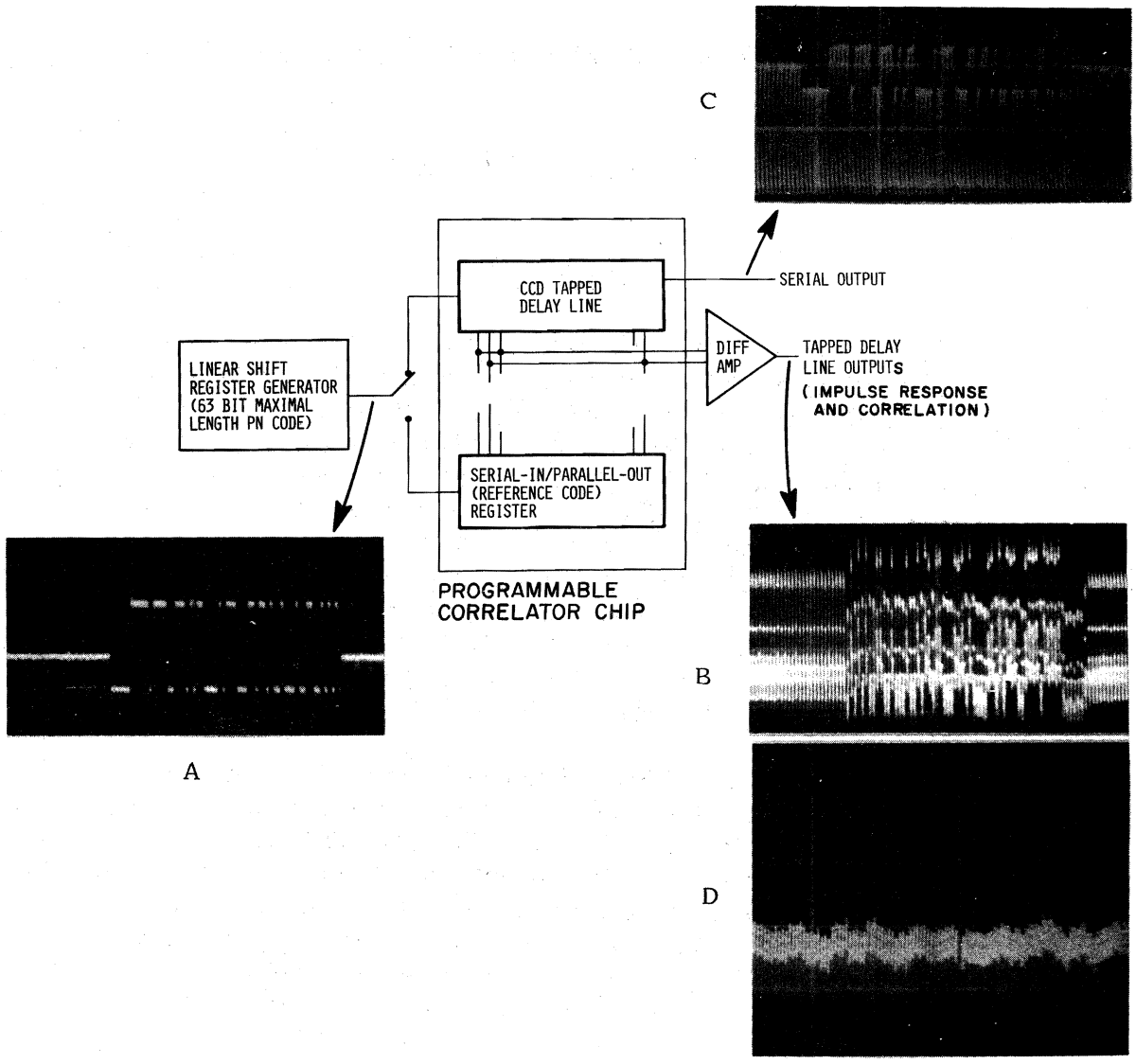

FIG. 3. EXPERIMENTAL SETUP AND WAVEFORMS OBSERVED.

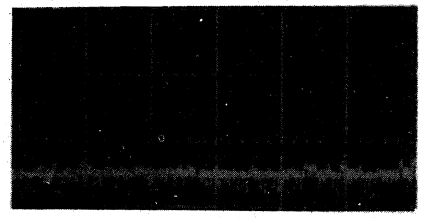

FIG. 4. CORRELATION SIGNAL OBSERVED WITH IMPROVED OUTPUT DIFFERENTIAL AMPLIFIER CIRCUIT.