FINITE FIELD ARITHMETIC WITH CHARGE TRANSFER DEVICES

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ABSTRACT

Charge transfer devices have been shown to have potential for implementing error correction coders and decoders for non-binary cyclic codes. A key element in such a coder/decoder is a unit to perform the finite field operations of addition and multiplication.

In this paper the properties of finite fields are exploited to develop an approach to implementing modulo-reduced addition and multiplication using charge transfer device delay lines. An arithmetic unit structure is evolved that is amenable to large-scale integration and programmability.

The requirements for the charge transfer devices needed in the arithmetic unit are described. Results of parametric studies of the delay line length and transfer loss versus finite field size are presented. The analysis shows that devices of modest capability can be used to implement the requirements. Test results from an experimental model of such a unit are discussed.

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FULL PAPER TO BE FOUND IN SECTION D

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