# CHARGE COUPLED DEVICE DIGITAL ARITHMETIC FUNCTIONS: EXPERIMENTAL RESULTS*

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## ABSTRACT

In this paper, the experimental characterization of larger scale digital CCD arithmetic functions is presented. Specifically, a digital adder that produces a 5-bit sum from two 4-bit words and a digital multiplier that produces a 6-bit product from two 3-bit words are discussed. The fundamental device design and theory of operation is shown and the design considerations are discussed that influence the layout of an array capable of doing n-bit arithmetic. The practical implementation of such a design is given and the experimental characterization of the multiplier and adder arrays is treated. The data shows how the devices perform as a function of temperature, frequency, and bias conditions. The compatibility of these devices with other existing digital technologies is evaluated; this is particularly significant from an applications standpoint in view of the fact that any real system will employ devices derived from a number of technologies. Future developments are indicated.

## INTRODUCTION

The basic concept of employing charge coupled devices (CCD's) in the digital domain has been explored in the past (refs. 1, 2). Some of the promising areas of application have been discussed (ref. 3) and some fundamental device work on a digital full adder circuit has been reported (ref. 2). The fundamental device design and theory of operation of digital CCD devices are shown and the design considerations are discussed that influence the layout of an array capable of doing n-bit arithmetic. The practical implementation of a two-word 4-bit adder and a two-word 3-bit multiplier array are discussed. Both of these arrays utilize a combimation of half and full-adder cells in a pipelining operation that achieves maximum operating speed.

## THREE-INPUT FULL-ADDER DESIGN

A full-adder logic cell has three inputs: a, b, and g, of which any one may have a binary value of 0 or 1. The logic cell adds the three bits together and generates a sum bit and a carry bit, each having a binary value of 0 or 1. Operation can best be described by referring to the schematic shown in Figure 1. In the design the charge storage buckets are the CCD channels under the polysilicon and are labeled in Figure 1 as D, M, C, etc. When the $\phi 1$ clock line goes to its negative value, the three input charges, a, b, g, transfer to the D storage area. Since the D charge storage area is identical in size to a, b, or g, it will fill completely if any

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one of the three inputs is at binary one. However, if two inputs are at binary one, it will overflow and also completely fill storage area C under the floating gate. The charge in the C storage area will cause a voltage change to occur on the master end of the floating gate. This voltage change is immediately transferred to the slave end, which in turn causes a change in the surface potential of the CCD channel beneath it, inhibiting the transfer of charges along the channel. When all three inputs are at binary one, then both the D and C storage areas spill over and the I storage area also fills completely.

For the first condition described, when only one input is at binary one, the charge stored in D is transferred into the H storage area, then under the slave end of the floating gate into M, and subsequently into S at the next $\emptyset 1$ negative transition and out as a binary 1 sum bit.

When two inputs are at binary one both the D and C storage areas fill, the charge in D again transfers into H, but now it is inhibited from passing under the floating gate. It is removed from the H storage cell before the next input bit appears by $\emptyset 4$ going negative and transferring the charge to the discharge diode; and the SUM bit is now an 0. Also at the $\emptyset 4$ negative edge, the charge stored in the C storage area is transferred out and becomes a binary 1 carry bit. For the final condition when all three inputs are at binary one and the D, C, and I storage buckets are full, the identical transfer conditions exist as when two inputs are at binary one; except that the charge in the I storage area transfers out at the $\emptyset 4$ negative transition. Thus both the sum and carry outputs have a binary 1 output.

Several clock lines are required for the full-adder cell, and in an attempt to keep the clock lines to a minimum number, it was decided to make the storage areas of C, D, M, I, S, K, N identical. For the layout reasons the standard area of these standard gates is 6.9 $mil^2$. In each of the logic cells described the aluminum gate is used for transfer and the polysilicon gate is used for storage. In general, an aluminum gate is connected to a polysilicon gate.

The design of the half-adder logic cell is very similar to the design of the full-adder, but since there are only two inputs (a, b) to a half-adder the need for the I storage cell disappears.

To perform binary multiplication it is necessary to use a 2-input AND gate. This function was mechanized by removing the floating gate and the N, M, and S storage areas from the half-adder design.

In order to obtain design, layout, and testing experience with CCD signal processing devices, a two-word 4-bit binary adder was included on the DP-1 chip. The addition of the two binary words $a_1$ - $a_4$, $b_1$ - $b_4$ is performed in a straightforward manner:

| | |
|---|---|
| Carry bit | $C_4\ C_3\ C_2$ |
| First word | $a_4\ a_3\ a_2\ a_1$ |
| Second word | $b_4\ b_3\ b_2\ b_1$ |
| Sum | $C_5 s_4\ s_3\ s_2\ s_1$ |

The least significant column has only 2 input bits so that a half-adder is satisfactory; however, the other three columns have three inputs and full-adders are required. A block diagram of the two-word 4-bit adder is shown in Figure 2 and the processed array is shown in Figure 5. It will be seen from the diagram that delay stages have been added to the

input signal paths of the most significant bits; this is to ensure that the input data arrive at the full-adder output synchronously with the carry bit. In order to compensate for the input delays applied to the most significant bits, it was also necessary to include corresponding delays to the sum output lines of the least significant output bits.

A two-word 3-bit multiplier array was also included on the chip as shown in Figure 6. The multiplier involves the use of an AND function besides half-adders and full-adders. The multiplication of the two 3-bit numbers $a_1 - a_3$, $b_1 - b_3$ is performed in the usual manner

$$
\begin{array}{cccccc}
 & & & a_3 & a_2 & a_1 \\
 & & & b_3 & b_2 & b_1 \\
\hline
 & & & a_3b_1 & a_2b_1 & a_1b_1 \\
 & & a_3b_2 & a_2b_2 & a_1b_2 & \\
 & a_3b_3 & a_2b_3 & a_1b_3 & & \\
\hline
P6 & P5 & P4 & P3 & P2 & P1
\end{array}
$$

The least significant column consists of an AND gate, the second least significant column requires two AND gates and a half-adder. The third column requires three AND gates; and a carry bit may also be received from the second least significant column and must be added to the three output bits from the AND gates. Thus, overall, the mechanization of that column used a full-adder and a half-adder as shown in the block diagram of the 3 x 3 multiplier (Figure 3). In the fourth column from the right, two AND gates are required; however, since a carry bit may be received from both the half-adder and full-adder of the lower column, again 4 bits must be added together. An identical combination of full-adder and half-adder were used to add the 4 bits. The second most significant column requires only an AND gate and full-adder, the carry output from the full-adder providing the most significant bit in the product. In order that the product bits were obtained in phase, it was necessary to add delay stages to the most significant input and least significant output columns.

## ARRAY FUNCTIONAL TESTING

### 4-Bit Adder Array

Testing was initially carried out at room temperature (25°C) and at a clock frequency of 10 kHz. The clock frequency was divided down by 16 to produce a 625 Hz word rate so that only one output word was displayed on the monitoring CRT at one time. By using this technique we could check that the phase correcting shift register stages had been inserted correctly since all output bits should be coincidental in time. The photograph of Figure 4 shows the 4 most significant bits of the output sum when input word-a is 1110 and input word-b is 1000.

All of the following tests were performed with bonded chips operating at a frequency of 11 kHz.

Output patterns for different input conditions were photographed at clock frequencies of 100 kHz and 175 kHz and the logic "1" output levels do not attenuate significantly as the frequency is increased; however, they become obscured as the logic "0" output levels (fat-zero) grow larger.

By switching the $b_3$ input and observing the output patterns on the oscilloscope, it can be seen that the adder array is performing the correct arithmetic functions up to just beyond 200 kHz, but with a deteriorated signal-to-noise level.

The operating temperature range was determined by functional testing in a temperature controlled chamber. The clock voltages were adjusted at a frequency of 11 kHz and at 25°C so that the 3 most significant output bits from the adder array were performing correctly for each input combination and with a maximum signal-to-noise ratio. The temperature was increased in 10° increments while the inputs were switched and the outputs monitored.

At 65°C the full-adder in the fourth channel ceased to switch, the $S_4$ sum-bit output remained at "0", and the $S_5$ carry-bit output remained at "1". The $S_3$ sum-bit output continued to function correctly.

At 110°C the fat-zero level of all outputs had increased so that no signals were discernible. It should be noted that the combination of high temperature and low frequency is the most difficult operating condition from the standpoint of thermal leakage. Indeed, proper operation at 125°C could be assured simply by operating the existing device at a frequency above about 500 kHz.

The temperature was then reduced to 25°C and all outputs resumed operating correctly. The temperature was then lowered in 10° steps, the inputs switched and again the 3 most significant output bits monitored.

At -15°C to -55°C the fat-zero level was reduced, but no further change in arithmetic performance. The temperature was then reduced to -65°C and the $C_2$ control line adjusted so that all channels performed correctly with a maximum signal-to-noise ratio.

## 3-Bit Multiplier Array

There are six parallel outputs from the multiplier, and 196 different output numbers, so that producing a meaningful photograph showing simultaneous outputs is quite difficult. For simple combinations where only four outputs are changing, the output pulses are similar to those shown for the adder-array. However, when all logic cells are operating and charges have to propagate through several full-adder, there is some deterioration of the charge and a difference in the amplitude of the most significant output bits can be observed. Nevertheless, correct operation for all input combinations was demonstrated.

## Characterization Summary

The circuit designs tested were produced to demonstrate the functionality of the arrays and consequently no effort was made to optimize the design. The relatively low operating frequency is a direct result of the maximum gate length used. The maximum length is much longer than required and future designs will be built for operation in the low megahertz range. It has already been mentioned that the relatively low test frequency (11 kHz) would be expected to impose a low maximum temperature. The low frequency allows more time for thermal carriers to accumulate and eventually cause an error in the output. Normally, the devices are expected to operate near 1 MHz and at this frequency even the existing design would operate correctly at temperatures exceeding +165°C. In future designs the total device area will be reduced and so the maximum operating temperature at 1 MHz would be even higher; viewed another way, at any given temperature the reduced area devices will allow operation at lower frequencies.

## INTERFACING THE CCD DEVICES TO TTL DRIVERS

It is very easy to interface CCD data processing devices to TTL logic gates; this was demonstrated by adding +10 volts to the substrate bias and all of the clock and control lines. The standard output swing of ground to 4.5 volts from the TTL gate is connected directly to an a, b, or g input gate on the full-adder or other CCD device.

## FUTURE EFFORTS

The encouraging results achieved on the multiplier and adder just described has prompted further work in the technology. It is now anticipated that a two-word 16-bit multiplier and a two-word 32-bit adder will be operational this year. The new designs incorporate some changes and use innovations that promise to produce devices with a much higher density and even more freedom from device characteristics.

## CONCLUSIONS

Although much of the technical interest in CCD's over the last few years has concentrated on analog capabilities, the application of CCD's to digital signal processing holds great promise. Not only shift register memories, such as the ones which have recently appeared on the market, but entire arithmetic functions can be implemented. High component density and low power consumption are the chief advantages of CCD's.

The realization of arithmetic functions by a sequence of logically controlled charge transfers results in a large propagation delay through the CCD circuit compared to conventional digital circuits; consequently, best speed is achieved by using pipeline operation. The significant speed improvement provided by pipelining (typically a factor from 10 to 50) makes CCD's best suited to applications which are inherently of a streaming nature.

## REFERENCES


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2. T.A. Zimmerman, "The Digital Approach to Charge Coupled Device Signal Processing," IEEE Advanced Solid State Components for Signal Processing; A Monograph of Papers Presented at the 1975 Circuits and Systems Symposium, April 1975, pp. 69-82.

3. C.S. Miller, T.A. Zimmerman, "The Application of Charge Coupled Devices to Digital Signal Processing," International Communications Conference, San Francisco, California, June 1975.

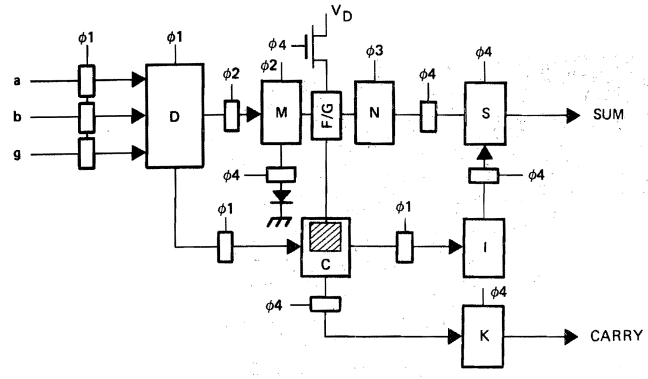


Figure 1. Full Adder

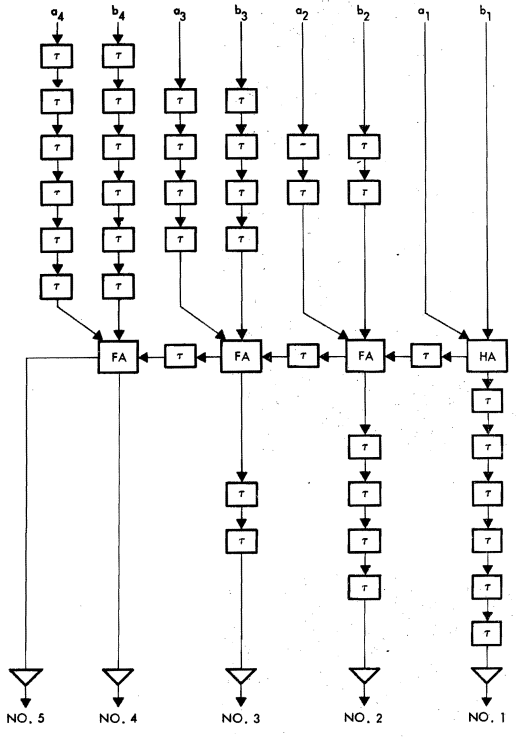


Figure 2. Two-Word Adder

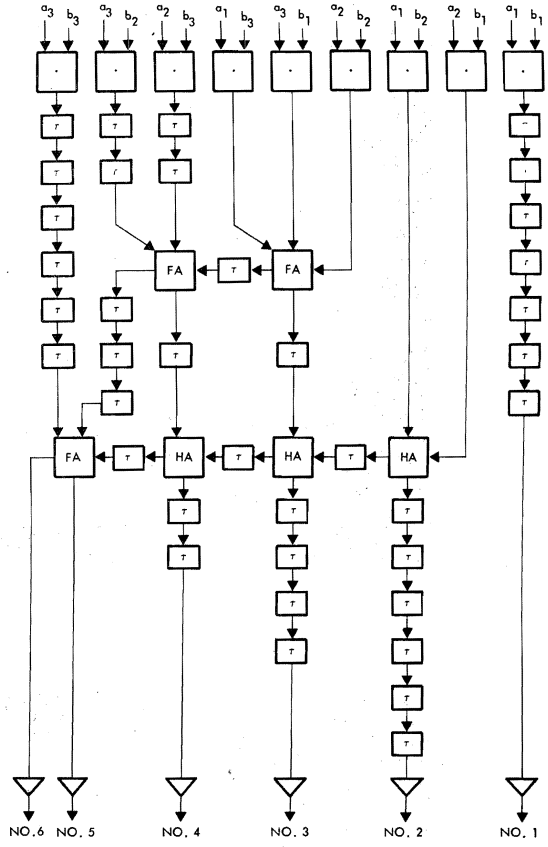


Figure 3. 3 x 3 Multiplier

[Not shown, $S_1 = 0$]

Output bit, $S_2 = 1$

Output bit, $S_3 = 1$

Output bit, $S_4 = 0$

Output bit, $S_5 = 1$

(Decimal 44)

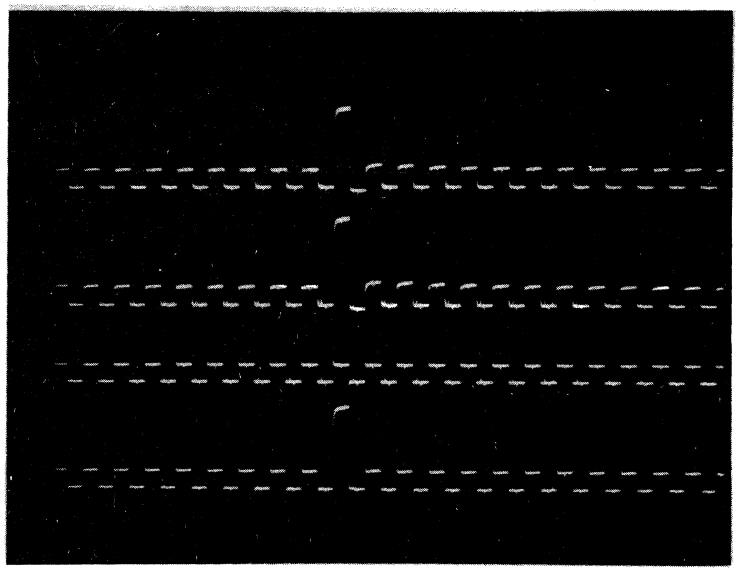

Figure 4. Test Results

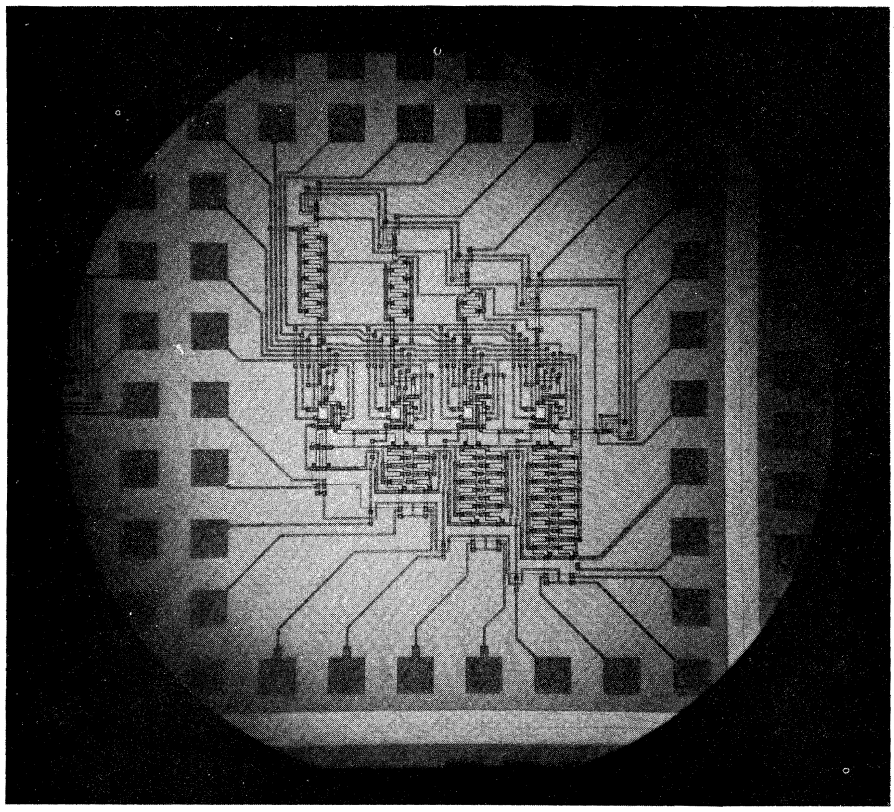

Figure 5. Two-Word 4-Bit CCD Adder Array

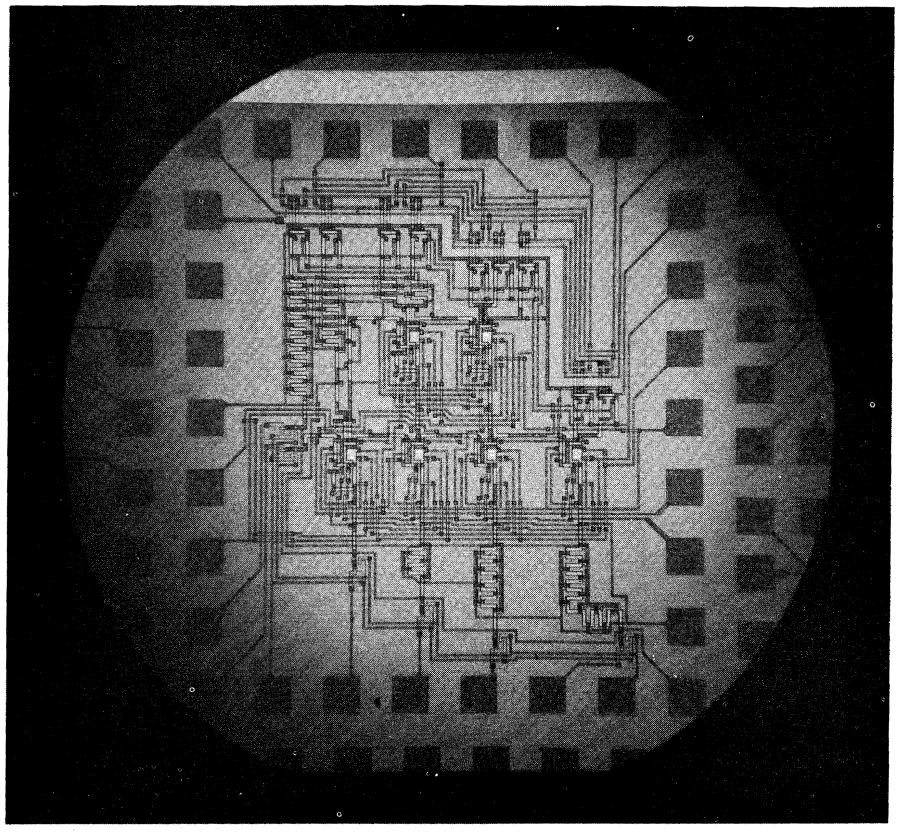

Figure 6. 3-Bit x 3-Bit CCD Multiplier Array