THE APPLICATION OF CHARGE COUPLING CONCEPTS TO MOS DYNAMIC RAM CELL DESIGN

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ABSTRACT

In recent years the basic CCD structure has evolved from the three- and four-phase designs to the uniphase structure. The MOS dynamic RAM cell has approached the same point in evolution with the advent of the charge-coupled RAM cell. The CC RAM cell consists of a single gate and may be structured in several different ways. These different structures are described and analyzed with regard to maximum charge capacity per unit area. A comparison of the cells with one another and with the one-transistor cell shows that the CC RAM cell with the implanted storage region (IS Cell) is the most attractive of the CC RAM cells. It will be shown that its charge capacity compares favorably (50-100 per cent) with that of the one-transistor and double-level poly-silicon cells for both conventional device parameters and high density conditions. In addition, the operation of the IS Cell is identical to that of the one-transistor and double-level poly-silicon cells.

INTRODUCTION

The evolution of the MOS dynamic RAM storage cell in recent years has proceeded in a direction which parallels the development of the basic CCD structure. This is not surprising as considerable effort has been devoted to decreasing the cell size of both structures, and many of the improvements realized in the CCD cell are applicable to the RAM cell. The CCD cell development has proceeded from the initial three- and four-phase designs to the higher density and simpler two-phase structure and finally to the uniphase structure. Similarly, the MOS dynamic RAM cell has progressed from the initial three- and four-transistor cells to the one-transistor cell and on to the double-level poly-silicon structure. More recently, a new charge coupled RAM cell has been reported (ref. 1,2) which brings the evolution of the MOS dynamic RAM cell to the same point as the uniphase CCD. The CC RAM cell combines the storage capacity and transfer gate of the one-transistor cell into a single gate. The resulting cell is simpler than the conventional one-transistor cell and possesses significant advantages in packing density and potentially higher yield.

In this paper various device structure approaches to the implementation of the CC RAM cell concept are described. The relative merits of these approaches are examined with regard to charge capacity, operating conditions and leakage current. The most attractive CC RAM structure is then compared with the conventional one-transistor and double-level poly-silicon cells for conventional device parameters and for very high density conditions.

CC RAM CELL STRUCTURES

The charge-coupled RAM cell concept has been described in detail (ref. 1,2), and it will be reviewed briefly before discussing the different structural approaches for implementing this concept. The operation of the CC RAM cell can be understood by referring to Figure 1, which shows the cross section of

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an N-channel CC RAM cell with an implanted storage region. The structure consists of a single gate which overlies two different regions. The storage region contains a shallow n-type ion implant (at or very near the SiO_2-Si interface) and a relatively deeper p-type ion implant, while the transfer region is free of implants. In the STORE mode the word line gate is off, but an isolated potential well exists in the storage region due to the n-type implant which shifts the flatband voltage to a negative value. When the word line gate is turned on (READ/WRITE mode), the surface potential in the transfer region is more positive than that in the storage region due to p-type implant which effectively increases the substrate doping in the storage region. The surface potential configurations for the STORE and READ/WRITE modes are also shown in Figure 1. The operation of this storage cell (voltages and timing) is identical to that of the one-transistor (ref. 3) and double-level poly-silicon cells (ref. 4,5).

The cell in Figure 1 is referred to as the implanted storage region (IS) structure and is one of four possible implementations of the CC RAM cell concept.

In order to provide better insight into the concept of the CC RAM cell and the various possible structures that may be used to implement this concept, it is useful to examine the relationship between the surface potential ϕ_s at the SiO_2-Si interface and the gate voltage V_G in dynamic operation.

$$\phi_s = V_o + (V_G - V_{FB} - V_{BB}) - \left[V_o^2 + 2V_o(V_G - V_{FB} - V_{BB})\right]^{\frac{1}{2}} \quad (1)$$

$$V_o = \frac{q\varepsilon_n N_A t_{ox}^2}{\varepsilon_{ox}^2}$$

where

V_{BB} = backgate bias voltage,

V_{FB} = flatband voltage,

ε_s = Permittivity of silicon,

N_A = Substrate doping,

t_{ox} = Gate oxide thickness,

ε_{ox} = Permittivity of oxide.

When V_o is small, as is the case for high resistivity material, ϕ_s varies linearly with $(V_G - V_{FB} - V_{BB})$. However, for either lower resistivity material or thicker gate oxide, the square root term in (1) becomes important and ϕ_s varies less than linearly with V_G. This effect may be realized in a given part of the device by altering the oxide thickness or by changing the local substrate doping by ion implantation. Further, the surface potential versus gate voltage characteristic may be translated along the gate voltage axis by altering V_{FB}. A small shift may be realized for a given Q_{SS} by altering t_{ox}. However, a more convenient method of shifting V_{FB} to a negative (positive) value is by implanting n-type (p-type) ions close to the Si-SiO_2 interface. (ref. 6,7)

With the above discussion in mind other structural approaches to the CC RAM cell concept are now described. The structure shown in Figure 2 is identical to the IS cell in Figure 1 except that a thick oxide has been

substituted for the p-type implant in the storage region. As mentioned earlier the thicker oxide has the same effect as an increased substrate doping in the storage region so that the thick oxide storage region (TS) cell operates exactly like the IS cell.

Another approach that may be used to realize a CC RAM cell has been described before (ref.2) and is shown in Figure 3. This cell which is referred to as the implanted transfer region (IT) cell has a single gate overlying a uniformly thick oxide. The storage region consists of the normal substrate material while the transfer region contains a relatively deep p-type implant to enhance the substrate doping. This implant causes the surface potential in the transfer region to vary sublinearly with gate voltage. The operation of this cell can be understood by referring to the surface potential configuration shown in Figure 3 (b) for the READ, WRITE and STORE modes. When the word line is turned on to write information into the cell, a potential well is formed under the storage region whereas a barrier exists in the transfer region. If the bit line is held more positive than the surface potential in the transfer region, no charge flows and a ZERO is written. If the bit line voltage is lowered below the surface potential in the transfer region, charge fills the well and a ONE is written. The word line voltage is then lowered to an intermediate level for the STORE mode to isolate the bit line from the storage region. To read the contents of the cell, the word line voltage is dropped to or near ground pushing the stored charge onto the bit line. The operation of this cell is a departure from that of the conventional one-transistor cell.

Yet another variation in cell structure which may be used to realize the CC RAM cell is shown in Figure 4. This structure is similar to the IT cell in Figure 3 except that the p-type implant is replaced by a thicker oxide in the transfer region. The thicker oxide results in a weaker dependence of ϕ_s on V_G in the transfer region, and it also produces a slightly larger negative flatband voltage shift due to the naturally occurring fixed positive charge (Q_{ss}) at the SiO_2-Si interface. The operation of the thick oxide transfer region (TT) cell is the same as that of the IT cell. However, note that in the READ mode the surface potential in the transfer region is actually more positive than that in the storage region, so that the stored charge is completely transfered to the bit line. This feature may, of course, be incorporated in the IT cell of Figure 3 at the expense of a slight threshold-shifting n-type implant in the transfer region.

Of the four different CC RAM cell structures described above, the question arises, "Which structure is most attractive for use in MOS dynamic RAMs and how does it compare with the conventional one-transistor or double-level poly-silicon storage cells?" A comparison of the relative merits of the four CC RAM cell structures must include factors such as charge capacity, operating conditions, and leakage current. Before a comparison of the cells is made, the charge capacity of each cell is analyzed and expressions for the maximum charge capacity per unit area are developed.

CHARGE CAPACITY ANALYSIS

A detailed charge capacity analysis has been performed for the CC RAM cell with an implanted storage region (IS cell).(ref. 8.9) Generalized expressions were developed which provide excellent agreement with experimental data. In addition, a simplified model was developed in reference 9 in order to provide clear insight to the dependence of charge capacity on device parameters such as implant doses and operating voltages. The results of this model agree well with the exact theory. The generalized equation of the exact theory will be reviewed below, and the simplified model will be expanded for application to all four of the CC RAM cell structures.

The subscript convention for the surface potential is illustrated in Figure 5 for the IS and TS cells where the first subscript (1 or 2) refers to the storage or transfer regions, respectively. The second subscript specifies the gate voltage level, and the third subscript denotes an empty (E) or full (F) well condition for the specified region. In normal RAM cell operation the bit line voltage V_{BL1} for writing a "1" into the cell is greater than the surface potential in the transfer region in the STORE mode (ϕ_{2SE}). This is necessary in order that the writing of a "1" (full well) into one cell does not destroy a "0" (empty well) in an adjacent cell along the same bit line. From Figure 5 it can be seen that the charge capacity is then equal to the quantity of mobile charge required to shift ϕ_1 from ϕ_{11E} to ϕ_{11F} where ϕ_{11E} and ϕ_{11F} are the empty- and full-well values of the surface potential when the gate voltage is at an intermediate level V_I. V_I is close to but not equal to V_S. It is the gate voltage at which $\phi_{2IE} = V_{BL1}$, and it occurs as V_G is switched from the READ/WRITE level V_{RW} to the store level V_S.

The generalized equation developed in Reference 9 may be applied to the IS cell to yield the following expression for the charge capacity

$$Q_{IS} = (\phi_{11E} - \phi_{11F})\, C_o + (Q_{BE} - Q_{BF}) \qquad (2)$$

where C_o is the oxide capacitance per unit area and Q_{BE} and Q_{BF} are the depletion space charges in the storage region for the empty- and full-well conditions, respectively. The simplified model shown in Figure 6 can then be applied to yield convenient analytical expressions for ϕ_1 and Q_B. In this model the positive space charge due to the n-type implant in the storage region (Q_t) is assumed to lie entirely at the SiO_2-Si interface. This is a very good approximation to the actual IS cell since the n-type implant is placed at or very near the interface. The simplified model also assumes separate substrate dopings N_{A1} and N_{A2} for the storage and transfer regions, respectively. These separate dopings reflect the p-type implants which are placed either in the storage region (IS cell) or the transfer region (IT cell) in order to increase the doping in these regions. The model approximates these implants with a uniform doping which allows the depletion approximation to be applied in obtaining simple expressions for ϕ and Q_B. In addition, the model in Figure 6 allows for different oxide thicknesses in the storage and transfer regions in order to include the TS and TT versions of the CC RAM cell.

For the case of the IS cell (Figure 1) t_{ox1} and t_{ox2} are equal and N_{A2} is the normal slice doping concentration. Application of this model to equation (2) yields the following expression for the maximum charge capacity per unit area.

$$Q_{IS} = C_o\sqrt{2}(\sqrt{V_{01}} - \sqrt{V_{02}})(\sqrt{\phi_{2RE}} - \sqrt{|V_{BB}|}) \qquad \text{(IS cell)} \qquad (3)$$

$$\phi_{2RE} = V' + V_{02} - \sqrt{(V' + V_{02})^2 - V'^2}$$

$$V' = V_{RW} - V_{FB} - V_{BB}$$

$$V_{oj} = \frac{qN_{Aj}\varepsilon_s}{C_o^2} \qquad j = 1 \text{ or } 2$$

where V_{RW} is the READ/WRITE gate voltage and ϕ_{2RE} is the empty-well surface potential in the transfer region in the READ/WRITE mode. Q_{IS} increases with increasing substrate doping and increasing Q_+ in the storage region. However, at the higher substrate doping there exists a boundary condition on Q_+ due to avalanching. That is, if N_{A1} and Q_+ are too large, the electric field

at the interface in the storage region becomes sufficient to result in avalanching. The avalanche boundary condition on Q_+ for a given substrate doping N_{A1} is given by (ref. 9)

$$Q_+ \leq (V_{BB} + V_{FB} - V_{RW})\, C_o + \varepsilon_s E_c \left(1 + \frac{C_o E_c}{2_q N_{A1}}\right) \tag{4}$$

where E_c is the critical field for avalanching (ref. 10). Thus the maximum charge capacity for the IS cell is given by equation (3) subject to the boundary condition in equation (4).

The model in Figure 6 may be applied to the CC RAM cell with the thick oxide storage region (TS cell) by setting $N_{A1} = N_{A2}$ and $t_{ox1} > t_{ox2}$. The shallow n-type implant is again represented by Q_+. Because the substrate doping is uniform in both regions of the TS cell, the model in Figure 6 is an accurate representation of this cell. The application of this model to equation (2) is straight forward and it yields the following results for the charge capacity per unit area of the TS cell.

$$Q_{TS} = C_o \sqrt{2V_o}\,(\sqrt{\phi_{2RE}} - \sqrt{|V_{BB}|})(1 - t_{ox2}/\, t_{ox1}) \quad \text{(TS cell)} \tag{5}$$

The boundary condition on Q_+ (equation 4) also applies at high substrate dopings. From equation (5) it can be seen that for a given substrate doping the charge capacity increases asymptotically with increasing oxide thickness in the storage region (t_{ox1}). The practical limit on t_{ox1} is taken to be one micron, a typical value for the field oxide in conventional MOS integrated circuits. This results in a charge capacity approximately 10 percent below the theoretical limit ($t_{ox1} \to \infty$).

By setting $N_{A2} > N_{A1}$, $t_{ox1} = t_{ox2}$, and $Q_+ = 0$, the simplified model in Figure 6 may also be applied to the CC RAM cell having an implanted transfer region (IT cell in Figure 3). To the extent that the implant schedules are tailored to provide a uniform doping in the transfer region, the model is an accurate description of the IT cell. In the description of this cell earlier in this paper, it was pointed out that the operation of this cell is different from that of the IS or TS cells. From Figure 3(b) it can be seen that for a given WRITE voltage V_W, and for $V_R \simeq 0V$, it is necessary to choose a STORE voltage V_S such that

$$\phi_{2WE} - \phi_{2SE} = \phi_{2SE} - \phi_{2RE} \geq V_n \tag{6}$$

where the voltage V_n represents a noise margin which may be set for a given operating condition. It is evident that equation (6) imposes a constraint on the maximum doping level N_{A2max} such that

$$V_W \geq \sqrt{2V_{02max}}\,(\sqrt{\phi_{2WE}} - \sqrt{\phi_{2RE}}) + 2V_n \tag{7}$$

where V_{02max} corresponds to N_{A2max}. It should be noted that N_{A2max} as determined from equation (7) may be greater than the maximum doping permitted by the avalanching boundary condition as applied to the N^+P junction formed by the boundary of the N^+ bit line and the implanted transfer region. In this case avalanching limits the maximum substrate doping in the transfer region. The STORE voltage which provides the noise margin consistent with equation (6) is given by

$$V_W - V_S \geq \sqrt{2V_{02max}}\,(\sqrt{\phi_{2WE}} - \sqrt{\phi_{2SE}}) + V_n. \tag{8}$$

Thus the charge capacity per unit area that results with the above mentioned

boundary conditions is then given by

$$Q_{IT} = \sqrt{2V_{01}}\ C_o\ (\sqrt{\phi_{2SE}} - \sqrt{\phi_{2RE}})\ (\sqrt{N_{A2}/N_{A1}} - 1) \quad \text{(IT cell)} \tag{9}$$

where ϕ_{2SE} and ϕ_{2RE} are obtained from equation (1) with $V_G = V_S$ and $V_G = V_R$, respectively.

As mentioned earlier, the CC RAM cell with the thick oxide transfer region (TT cell in Figure 4) operates exactly as the IT cell discussed above. The simplified model of Figure 6 is an accurate model of the TT cell since the substrate doping in the storage and transfer regions are equal and uniform. For this case $N_{A1} = N_{A2}$, $T_{ox2} > t_{ox1}$, and $Q_+ = 0$. The constraint on the cell parameters set by the noise margin condition of equation (6) applies. However, since the substrate doping is not enhanced in the transfer region, the avalanche condition does not apply at the boundary of the N^+ bit line and the transfer region. For a given WRITE voltage the maximum thickness of the oxide in the transfer region t_{ox2max} is restricted by equation (7) where V_{02max} now corresponds to t_{ox2max}. This maximum oxide thickness is also subject to the practical limit in actual device fabrication which as before we assume to be one micron. As in the case of the IT cell, the STORE voltage dictated by the noise margin requirements is given by equation (8), and the charge capacity which results for the CC RAM cell with the thick oxide transfer region is

$$Q_{TT} = \sqrt{2V_{01}}\ C_o(\sqrt{\phi_{2SE}} - \sqrt{\phi_{2RE}})(t_{ox2}/t_{ox1} - 1) \quad \text{(TT cell)} \tag{10}$$

COMPARISON OF CELLS

In the preceding section expressions were developed for the charge capacity of each of the four CC RAM cell structures. With these results the CC RAM cells can be compared with one another and with the conventional one-transistor and double-level poly-silicon cells with regard to maximum charge capacity, leakage current, and operating conditions. The comparison of maximum charge capacity per unit area is shown in Table I for conventional device parameters with two different backgate bias voltages and for very high density conditions. The data is normalized to the charge capacity of the one-transistor cell. The conventional parameters are listed as

t_{ox}	= 1000Å	V_{RW}	= 10v
N_A	= $10^{15}cm^{-3}$	V_{BB}	= -5v and -1v
V_{FB}	= -1v	V_n	= 1v
V_{DD}	= 12v		

The high density conditions are selected according to the results of Dennard et al. (ref. 11) and are also summarized below.

t_{ox}	350Å	V_{RW}	= 3v
N_A	$2.5 \times 10^{16}cm^{-3}$	V_{BB}	= -1v
V_{FB}	= -1v	V_n	= 0.5v
V_{DD}	= 5v		

From Table I it can be seen that the CC RAM cell with the implanted storage region (IS cell) provides the best charge capacity of the CC RAM cells, and its capacity ranges from 50 to 90 percent of the one-transistor cell for conventional device parameters. At the high density conditions the preceding statement applies except that the IS cell compares slightly more favorably with the one-transistor and double-level poly-silicon cells. The IT and TT cells have lower charge capacity primarily because of the noise margin requirements which result from the operation of these two cells. The TS cell capacity is quite low due to the fact that charge is stored beneath a thick oxide gate.

As mentioned in the description of the IT and TT cells in Figures 3 and 4, the operating conditions differ from those normally encountered in one-transistor cell operation. Three rather than two gate voltage levels are required on the word line. As a result of this requirement and the noise margin requirements on the bit line, the IT and TT cells are less attractive than the IS and TS cells. The appeal of the IS and TS cells is further enhanced by the fact that the IS and TS cell operation is identical to that of the one-transistor cell.

The IS cell possesses another attractive feature which also makes it more favorable than the other CC RAM cells. The storage region of the IS cell contains a p-type implant for the purpose of increasing the substrate doping in the storage region which results in a narrower depletion region. This should result in decreased leakage current provided that the p-type implant does not degrade the bulk lifetime or the higher electric field in the narrower depletion region does not lead to carrier multiplication. A decreased leakage current permits longer time between cell refresh, or higher operating temperatures.

From the discussion in this section it can be seen that the CC RAM cell with the implanted storage region (IS cell) is clearly the most attractive of the CC RAM cell structures in terms of maximum charge capacity, operating conditions and leakage current. Furthermore, the charge capacity of this cell compares favorably with that of the one-transistor and double-level poly-silicon cells for both conventional device parameters and high density conditions.

SUMMARY

In this paper various structural approaches to the implementation of the CC RAM cell concept have been described. The charge capacity of each structure was analyzed in order to allow a comparison of the cells with respect to maximum charge capacity as well as operating conditions and leakage current. The CC RAM cell with the implanted storage region (IS cell) was found to be the most attractive of the CC RAM cells, and its maximum charge capacity was found to range from 50-90 percent of that of the one-transistor and double-level poly-silicon cells for conventional device parameters. At high densities a similar but somewhat higher range was found to apply. Because of its structural simplicity, its operational compatibility with the one-transistor cell, and its potential for lower leakage current, the CC RAM cell is attractive for high density MOS RAMs.

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TABLE I

RAM CELL CHARGE CAPACITY COMPARISON*

Structure	Conventional Parameters		Very High Density
	V_{BB} = -5v	V_{BB} = -1v	
Implanted Storage (IS)	.55	.91	1.10
Thick Oxide Storage (TS)	.07	.10	.22
Implanted Transfer (IT)	.43	.45	.27
Thick Oxide Transfer (TT)	.45	.45	.24
One-Transistor or Double-Level Poly-Silicon	1.00	1.00	1.00

* Normalized to the charge capacity of the one-transistor cell.

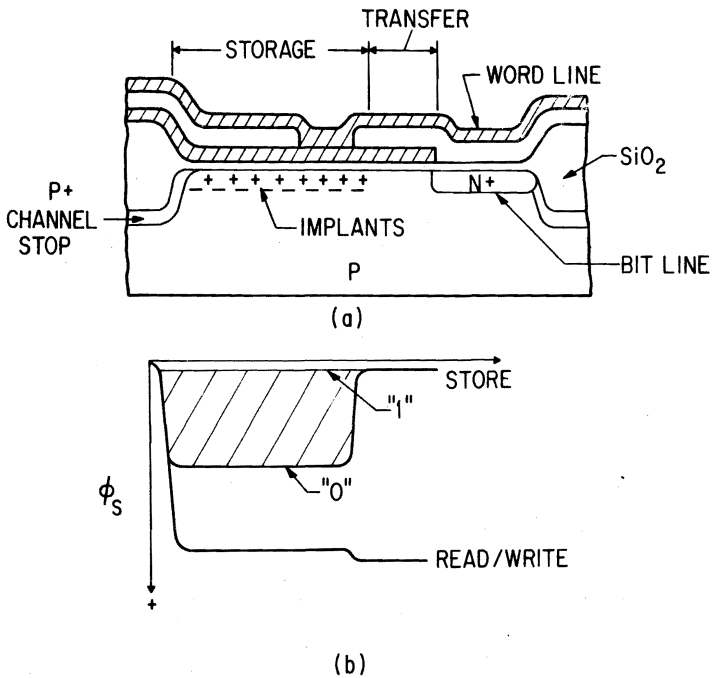


Figure 1. CC RAM cell with implanted storage region (IS cell). (a) Cross section of cell structure (N-channel case). (b) Surface potential configurations for READ, WRITE and STORE modes.

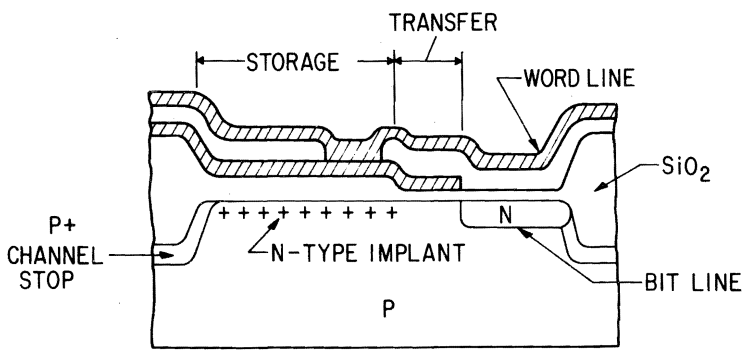


Figure 2. Cross section of CC RAM cell with thick oxide storage region (TS cell).

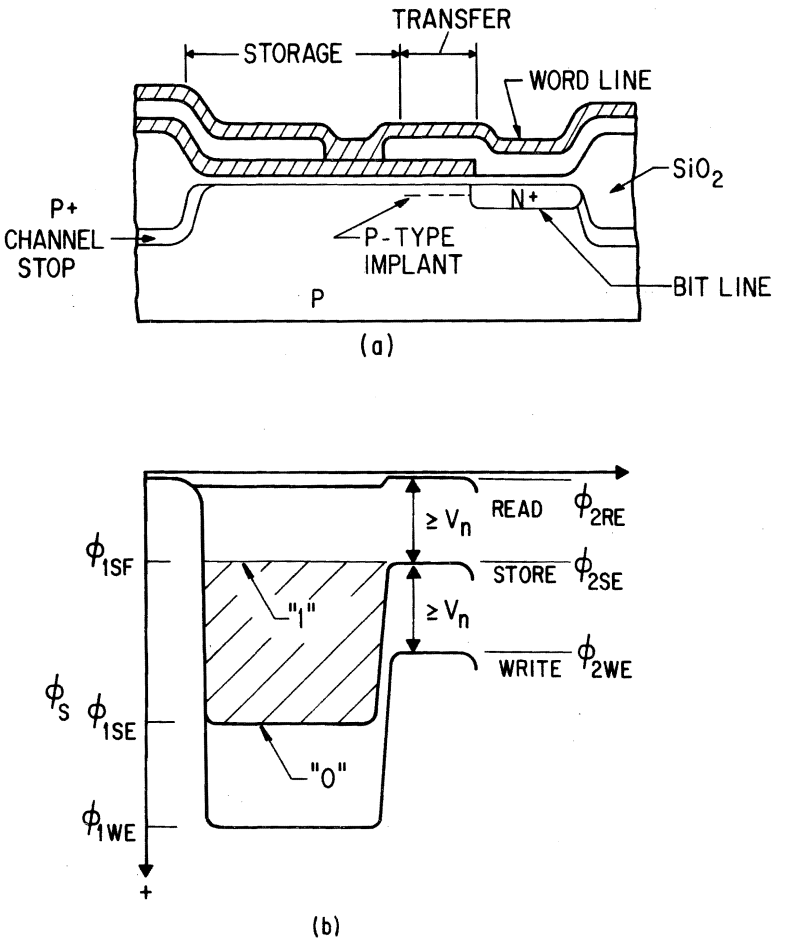
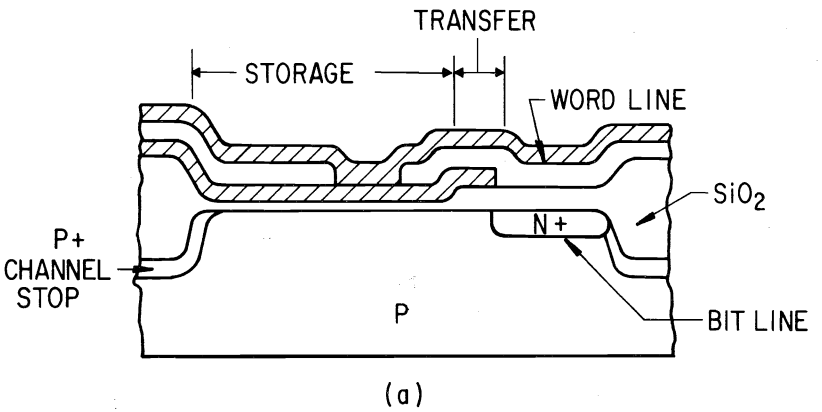


Figure 3. CC RAM cell with implanted transfer region (IT cell). (a) Cross section of cell structure. (b) Surface potential configurations for READ, WRITE and STORE modes.



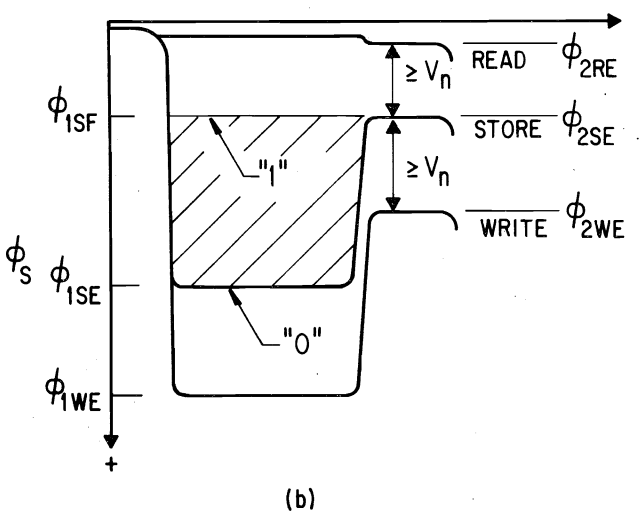


Figure 4. CC RAM cell with thick oxide transfer region (TT cell). (a) Cross section of cell structure. (b) Surface potential configurations for READ, WRITE and STORE modes.

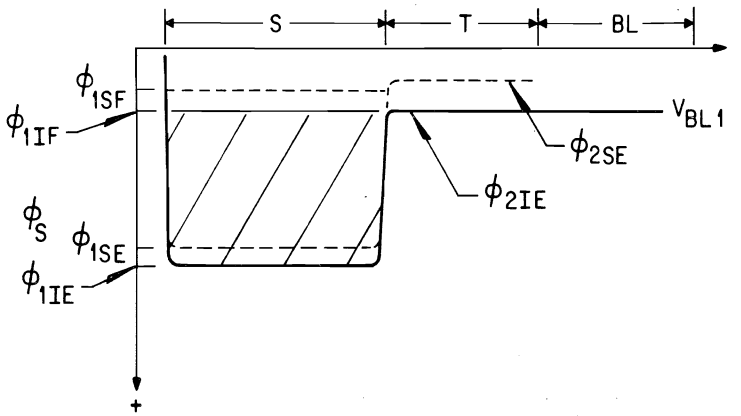


Figure 5. Illustration of subscript notation for the surface potential. Refer to the text for details.

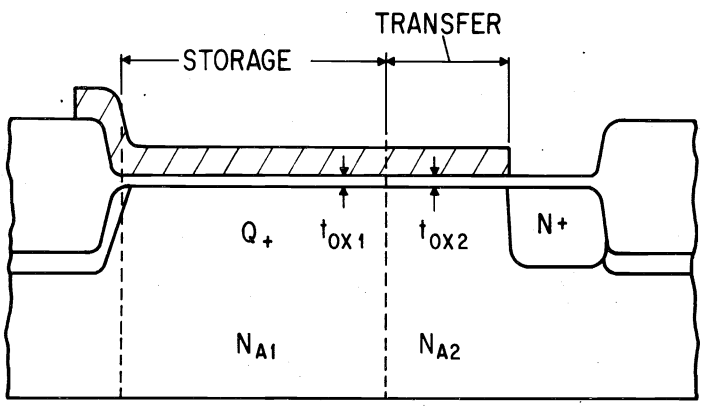


Figure 6. Cross section of the simplified model of the CC RAM cells in Figures 1-4.