OPTIMIZATION OF A SOLID STATE IMAGE SENSOR

Hsin Fu Tseng* and Gene P. Weckler*

ABSTRACT

The basic architecture of a solid state image sensor may be reduced to two basic functions, that of detecting photo-generated carriers and that of reading out information gained therein. The absorption of a photon by silicon results in the generation of an electron hole pair. Detection of this phenomenon requires the separation of the electron from the hole. This is normally accomplished by the depletion regions of either a diffused p-n junction or a field induced junction produced by applying the appropriate voltage to a field plate such as that formed by an MOS capacitor.

Having detected internally the absorption of a photon, it is necessary that this information be made available at terminal. Here lies a significant difference in the architecture of solid state image sensors.

In either case, the electron and hole are separated and the charge equivalent to one electron appears on the depletion region capacitance. Individual picture elements, or pixels, are either sequentially multiplexed to an output terminal by a digital shift register, or parallel transferred into an analog shift register and then clocked to an output terminal. Arguments will be developed that lead to the conclusion that the optimum architecture uses a diffused p-n junction as the picture element and an analog shift register to facilitate readout.

A matrix array using this architecture will be described. Its performance characteristics will be shown and compared to the performance obtained from other architectures.

INTRODUCTION

Evolution has produced several solid state image sensors, each possessing a different architecture. Most of these architectures can be broken down into combinations of four basic building blocks. This paper will present a review of the most common architectures and discuss in detail a new architecture which results in the optimal solid state image sensor.

The solid state image sensor takes advantage of the highly developed silicon integrated circuit technology. The mechanism of detection is based on the absorption by silicon of photons within an energy range of 1.1 ev to about 6 ev. This corresponds to a wavelength range of 0.2μ

* Reticon Corporation, Sunnyvale, California.

to 1.1μ as shown in Figure 1 by a typical spectral response curve. When a photon is absorbed, it generates an electron-hole pair. If we are to detect this electron-hole pair, the components must be separated. This is normally accomplished by the depletion region of a p-n junction or the depletion region induced by applying the appropriate voltage to an MOS capacitor. This is also referred to as a potential well. In either case, the electron and hole are separated and the charge equivalent to one electron will then appear on the depletion region capacitance. Let us briefly compare these two basic detection mechanisms. The internal quantum efficiencies can for all practical purposes be assumed to be the same for both mechanisms, i.e., the efficiency of collecting photo-generated electron-hole pairs. The main difference is in the external quantum efficiency of the two mechanisms. Figure 2 shows the basic structure of these two detectors. The external quantum efficiency of the diffused photodiode suffers minimum losses due to only two interfaces between materials of different refractive indices, i.e., Air-SiO_2 interface and SiO_2-Si interface. The thickness of the SiO_2 is such that the modulation of the spectral response of the diffused photodiode is negligible. It is apparent from Figure 2 that for the field induced detector an additional two interfaces are present to introduce losses. Furthermore, the transparent electrode is not really transparent since it is usually polysilicon. Since silicon is absorptive, some of the incident photons are absorbed in this layer. This is particularly true for the short wavelength or the blue end of the spectrum. The use of exotic metallic materials have resulted in field plates that are more transparent over the spectral range of interest than is polysilicon; however, these materials are foreign to standard integrated circuit technology.

The absorption of incident photons in this quasi-transparent layer can be reduced by making the layer thin. This, however, usually results in modulation of the spectral response due to interference patterns set up in the electrode layer and in the silicon dioxide layer between the electrode layer and the silicon since it too must be thin to insure reasonable operating voltages. Furthermore, the thickness of these films are subject to normal processing variations. It is, therefore, difficult to insure reproducability of sensitivity, uniformity, or spectral response. It is apparent that the diffused photodiode is a far superior detector, possessing the following advantanges: 1. external quantum efficiency approximately three times that of the quasi-transparent electrode employing polysilicon; 2. full spectral response extending from 0.2μ to 1.1 μ and; 3. a relatively smooth spectral response not subject to process variations.

Having now detected internally the absorption of a photon, it is necessary that this information be made available at a terminal. Here lies another of the principal differences in the design of solid state image sensors. Figure 3 shows schematically two approaches used to interrogate and read out the individual picture elements of an image sensor. Each approach uses a shift register to read out the information stored on each individual photosensitive element or pixel. In the first case a digital shift register is used to sequentially access a transfer switch

which connects individual pixels in turn to a common terminal. This approach has the definite advantage that digital shift registers and multiplex switches have been highly developed, use standard MOS processes, and are relatively easy to implement. The performance of this readout technique is dependent on both the total number of multiplex switches and on the uniformity of the multiplexing function, i.e., ideally each multiplex switch and its drive should be identical. Non-uniform multiplexing results in a fixed pattern modulation which is superimposed on the video information from the pixels. Differential signal processing techniques have recently been incorporated which have reduced the fixed pattern component to a negligible level. The fixed pattern has been reduced to the point where the total number of multiplex switches is now of practical significance. The random noise depends directly on the size of the output capacitance which in turn is a function of the number of multiplex switches connected to the output line. In the majority of applications, particularly those for which the solid state image sensor serves as an input to a machine, random noise does not appear to be a practical problem. The level of the random noise, however, does set a basic limit to the minimum detectable illumination level that can be detected, and in doing so, must be considered in any design.

The second approach, shown in Figure 3 also employs a transfer switch (really an adjustable barrier) for each pixel; however, all pixels are sampled simultaneously, thus transferring all the information in parallel into an analog shift register. This information is then clocked to an output terminal at the end of the analog shift register. The analog shift register has been highly developed over the past few years. Charge-transfer devices, both bucket brigade and charge-coupled, can now be made with transfer efficiencies exceeding 0.9999 at megahertz clocking rates; therefore, the initial problems of shading and loss of resolution are no longer a serious problem.

ARCHITECTURE OF AN IMAGE SENSOR

Figure 4 shows four architectures that may be implemented using the building blocks described above. Let us begin by examining each structure. The first structure to be discussed uses photodiodes as the detectors and a digital shift register to sequentially interrogate these diodes and is depicted in the figure as Combination A. This structure operates in the charge-storage mode and is commonly referred to as a self-scanned photodiode array. To obtain line storage requires a single multiplex switch connected to each photodiode, thus making possible high density linear arrays which possess all the advantages of the photodiode detector. To obtain frame storage in a matrix or two-dimensional array requires that each photodiode have two multiplex switches associated with it. As a result, the size is limited since the minimum center-to-center spacing is about 75 microns. This architecture has, however, been quite adequate for small matrix arrays used primarily as computer inputs, in particular as inputs to microprocessors where, due to limited speed, the amount of data has to be limited. For small chips the I/O usually sets the chip size, hence a higher packing density of some other

architecture would do little to reduce die size. Furthermore, the testing associated with any imaging devices is far more expensive than for other semiconductor devices. This results in the die costs equaling the testing costs for a considerably larger die size than is generally considered by most semiconductor manufacturers. For linear arrays, this architecture is perfectly adequate for realizing long high density arrays. Linear arrays approaching 2000 pixels in length with pixels as close as 15 micron centers have been available for some time. This architecture, however, has reportedly two serious shortcomings. The one most often referred to is the output capacitance, which increases directly with the number of pixels. Its effect is to increase directly the thermodynamic or random noise of the system, thus limiting the minimum number of photons/pixel that can be detected. For linear arrays or for matrix arrays of less than about 10^4 pixels the resulting increase in noise due to increasing output capacitance is usually of no practical importance since other sources of noise usually dominate.

It is usually the fixed pattern noise that has limited the number of grey levels that are discernable. The fixed pattern noise has two origins. Slight differences in the shift register and multiplex switches have been in the past a source of a fixed pattern noise discernable primarily at lower levels of illumination. This, however, has been virtually eliminated by the differential techniques and is, therefore, much less of a problem now as compared to earlier arrays using this architecture. Another source of fixed pattern noise results from the pixel-to-pixel variation in photosensitivity. This results in an uncertainty that also limits the number of grey levels that can be discerned.

The second architecture to be discussed is commonly referred to as a charge-coupled device which uses the field-induced photo-detector as the pixel and the analog shift register to shift the information from the pixel to the output terminal and is depicted by Combination B. Two typical matrix structures are shown in Figure 5. These structures permit very high density with pixel spacings of 20 to 30 microns not uncommon. Depending on the particular criteria employed, the performance of these structures has ranged from adequate to excellent. As a result of the very low output capacitance and the elimination of sequential sampling with multiplex switches, both the thermodynamic and the fixed pattern noise in the dark are exceptionally low. This, however, is offset by the resulting non-uniformity that prevails under illumination. This non-uniformity is a result of the variations in film thicknesses that occur in fabricating the field-induced photo-detector added as well as those non-uniformities that are always present in the bulk silicon. Since the reflectivity as well as the absorption depends on the relative thicknesses of several films, a compromise must be made between spectral response, quantum efficiency, and the non-uniformity. Normal process variations make reproduction of consistent parameters over a period of time somewhat more difficult than for the simpler diffused diode structure. This problem is further aggravated by both the complexity of the required process and its developmental nature, i.e., most CCD processes are not high volume production processes, therefore, they

lack the stability of a standard production process.

The third structure to be discussed, shown as C in Figure 4 combines the field-induced photo-detector with the digital shift register in an effort to obtain higher density with an existing technology. As initially conceived, this structure exhibited excessive uncontrolled blooming, less sensitivity than the photodiode, spectral variations, excessive non-uniformity, fixed patterns in the dark resulting from digital sampling, and an extremely large output capacitance. Most of these difficulties are now under control; however, the technology is no longer standard requiring an exotic metal/silicon gate MOS process on an epitaxial substrate. Furthermore, a double sampling technique must be used to process out the fixed pattern noise resulting from the sequential sampling of multiplex switches and the KTC of thermodynamic noise associated with resetting the output capacitance. As a result of employing this more complicated signal processing technique, the inherent forms of signal contamination are eliminated, and good low level performance is obtained.

The final structure to be assembled from the set of building blocks is shown in Figure 4 as D. This structure uses photodiodes with all their inherent advantages, i.e., spectral purity, high-external quantum efficiency, combined with an analog shift register for readout. This combination possesses all the advantages of the photodiode detector with those of the analog shift register readout. The discussion to follow will describe the practical realization of a matrix array employing this architecture. For lack of a more descriptive acronym, let us refer to this architecture as the optimum solid state image sensor.

REALIZATION OF THE OPTIMUM SOLID STATE IMAGE SENSOR

The architecture of the optimum solid state image sensor has been realized using standard production MOS processes.

Figure 6 shows schematically the basic structure of a matrix array. The sensitive region consists of a matrix of photodiodes. Each column of diodes can be connected to a common video through individual multiplex switches associated with each photodiode. A two-phase dynamic shift register is used to sequentially sample a line of photodiodes, simultaneously dumping the charge into an analog shift register which, in turn, transfers the information to the output terminal. Two analog shift registers are used with alternate photodiodes along a line being dumped into the same readout register. This not only doubles the data rate, making 10 MHz readout rates possible, but also results in a "full wave" or zero-order sample and hold output.

This architecture makes possible a matrix array of photodiodes, each having only a single multiplex switch which provides frame storage. Furthermore, the output capacitance is that of a single line and not the total number of pixels as described earlier.

The reset line ϕ_r biases all video lines at a reference level while the active photodiodes are integrating charge. The biased video lines, therefore, provide anti-blooming and anti-crosstalk control during the readout period. The reset switch ϕ_r is turned off just prior to advancing the line select digital shift register to the next line, and the transfer switch ϕ_t is turned on to the same reference level set by ϕ_r. Conditions are now set for the transfer of the next line of photodiodes into the analog shift registers. An added feature of this structure is that it may be operated in a non-interlaced mode by connecting switches ϕ_3 and ϕ_4 to $+V_{dd}$. Interlacing is obtained by driving ϕ_3 and ϕ_4 with complementary square waves at the field rate. It is also possible to reset the entire frame with one pulse. This permits the monitoring of pulsed illumination.

A timing diagram is shown in Figure 7 for the array operating in the non-interlacing mode. Three sets of complementary clocks (0 to +15 volts) are required: 1. analog shift registers; 2. digital shift registers; and 3. reset and transfer switches. The positive going edge of the transfer clock ϕ_t should lead a transition of the digital shift register clock by about 100 ns to insure that no signal charge is lost. The width of the ϕ_t clock should be minimized (about 1 μsec) to insure good anti-blooming control.

Figure 8 shows a photograph of a 100x100 matrix fabricated using standard two-level polysilicon N-channel MOS process. Although this device is made on 60 micron centers, it is possible to reduce the centers to less than 40 microns without sacrificing performance. The readout registers are bucket brigade. This device has been operated at a combined video rate of 12 MHz without any observable degradation of transfer efficiency in the readout registers. That corresponds to a frame rate of 1200 frames per second. Frame rates as low as 20 frames per second have shown no observable leakage affect at 25^{o}C.

The saturation charge of 2 pc per pixel produces a 2 volt signal at the output of the bucket brigades. A fixed pattern was perceptible in the dark, however, it was more than 60 db below the saturation level. The origin of this fixed pattern is suspected to be due to the short range threshold variation of the reset and transfer switches.

The "anti-blooming" control has been found to be quite effective. Quantitatively, no uncontrolled streaking or smearing could be seen on the monitor when a lighted match is viewed three to five feet from the lens.

CONCLUSION

The basic building blocks of the optimum solid state image sensor have been available for some time, but until now they have not been optimally combined. Not only does this structure excel in its electro-optical performance it also provides electrical versatility as demonstrated by its variety of operating modes.

The structure described in this paper represents the proper combination to realize the full potential of the solid state image sensor.

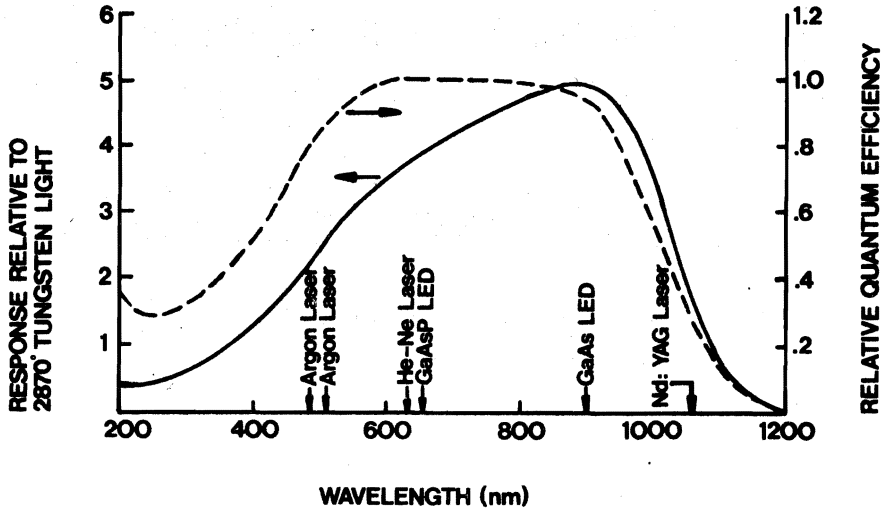

Figure 1. Typical Spectral Response of a Diffused Diode

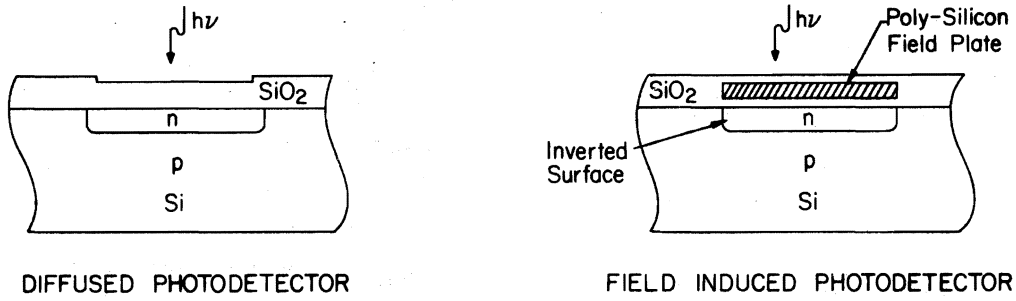

Figure 2. Two Basic Photodetector Structures.

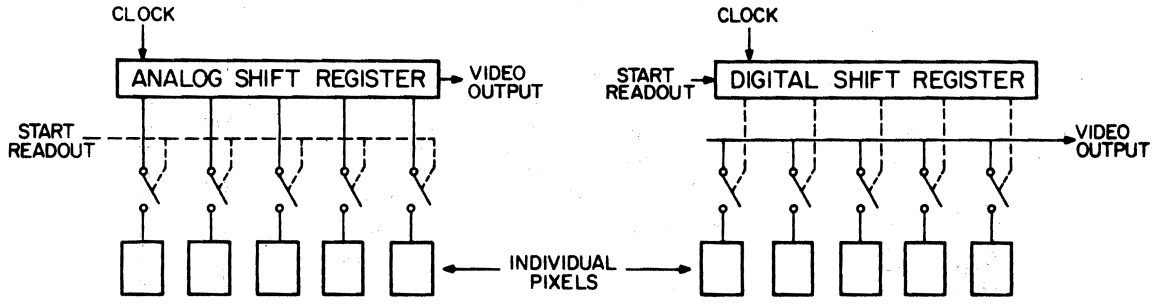

Figure 3. Techniques for Interrogating and Reading-Out Picture Elements.

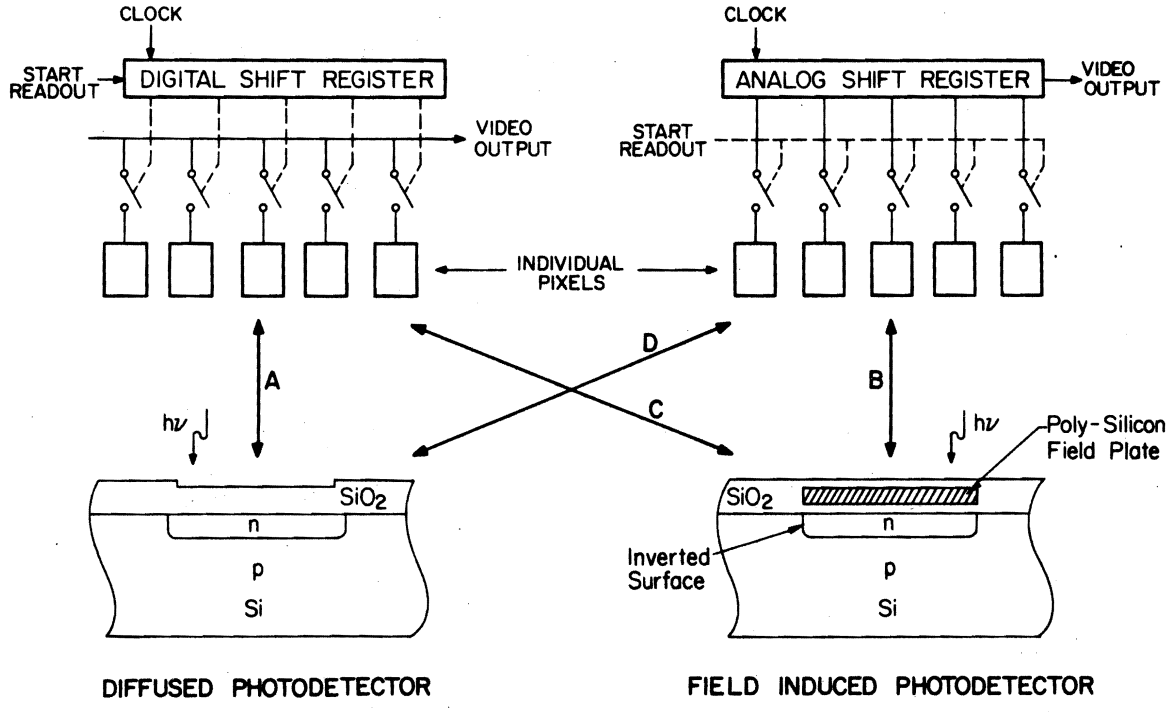

Figure 4. Four Basic Architectures of a Solid State Image Sensor

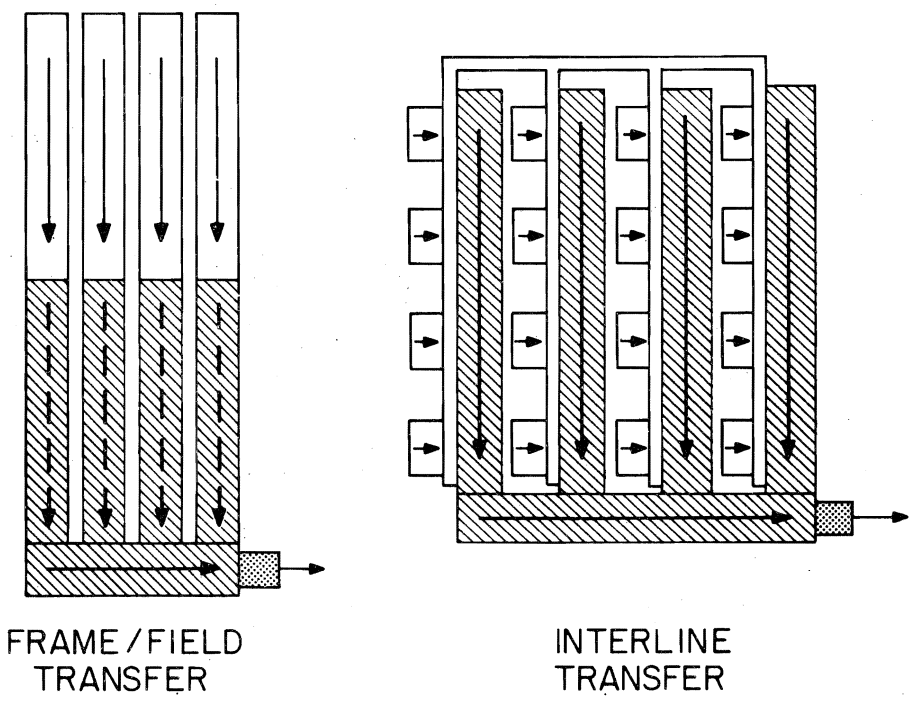

Figure 5. Readout Organization of CCD Matrix Array.

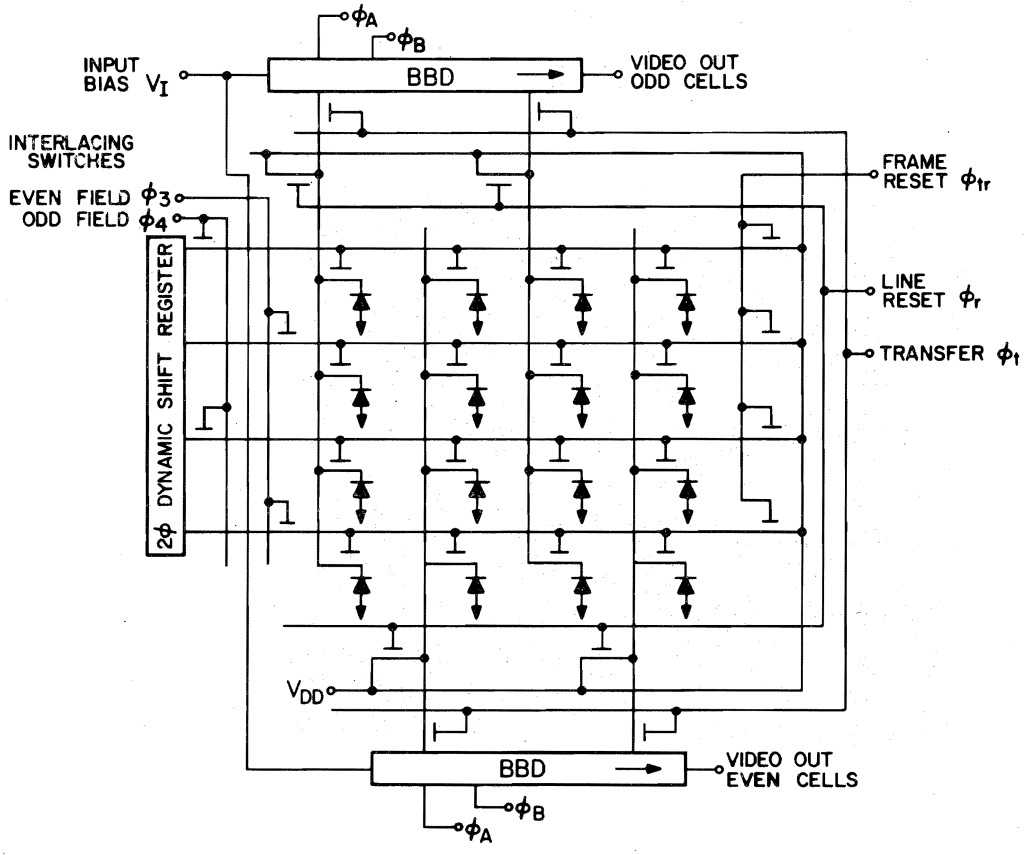

Figure 6. Schematic of Optimum Matrix Architecture.

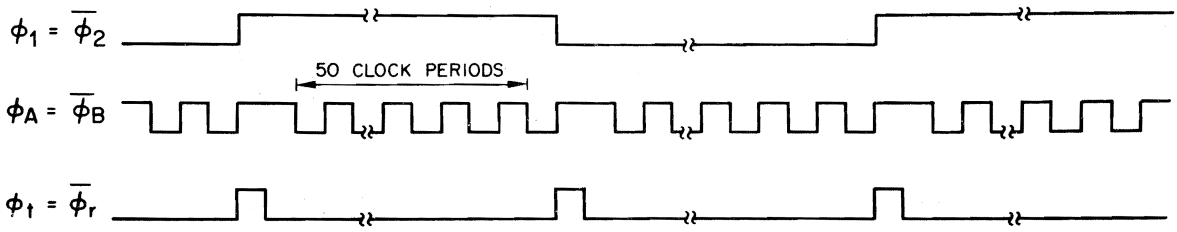

Figure 7. Timing Diagram for Optimum Matrix (Non-interlace model)

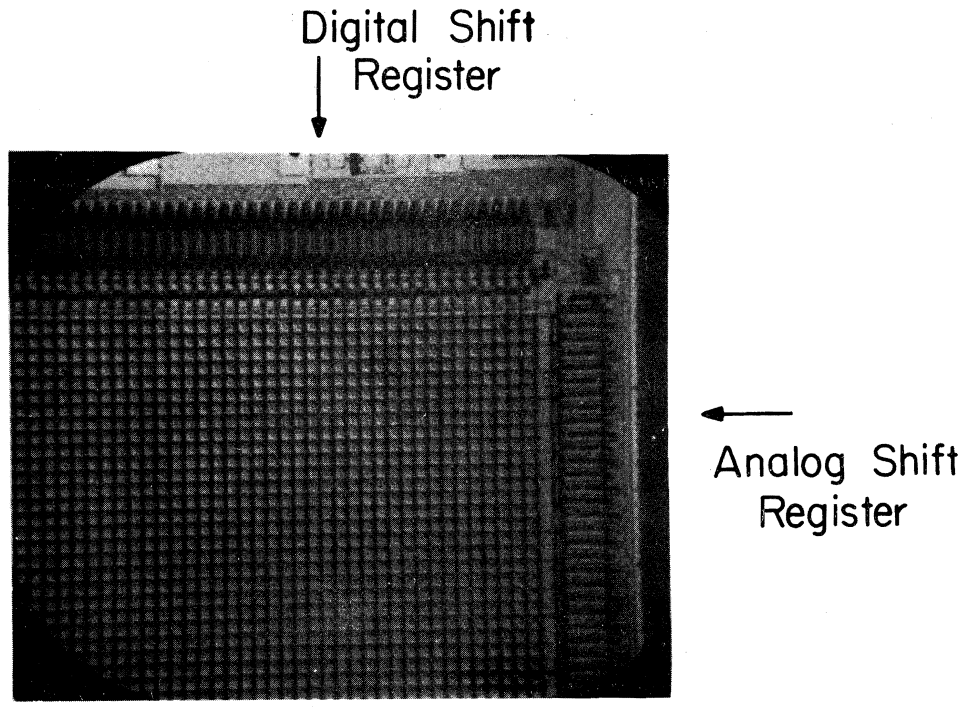

Figure 8. Photograph Showing a Corner of the 100x100 Matrix.