BUCKET BRIGADE DEVICES - CIRCA 1976

Robert R. Buss*and Gene P. Weckler*

ABSTRACT

The bucket brigade was a development of the late 60's at which time it was quite extensively studied. The major shortcoming was found to be inadequate transfer efficiency, thus relegating its usage only to audio applications. Before the problem could be solved, along came charge-coupled devices which showed promise of improved transfer efficiency, higher clocking frequencies and higher density; therefore, most of the work switched from bucket-brigade devices to charge-coupled devices. New processes were developed in order to make charge-coupled devices that could truly realize their predicted potential; however, with these new processes and with charge-coupled devices working fairly well, nobody ever asked what improvement could be realized in a BBD if both modern technology and modern understanding were applied.

In this paper we will describe the modern bucket-brigade device. Transfer efficiencies greater than 0.9998 have been obtained at 5 MHz sampling rates. Bucket-brigade technology is such as to make internal taps and tap weights relatively easy to implement. Interfaces with other MOS devices on the same chip likewise are easy to implement. The modern BBD thus leads to the realization of simple delays, tapped delays, and programmable tapped delay -- both real time and erasable -- as well as to correlators and transversal filters. In many cases a BBD offers a simpler solution than would a corresponding CCD.

INTRODUCTION

The basic structure of the bucket brigade is shown in Figure 1. This device in its integrated form was invented by Sangster (ref 1,2) at Phillips in 1968. There was much interest in this device since it offered a first glimpse of a practical way of implementing an analog delay. However, the initial device had many shortcomings, with the major one being very poor transfer efficiency. Potential variations during the charge-transfer period introduced excessive channel-length and barrier-height modulation and consequent transfer inefficiency. As a result, the device was limited to few stages and to low-frequency applications.

The first major advance made in improving the transfer efficiency was also made by Sangster (ref 3,4) and his co-workers at Phillips. It came from the introduction of an isolation or tetrode structure with a d-c biased gate separating each clocked element from its neighbor, as in Figure 2. The performance was greatly improved, but still limited to audio frequencies and to a relatively small number of transfers. At about this time the charge-coupled device (CCD) was invented at Bell Telephone Laboratories (ref 5). CCD showed the promise of making possible charge-transfer

*Reticon Corporation, Sunnyvale, California.

devices without the shortcomings which appeared inherent in the bucket-brigade device. The CCD did not have a discrete capacitance to charge in every stage, with the result that the KTC noise associated with charging the capacitance over a barrier was nonexistent, and the problems of driving capacitive elements were less severe. In short, CCD looked to have all the potential advantages that were at first associated with the bucket brigade. The CCD appeared to be a very simple structure requiring only simple processing. However, despite the theoretical improvement, the simple structure with the simple process produced devices not much better in performance than the bucket-brigade devices on which there was supposed to be improvement. It took five years and many millions of dollars to develop the understanding and technology to the point which allowed these advantages to be truly realized. It was then that a re-examination of bucket-brigade technology was initiated. Devices fabricated using some of the modern techniques and employing a tetrode structure were found to perform reasonably well, (ref 4) but transfer efficiencies were still less than one could wish; furthermore stability was erratic and the devices were sensitive to clock shapes, particularly the transition edges.

DEVELOPMENT OF THE MODERN BBD

It was at this point in the development of charge-transfer devices generally that a closer look was taken at the underlying BBD structure, the technology, and the processing techniques. Self-aligned structures would reduce parasitic capacitance and improve efficiency. A decrease in substrate resistivity would help to reduce the sensitivity to voltage and to clock wave shape. It would also reduce the conductivity modulation of the region under the transfer gate, which should improve transfer efficiency. However, junction capacitance effects would be adversely affected. It was then determined, that, using modern technology, one could selectively control resistivity and its effects by ion implantation—conductivity could be high where wished, and low where wished. The bucket brigade could have the advantages of a high-resistivity basic substrate for minimum junction capacitance but without its deleterious effects on modulation, etc. The desired low-resistivity areas could be selectively controlled. Further, the ion implantation could be used to control thresholds so that N-channel devices became eminently feasible, with all the consequent advantages of higher speed, better transfer efficiency, etc., which follow from the higher mobility of the carriers. Devices were made using the structures and processes described. Performance is illustrated in Figures 3-5. Transfer efficiency vs. sample rate is shown in Figure 3. Transfer efficiency as high as 0.9998 has been obtained at sample rates up to 5 MHz. Figure 4 shows the dynamic range, in excess of 70 db, and Figure 5 shows the relationship between delay-bandwidth product and the product $N\epsilon$ of transfer inefficiency, ϵ, with the number of transfers, N. It can be seen that modern technology applied to the bucket brigade permits devices with quite adequate dynamic range and yet capability approaching 5000 transfers.

CONSTRUCTION FEATURES

The input structure to the bucket brigade is very simple. It is basically an NMOS transistor analog switch connecting the input to a capacitor, as in Figure 2, which allows one to run a given amount of charge onto the input capacitance and then, via the bucket brigade, transfer that charge on into the first and later buckets. The size of the input structure can be varied to tailor the voltage sensitivity at the input. It allows one to tailor the gain and, along with the ion implant level, also set the bias requirements. The output structure is equally simple. It can consist of a source follower connected to one of the buckets of a stage (note that a "stage" encompasses two buckets). The source follower adds some small amount of capacitance to that bucket. The gain from input to output is determined by the ratio of the capacitance of the output device (the source follower bucket) to the capacitance of the input section, because charge is conserved. A single source follower will produce a half-wave output signal; each time the appropriate clock goes high an output will be produced from the source follower. Two source followers may be used, one connected to a bucket driven by phase one of a stage and the other connected to an adjacent bucket driven by phase two of the stage, as illustrated in Figure 6. Then a full-wave output will result. A full-wave output is much easier to handle, requiring only simple filtering to reduce any clock glitches or sampling glitches, and it does not require an external sample and hold. It also allows one to work much closer to the Nyquist frequency without as severe filtering requirements. The clocking requirements of the bucket brigade are also quite simple; it requires two-phase complementary square-wave clocks. The timing is not critical, the edges are not particularly critical. The device is basically very forgiving. Tetrode gate voltage does have an effect on transfer efficiency; it preferably is set to operate at a voltage very nearly equal to the clock, or less than but within a volt of the clock maximum.

Another very nice feature of the bucket-brigade device is the ease with which buckets may be tapped to obtain output, as mentioned above. A tap may easily be implemented by connecting a source follower to an intermediate bucket. It is possible to connect source followers to every bucket along a device, as shown in the diagram of Figure 6, and not seriously affect the transfer efficiency. This is in part due to the fact that we are looking at real capacitances and not trying to tap in on "phantom capacitances". Another way of implementing taps is by capacitive divider pickoff, as shown schematically in Figure 7, which allows one to build transversal filters with taps which can be capacitively weighted, with on-chip electrode structures, just as is done with charge-coupled devices; however, in the BBD it is possible to separate the sensing-electrode pattern from the clocking-electrode pattern without causing any serious degradation of transfer efficiency. Furthermore, is is possible to cancel clocking transients because coupling from $\emptyset_1$ through C_a cancels that from $\emptyset_2$ through C_a', etc. In Figure 7, the relative tap weight is given by

$$w = \frac{C_a - C_b}{C_a + C_b}$$

It is evident that the weight, w, may be controlled over the range +1 (when $C_b = 0$) to -1 (when $C_a = 0$). One thus realizes simplicity of signal extraction, without having to bother with coordination with clocks multiplexed on the same lines as the signals. These are but a few of the unique advantages of the bucket brigade which, with suitable modern technology, make it a device quite adequate for a goodly number of signal-processing applications.

WHY USE BUCKET-BRIGADE DEVICES?

We have all known that charge-transfer devices are very suitable for analog signal processing. However, most people immediately conclude that using charge-coupled devices is the only way to do the job. If you say that you are going to use a bucket-brigade device, immediately they ask: "Why not use charge-coupled?" Well, probably the most important single reason is that bucket-brigade devices use standard MOS processing. This means that they can be processed on a standard production line using existing technology, which in turn results in higher yield, and more cost-effective components. Another advantage, which is often overlooked, is that being compatible with existing MOS processes means that a wealth of circuitry used in making ROM's, RAM's, PROM's, and micro-processors is all available to the charge-transfer device designer. This allows the designer to build such things as flip-flops, clock drivers, shift registers, and even programmable memory onto the same chip with the charge-transfer device. Another advantage of bucket-brigade devices is the ease with which the clocks may be generated. There are no tricky multi-phase clocks; a simple two-phase complementary square-wave clock is all that is required. The output circuitry is equally simple, allowing one to do either capacitive sampling of the bucket such as in a tapped delay line, or to use source followers which are directly driven by the buckets and in turn act as current sources to the outside world. The bucket-brigade is capable of sampling at rates up to 5 MHz or more. This situation is also compatible with peripheral circuitry, which usually is capable of operating to 5 MHz rates or greater.

WHEN SHOULD ONE USE BUCKET-BRIGADE DEVICES?

Bucket-brigade devices are most suitable for sample rates below 5 MHz, for delays not exceeding 5,000 transfers (2500 stages), or when simplicity of associated circuitry for peripherals, etc., is a major consideration. There is also no advantage to using the alternative CCD (which does allow higher packing density) when packing density is only secondary, such as when peripheral circuitry or when pads determine the size of the chip and not the charge-transfer device itself. In such cases no real advantage can be obtained by using charge-coupled devices. Bucket-brigade devices are a natural in audio delays up to about 2,000 stages. For more than 2,000 stages one runs into transfer-efficiency problems, as well as into an increasing noise floor, both functions of the number of stages in a bucket brigade.

The following examples illustrate areas of suitability for bucket-brigade devices. The SAD-1024 illustrated in Figure 8 is widely used in

audio delay applications. It uses ion-implanted N-channel technology and is the first of a family of such devices. Other members take advantage of MOS processing compatibility to add on-chip clock drivers, etc. The high-speed delay element of Figure 9 illustrates a multiplexing technique to increase the effective sample rate. This device routinely operates at a 10.7 MHz sample rate, with signal frequency performance limited by recovery of the fundamental-frequency components from the stair-step sample-and-hold waveform rather than by device limitations.

The 32-stage tapped analog delay (TAD-32) illustrated in Figure 10 (schematic as in Figure 6) is the first member of a whole family of signal processing devices based on tapped bucket-brigade delay lines. This device permits arbitrary tap weights for such uses as transversal or recursive filtering, fixed-weight correlation, convolution, etc. Figure 11 illustrates the BAC-32, a somewhat different arrangement functioning as a binary-analog correlator. This device has an on-chip static shift register which may be loaded with any desired binary sequence which then controls the (positive or negative, one or zero) tap weights from the BBD delay-line taps. This device permits 32-point real-time binary (or P-N) sequence correlation with an analog input signal.

Other processing devices are in advanced development status. These include analog-to-analog correlators, pre-weighted filters (with capacitive pickoff taps) and electrically programmable (and reprogrammable) multitap tapped delay devices. These same BBD structures are also finding applications as a readout mechanism for a solid-state image sensor, as described in a later session (ref 6).

SUMMARY

In summary, then, bucket-brigade devices should be used for audio and other low-frequency applications, in some video-delay applications, and in signal processing generally, where the bucket brigade is a natural. It is exceedingly flexible and noncritical in delay applications. With modern technology, it exhibits high transfer efficiency, moderate speed, and simplified interface requirements. It allows you to make transversal filters using split-electrode structures; however, the split electrodes are strictly sensing structures and are not part of the clocking circuit, nor do the structures suffer from overlap capacitance as is typical in CCD split-electrode structures. The sense electrodes are separate from (and balanced to) the clocking electrode structure. Furthermore, in a transversal filter, a processing gain is available because of the summed signals from multiple taps; thus, the device is not as sensitive to noise as would be a simple long delay used, for instance, in audio or video type applications.

CCD is needed when extremely long delays are desired, such as an 8000-stage audio delay line where wide dynamic range is also desired. Properly designed CCD's have higher transfer efficiency, and a noise limit that does not increase as rapidly as in a BBD when the number of stages is increased. CCD's also should be used when sampling rates significantly in excess of 10 MHz are desirable, or when packing density is of prime importance, and where the penalty of extra complexity is permissible.

Operation at elevated temperatures limits storage lifetimes, and hence forces a practical limit to the amount of delay possible, or

alternatively, to the number of taps possible. Further, in most signal processing applications such as correlators or transversal filters, one finds a limitation imposed by the time required to do the calculation and the number of points in the calculation. Therefore, a time-complexity compromise must be made. For instance, at 1 MHz sample rate, it would take 32 ms to compute a 32-point calculation, and 64 ms for a 64-point calculation. A compromise must be made between the total number of taps in the device and the speed of the computation. It has been found that, for the accuracy that is possible in today's charge transfer devices and the speeds at which they are capable of operating, 32 to 64 stages are about the optimum number of stages in signal processing. This is not to say that units could not be cascaded or extended to increase the number of points in the computation; however it takes time to make the application to additional points. Therefore, if processing requires less than 100 stages, it is much better to use a bucket-brigade and have all the advantages of today's technology and the advantages of available peripheral circuitry, rather than have all of the processing and application problems of charge-coupled devices.

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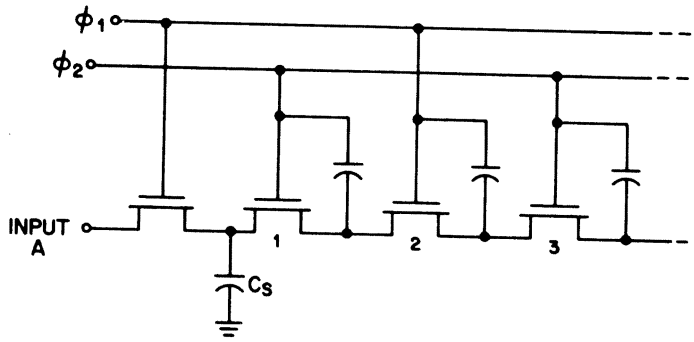

Fig. 1 Basic bucket-brigade structure.

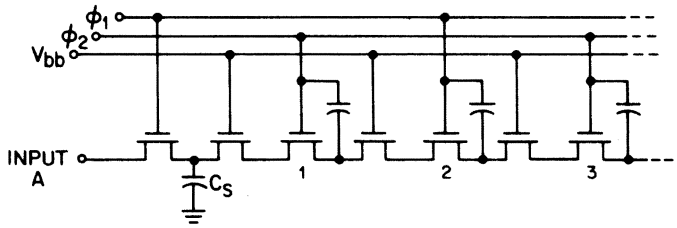

Fig. 2 Improved bucket-brigade structure with tetrode isolation.

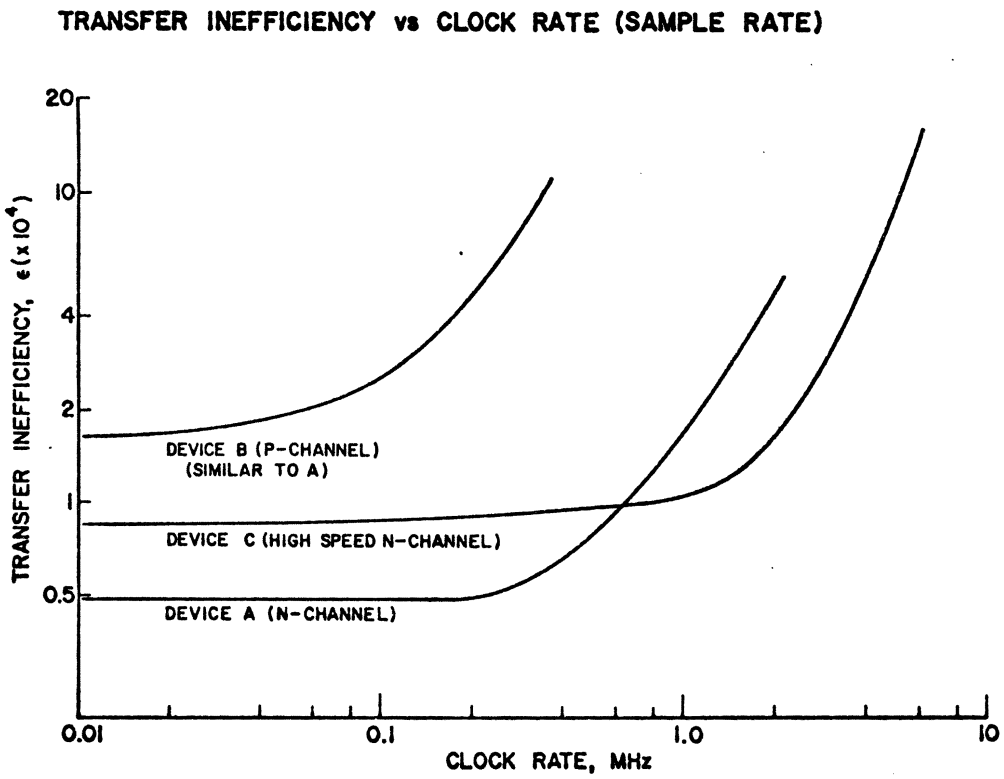

Fig. 3 Transfer efficiency vs. sample rate for two commercial audio devices and one high-speed device.

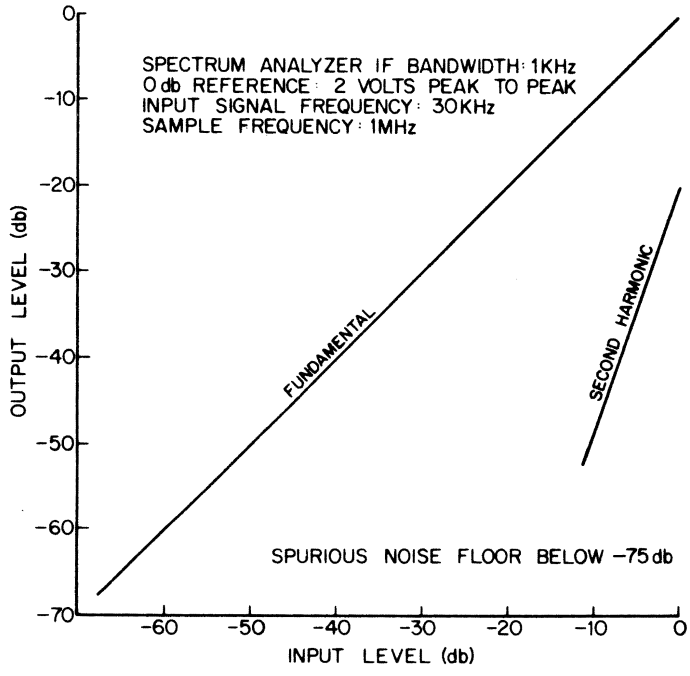

Fig. 4 Dynamic range and linearity for tetrode BBD.

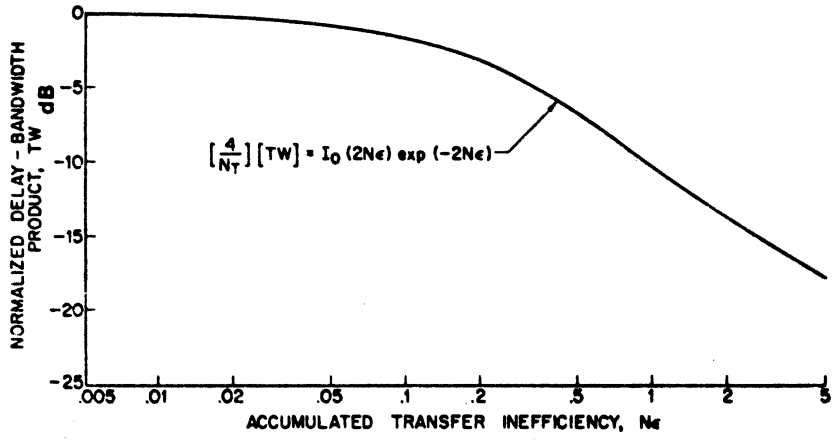

Fig. 5 Normalized delay-bandwidth product vs. accumulated transfer inefficiency Nε.

A TAPPED ANALOG DELAY LINE MADE USING METAL-OXIDE-SILICON INTEGRATED CIRCUIT TECHNOLOGY

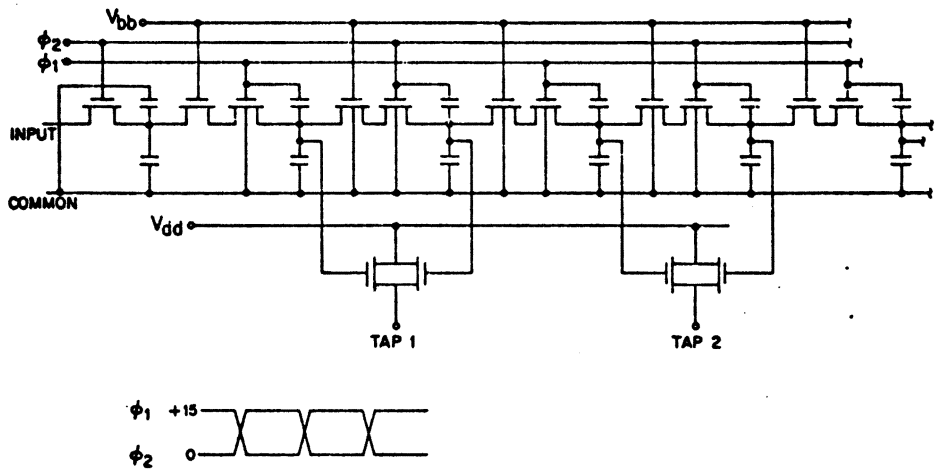

Fig. 6 Equivalent schematic circuit for tapped BBD.

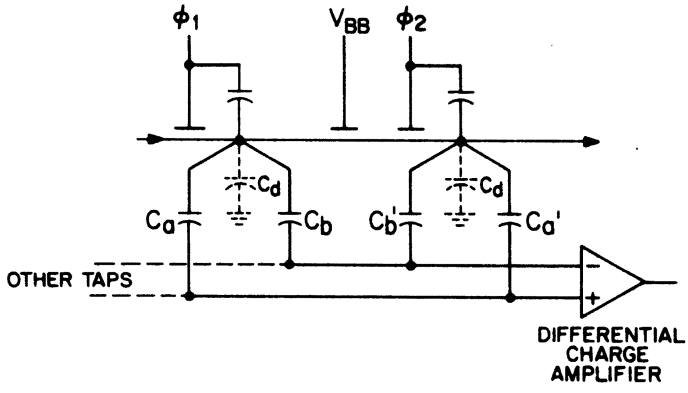

Fig. 7 Capacitive divider taps for BBD.

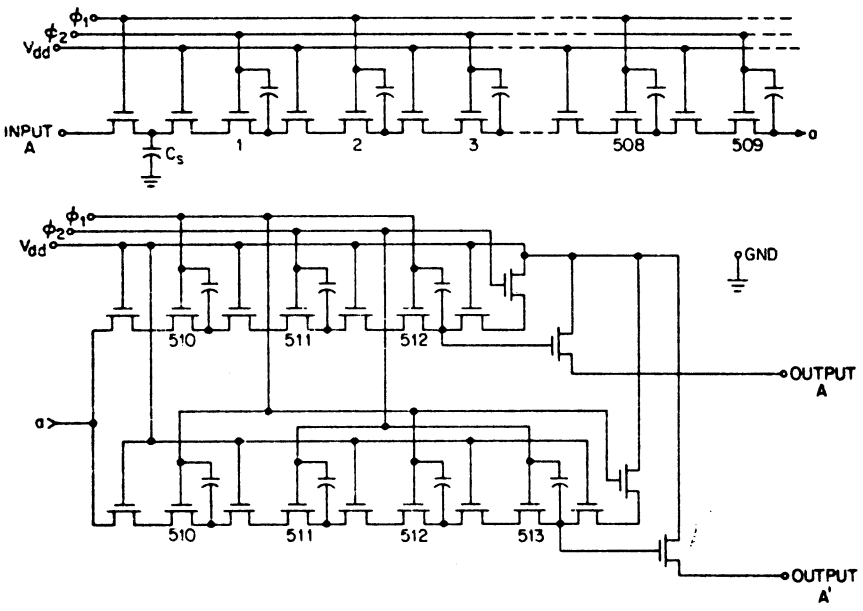

Fig. 8 Equivalent circuit diagram for an audio-frequency BBD, the SAD-1024.

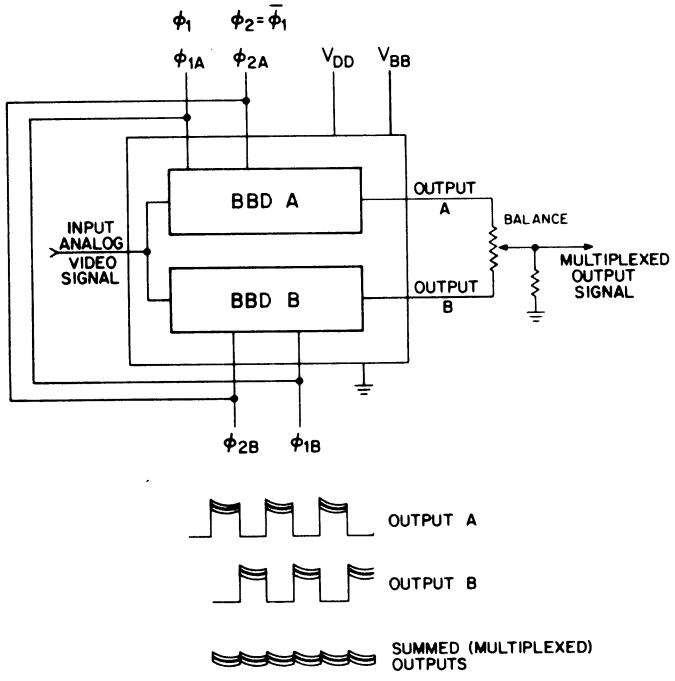

Fig. 9 Method of multiplexing delay lines to obtain wide-band high-frequency operation (SAD-341).

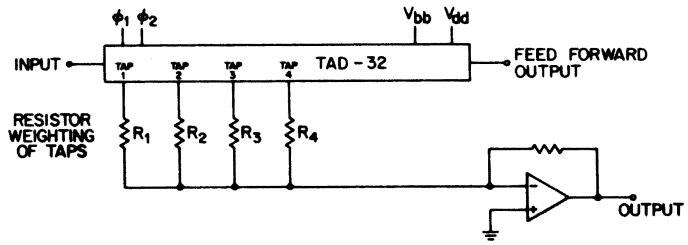

Fig. 10 The TAD-32, a Tapped Analog Delay device.

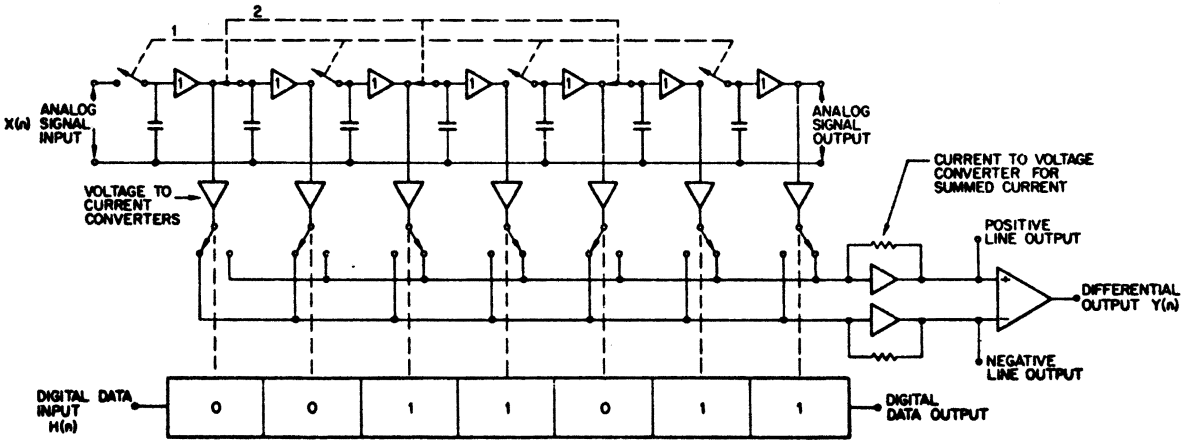

Fig. 11 An example of a BBD Binary-Analog Correlator (BAC-32).