DESIGN ASPECTS OF S-SHAPED BULK C-COUPLED DEVICES

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ABSTRACT

A two-dimensional potential model of a Bulk CCD containing no mobile charge is used to estimate the charge handling capability and the speed of charge transfer. The influence of unequal gate electrode lengths, the geometry of the bend and the donor distribution in the charge transporting layer are evaluated numerically and compared with measurements of experimental S-shaped devices.

INTRODUCTION

Measurements on experimental Peristaltic Charge-Coupled Devices (PCCDs) have shown that high transfer efficiencies and relatively high charge-handling capabilities can be obtained even at high clock frequencies (refs 1 and 2). Several new signal processing applications are therefore within the capability of this device. From the viewpoint of costs and for other reasons, it is desirable to use an existing MOS-process technology, although the design rules of the latter often require somewhat larger electrode lengths than a CCD process. We have available a MOS-technology (ref. 3) with a two-layer metallization of poly Si and Al, having a layer of thermal SiO_2 in between. Designing a CTD in this technology, mask and alignment tolerances give rise to an asymmetric gate structure with e.g. poly gate lengths of 14 μm and Al gate lengths of about 6 μm. With these gate lengths a device with several hundreds of stages and a straight transfer channel would give the chip a large and unfavourable length-to-width ratio. A better ratio can be obtained by folding the transfer channel. The influence of the inequality of the gate lengths, the geometry of the bend and the donor distribution in the charge transporting layer are evaluated numerically.

BASIC MODEL AND ASSUMPTIONS

The Bulk CCD (fig. 1) is assumed to consist of:

- an n-type layer with a special doping profile in the depth (y-direction), completely depleted of electrons;
- a homogeneously doped p-type substrate, depleted to a depth H which is assumed to be constant in the transfer direction x;
- a gate dielectric without charge;
- an overlapping electrode structure with alternating electrodes of lengths L_1 and L_2; the interelectrode gap is negligibly small and is taken to be zero; the electrode width w is large compared to its length L ($w \gg L$).

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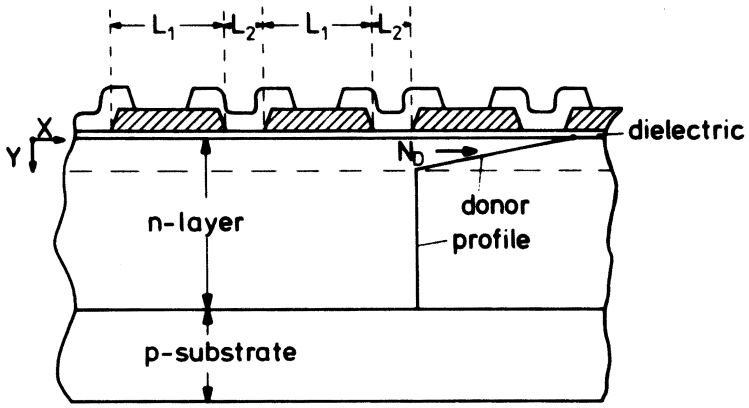

Fig. 1. Cross-section of a profiled Bulk CCD.

The potential V in the dielectric, the n-type layer and the p-type layer satisfies Poisson's equation

$$\nabla^2 V_i = -\frac{\rho_i}{\varepsilon_i} \qquad (1)$$

in which ∇^2 denotes the two-dimensional Laplacian, ε_i the permittivity and ρ_i the space-charge in the appropriate regions. In order to make a two-dimensional calculation of the potential V(x,y) and the field E(x,y) in the depleted n- and p-type layers, the following procedure was followed. Using the principle of superposition the solution of eq. (1) under the appropriate boundary conditions is assumed to consist of two components V_i^I and V_i^{II}. The potential V_i^I is due to the electrostatic influence of the electrodes, whereas the potential V_i^{II} accounts for the influence of the space-charge of ionized impurities in the silicon layers. As pointed out in ref. (4), the potential V_i^I can be found by the method of images as a function of the potential difference ΔV between the two electrodes and the angle Θ, as shown in fig. 2. Taking into account reflections and transmissions at the

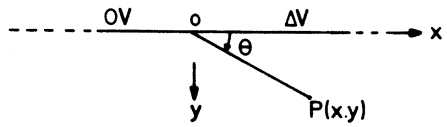

Fig. 2. Diagram of a two-electrode unit.

permittivity interface SiO_2-Si and reflections at the electrodes, the solution for V_i^I can be expressed in terms of gate potentials and the corresponding angles (ref. 4). The method is particularily suitable for solving problems where non-periodic electrode lengths are involved.

The second part takes into account the space-charge distribution in the semiconductor. The electrode potentials are assumed to be at their average value. V_i^{II} satisfies Poisson's equation (1) and can be solved analytically. The actual donor distribution $N_D(y)$ is modelled into such a form that it can be integrated twice. For the PCCD the donor concentration in the top layer is assumed to decrease linearly. The deeper part of the (epi-) layer has a constant dope level. We shall call this a linear graded donor distribution. In the case of a Bulk CCD with a Gaussian donor distribution an approximation with two parabolas can be made, matched at the points of the maximum and minimum concentration and at the bending point.

An example of the two-dimensional distribution of the potential is given in fig. 3. A potential well for electrons is formed under the

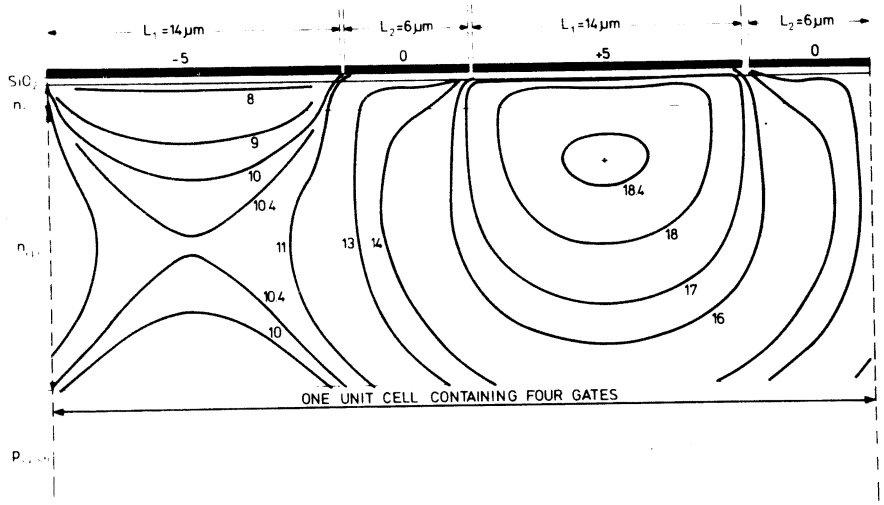

Fig. 3. Equipotentials for a four-phase profiled PCCD with L_1 = 14 µm, L_2 = 6 µm, N_D decreasing linearly from 1.3×10^{17} cm^{-3} to 6×10^{14} cm^{-3} over 0.3 µm and remaining constant from 0.3 µm to 4.5 µm; the gate-oxide is 1000 Å thick. The smaller gates are at zero volt; the larger are at +5 and -5 V.

storage electrode (+5 V) and under the two transfer gates (0 V); the blocking gate (-5 V) separates one well from the next. The potential (and field) distribution is firstly used to estimate the charge handling capability and secondly to establish the maximum clock frequency with which the signal charge can be transported from one well to the next.

THE CHARGE HANDLING CAPABILITY Q_{MAX}

For the calculation of Q_{max} we followed a method proposed by Collet (ref. 5). It is based upon the fact that the size of a charge packet can be limited either by overflow or by accumulation (fig. 4). Overflow of carriers to the neighbouring wells occurs when the internal potential under the storage gate V^S (and under the transfer gates) reaches the potential level maintained under the blocking gate V^b_{max}, which is assumed to remain constant. Taking $V^S - V^b_{max}$

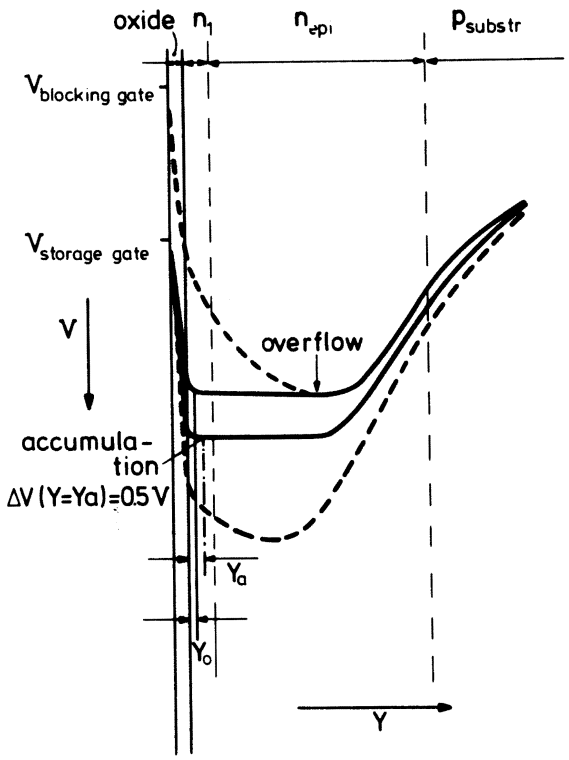

Fig. 4. Schematic representation of the potential distribution under the storage and blocking gate as a function of the depth y. The solid lines give the potential distribution under the storage gate. Of the two limiting mechanisms, i.e. overflow and accumulation, accumulation here limits the packet size (Ya > Yo)

equal to zero, the distance Yo by which the charge stays away from the interface can be found by a simple one-dimensional calculation. Accumulation occurs if the potential well is filled up to the $Si-SiO_2$ interface. Unoccupied surface states will be filled and interact with the packet during charge transfer. To prevent this interaction the charge packet must stay away from the interface, e.g. a 0.5 V difference between the interface and the edge of the packet will be a reasonable value. The corresponding distance Ya can be calculated taking into account the donor profile in the n-layer. Which of the two mechanisms will limit the maximum amount of charge to be stored in a potential well can be determined by comparing Ya and Yo. Fig. 4 shows the situation where accumulation is the limiting mechanism with Ya > Yo. The maximum charge can be found by integrating the dopant between either Yo or Ya and Y^b, where Y^b is the boundary of the charge packet on the substrate side. It can be calculated from the potential difference between substrate and charge packet and the substrate and n-layer dopant concentrations.

$$Q_{max} = Q^S_{max} + 2 \cdot Q^{tr}_{max}$$

$$= A^S \int_{Yo\ or\ Ya}^{Y^b} N(y)dy + 2.A^{tr} \int_{Yo'\ or\ Ya'}^{Y^b} N(y)dy \qquad (2)$$

where A^S and A^{tr} are the areas of the storage gate and the transfer gate respectively. To what extent the transfer gates may contribute to the charge handling capability depends strongly on the phasing of the clock voltages. Eq. (2) holds if the transfer gates are both at half the potential of the storage gate. For devices with $L_2 < L_1$, which are operated in such a way that charge is stored under one gate at a time, the value of Q_{max} will always be limited by the small gate (of length L_2). Eq. (2) is then reduced to

$$Q^S_{max}\ (L_2) = A^S\ (L_2) \int_{Yo\ or\ Ya}^{Y^b} N(y)\ dy \qquad (3)$$

THE SPEED OF CHARGE TRANSFER

It has been shown previously (ref. 1) that fringing fields, caused by the difference in gate potentials, determine the transfer speed of the last fraction of the charge. The two-dimensional calculation of the electric field shows that its value in the transfer direction E_x depends upon the position x under the transfer electrode and upon the depth y. Carnes et al (6) showed that for the transfer of a single electron from the middle of the transferring gate to the middle of the storage gate, the average field is about twice the minimum field under the middle of the transfer gate E^o_x. The single carrier transit time τ_o is then given by:

$$\tau_o = \frac{\frac{1}{2}\ (L_1 + L_2)}{\mu_n . 2\ E^o_x} \qquad (4)$$

in which μ_n is the electron mobility at the depth where the transfer takes place. Because of the thermal motion of the charges, diffusion has to be taken into account (ref. 6) resulting in:

$$Q(t)/Q(o) = \exp\ (-t/\tau_o) \qquad (5)$$

where Q(o) and Q(t) are the amount of charge present under the transfer gate at t = 0 and t = t respectively. Q(t)/Q(o) is per definition identical to the transfer inefficiency ε. For a p-phase system the maximum clock frequency f^{max}_{clock} for a transfer inefficiency ε is given by:

$$f^{max}_{clock} = \frac{-1}{p . \tau_o\ \ln\ \varepsilon} \qquad (6)$$

THE PERFORMANCE FACTOR I_{MAX}

The maximum output current of the device:

$$I = Q_{max} \cdot f_{clock}^{max} \tag{7}$$

contains both the maximum stored charge and the maximum clock frequency. We use it as a figure of merit and call it the performance factor.

NUMERICAL RESULTS

Straight channel devices. With -5 V, 0 V and +5 V on the blocking, transferring and storage gates respectively we calculated for devices with equal and unequal gates lengths L_1 and L_2 the following: $Q_{max}^{+5}(L_2)$ (i.e. the charge stored under the smallest gate, when it is the storage gate), f_{clock}^{max} for $\varepsilon = 10^{-4}$ and I_{max} $(= Q_{max}^{+5}(L_2).f_{clock}^{max})$. The results of this numerical calculation are presented in fig. 5.

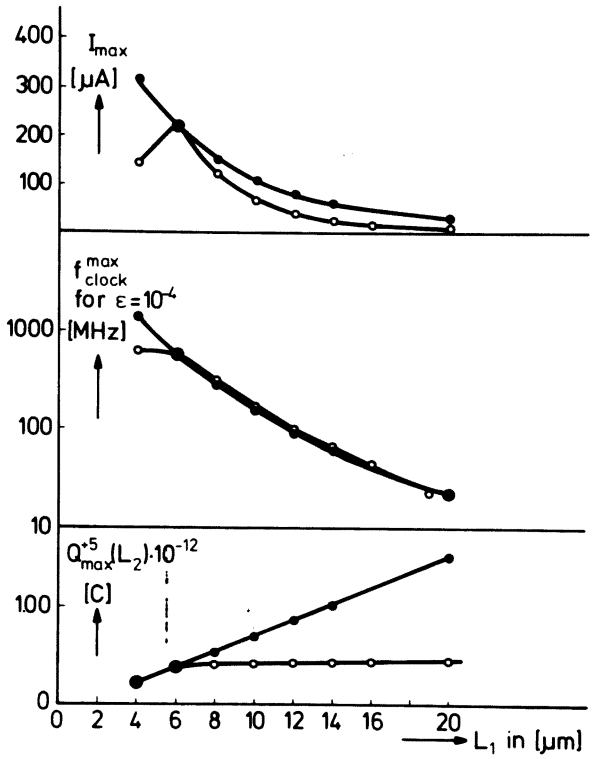

Fig. 5. Comparisons between the $Q_{max}^{+5}(L_2)$, f_{clock}^{max} and I_{max} for a PCCD with equal •–• and unequal o–o lengths of the clock electrodes. For the unequal lengths L_2 has been taken constant (= 6 μm). The width of the channel is 40 μm.

Varying the length of gate L_1 changes the maximum charge packet size per unit cell only when $L_1 < L_2$. For $L_1 > L_2$ the L_2-gate will limit the packet size. The lateral electric field E_x will be smallest under the longest gate L_1. Thus f_{clock}^{max}, being proportional to the

electric field E_x, according to eq. (6), will depend primarily on the length of gate L_1 for $L_1 > L_2$. When L_1 becomes smaller than L_2 ($L_1 < 6$ µm), the field E_x under L_2 becomes smallest. Hence in this dimensional range the length L_2 influences the value of f_{clock}^{max}. With gate length L_1 longer than 6 µm (= L_2), the speeds of devices with $L_1 = L_2$ and $L_1 > L_2$ are practically the same, although the distance $\frac{1}{2}(L_1 + L_2)$ over which the electrons are transferred (eq. 4) is larger for the devices with the equal gate lengths. The larger distance, however, is just compensated by the higher field which is present (and numerically calculated) in the symmetrical devices. The maximum device current $I_{max} = Q_{max}^{+5} \cdot f_{clock}^{max}$ is always higher for devices with equal gate lengths ($L_1 = L_2$), than for those with unequal lengths ($L_1 = L_2$).

Bent channel devices. To evaluate to what extent charge handling capability and speed are lowered in a bend would require a knowledge of the potential and field in every point in the transfer channel, taking into account the increase in gate length when going radially from the inside to the outside of the bent transfer channel. A third coordinate dependence, perpendicular to the x-y plane (see fig. 3) would have to be introduced. This would drastically complicate the calculations. To estimate the effect of the bending the normal calculation procedure was carried out for different values of the gate length L_2 keeping L_1)= 14 µm) constant. An approximation is then made to the sector of the bend with radially increasing L_2 values by rectangular parts with gate length L_2 and constant width W. The approximation is sketched in the lower part of fig. 6. By this approximation the assumption of infinite extension of the gates in the width (= z-direction) has been violated, but the potential distribution obtained will not deviate too much from the exact solution because $W > L_2$. Fig. 6 gives the values of Q_{max}^{+5} (L_2)

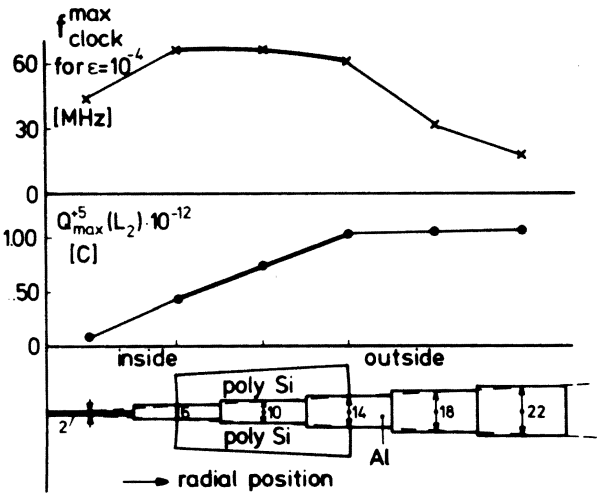

Fig. 6. The charge-handling capability Q_{max}^{+5} (small gate) and f_{clock}^{max} for different values of the length L_2, which approximates to the situation in a bend in a Bulk CCD. The length L_1 has been taken constant (14 um); the width of the n_1-channel is 40 um. The profile of n-type layer is linear graded.

and f_{clock}^{max} for $\varepsilon \approx 10^{-4}$ as a function of gate length L_2. Going from the inside to the outside of the bend the value of Q_{max}^{+5} (L_2) increases until $L_1 = L_2 = 14$ µm. For $L_2 > L_1$ the L_1-gates, now being the smallest, will limit the charge packet size, and Q_{max}^{+5} $(L_2 > L_1 = 14$ µm) remains constant.

It may be noted that f_{clock}^{max} keeps practically the same value when L_2 varies between 6 and 14 µm; this value is numerically the same for a device with a straight transfer channel having gate lengths of $L_1 = 14$ µm and $L_2 = 6$ µm. That the speed of charge transfer is lowered for $L_2 > L_1$ has been explained before, but a lower speed is also found, for $L_2 > 6$ µm, although L_1 is constant at 14 µm. This means that the fringing field E_x under the middle of longest gate L_1 is lowered when the two neighbouring L_2 gates become very small. The results of Q_{max}^{+5} (L_2) and f_{clock}^{max} show that a straight transfer channel and a bend are identical as long as L_1 (straight section) = L_1 (bent section) and L_2 (straight section) < L_2 (bent section) < L_1.

A further consequence of the increasing length of the L_2-gate with the radius is the increasing value of the potential V_{max} when L_2 is at +5 V. This means that the first electrons will be stored only at the outside of the bend; when the charge packet increases the inside will also be filled. This has been visualized in fig. 7.

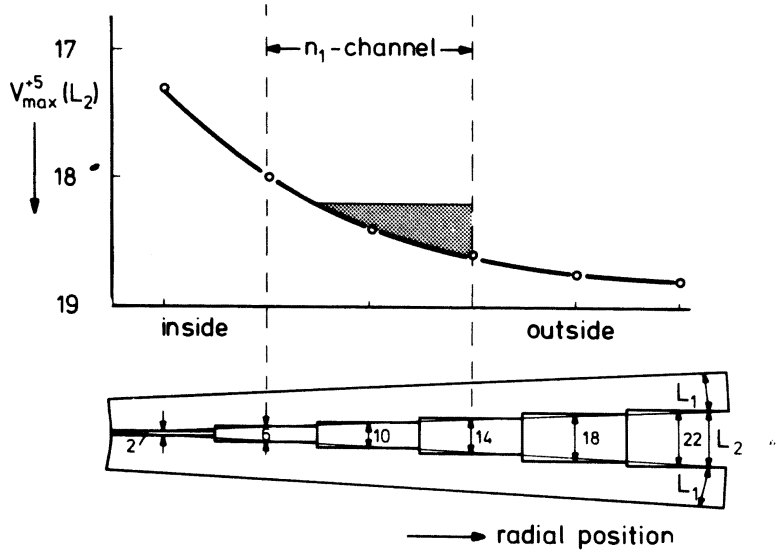

Fig. 7. V_{max}^{+5} (L_2) as a function of the radial position in a bend. A small charge packet will be stored at the outside of the bend.

Small packets of electrons will follow a transfer path which lies along the outside of the bend.

Gaussian dopant profiles. Four different Gaussian donor distributions, differing in the depth of the maximum donor concentration and in the width ($\sqrt{2}$ Dt) of the distributions, have been compared with a distribution of the linear graded type. The comparison has been made for the same electrode lengths ($L_1 = 14$ µm, $L_2 = 6$ µm), for the same dope density (2.25×10^{12} cm^{-2}) and for the same substrate bias voltage. The results of fig. 8 show that for increasing values of Y_b ($= Y_m + \sqrt{2}$ Dt), i.e. for flatter profiles, the value of Q_{max}^{+5} (L_2) decreases while the speed increases. The results show further that the maximum possible device current I_{max}

in the device with the linear graded distribution is higher than for devices with the Gaussian profiles considered.

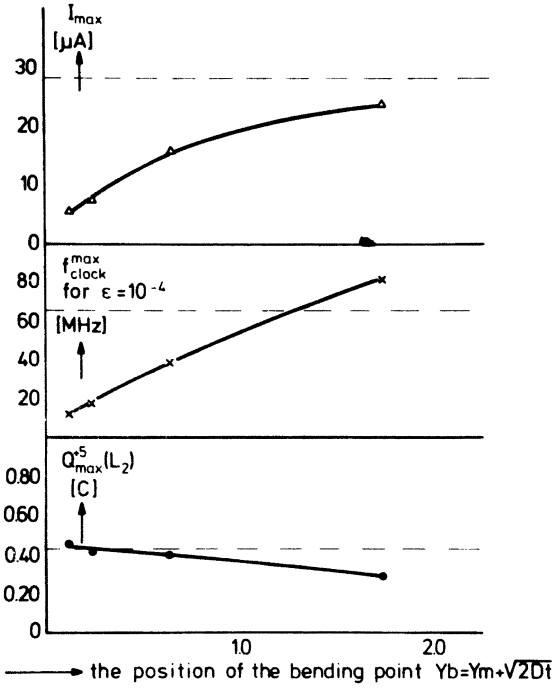

Fig. 8. $Q_{max}^{+5}(L_2)$, f_{clock}^{max} for $\varepsilon = 10^{-4}$ and I_{max} for Bulk CCDs having a different distribution of donors in the n-type layer. The dashed line represents a PCCD with a linear graded profile. The donor dope is 2.25 x 10^{12} cm^{-2}; the channel width is 40 μm.

EXPERIMENTAL RESULTS

Experimental S-shaped PCCDs (photograph 1) were made and Q_{max} was measured. On the masks the electrode lengths were 14 μm (poly Si; L_1) and 6 μm (Al; L_2). In the bends the length of the poly Si was kept constant; L_2 increased radially from 8 to 12 μm over the active region. The width of the channel was 50 μm, the oxide thickness 1000 Å. The linear graded donor distribution was made by an As implantation of 40 keV energy and a dose of 2 x 10^{12} cm^{-2} in an epilayer with a dope of 6 x 10^{14} cm^{-3} phosphorous and a thickness of 4.5 μm; the substrate dope was 2 x 10^{14} cm^{-3}.

The measurements of the charge handling capability were performed under optimum conditions (i.e. the average gate voltages on the poly Si and Al electrodes were adjusted to correct for differences in threshold voltages; the substrate voltage was set such that overflow and accumulation occurred simultaneously). The values of the measured Q_{max} were always within 10% of the calculated value.

The dependence of f_{clock}^{max} on the various design parameters has not been checked experimentally. Measurements of the transfer inefficiency ε showed that, for the experimental S-shaped structure, the ε-values stayed low (about 2.10^{-5}) up to 60 MHz, the highest clock frequency which could be generated in the present set up. This value suggests that the

theoretically found maximum clock frequency of 66 MHz for $\varepsilon = 10^{-4}$ can be easily reached.

SUMMARY AND CONCLUSIONS

1. The maximum "signal" current for a device with given bit-length can be obtained with a symmetrical structure i.e. $L_1 = L_2$. Asymmetrical gate structures, which are often the result of a technological compromise, have either lower charge handling capabilities or lower transfer speeds.
2. If properly designed, i.e. L_1 (straight channel section) = L_1 (bent transfer section) and L_2 (straight transfer section) < L_2 (bent transfer section) < L_1, the folding of the transfer channel will not limit the performance of the Bulk CCD. Within the limits given above (pnt 1), the straight transfer channel will determine the ultimate behaviour of the device. The radial distribution of the potential, when L_2 is the storage gate, causes small charge packets to move along the outside of the bend during charge transfer.
3. Bulk CCDs having one single Gaussian donor distribution have either lower transfer speeds or lower charge handling capabilities when designed and operated in the same manner as a device with a linear graded profile.
4. Under optimum conditions the measured values of Q_{max} agree reasonably well with those calculated.

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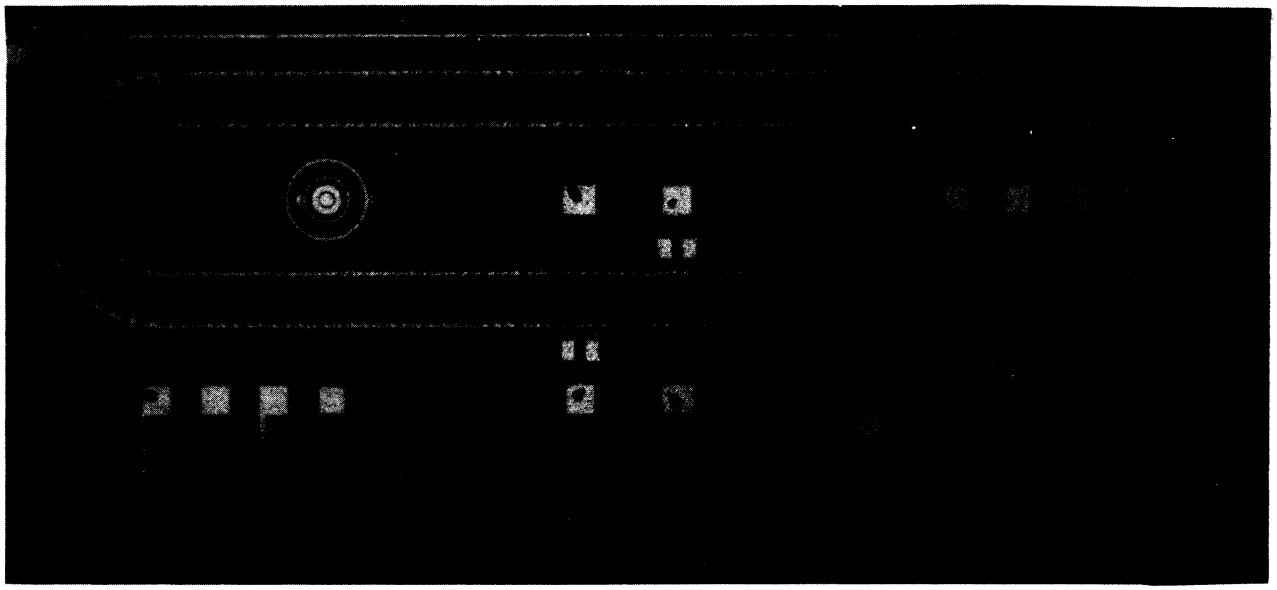

Photograph 1. An S-shaped PCCD of 256 bits.