

CCD WITH MEANDER CHANNEL

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ABSTRACT

A CCD with two straight gate electrodes over a meander channel is proposed. The proposed CCD is suitable for transversal filters and clock line addressable memories because (a) the signal can be picked up at any point along the channel by a simple electrode without a crossover, and (b) only two discrete electrodes have to be driven for each channel and there is no need for bus lines which complicate the electrode pattern.

The preliminary experiments of 32 bit shift registers exhibited a transfer efficiency above 99.95 % in one phase mode operation. The features and applications of the CCD are discussed.

I. INTRODUCTION

CCDs with many structures of gate electrode and channel have been developed to provide a high efficiency, high speed and high packing density¹⁻¹⁰⁾. Some practical devices of those structures are put on the market as linear and area image sensors, high capacity memories and analog delay lines.

Those devices require a complicated structure to provide desired functions. It also decreases the packing density and fabrication yield, and therefore increases the cost. For example, line addressable random access memory organizations permit CCDs to provide short access time and a high serial data rates with low power consumption and low drive requirement (11).

The organizations by the conventional structures, however, decrease the packing density due to the space for bus lines, or increase the overlapping of the gate electrodes. Both of them increase the device cost. Another example is a tapped delay line which is useful as a transversal filter. It requires parallel taps along the shift register in order to put in and pick up a signal. The presence of bus lines on both sides of conventional CCDs complicates the structure of taps.

The above mentioned demerits of conventional CCDs concerning the structure are caused mainly by the fact that each line (channel) is constituted by a large number of discrete electrodes and requires bus lines to connect them.

The proposed CCD provides a simple structure which has only two gate electrodes for each line and no need for bus lines.

II. THE CONCEPT

The basic device structure is shown in Fig. 1. The channel is defined by interdigitated channel stops. The gate electrodes, 1 and 2, are parallel to each other, closely spaced and laid over an oxide layer

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covering the channel. The CCD cells are staggered along the device. Every other cell is under electrode 1 and the remainder under electrode 2. Each cell is divided into two parts. The channel layer of the second part is doped more highly than the first part to form a potential well in each cell. When the potential of electrode 1 is lowered, a charge in a cell under electrode 1 is transferred to the next cell under electrode 2. In the cell, the charge moves from the first to the second part and settles in the potential well. When the electrode potential is reversed, the charge is transferred to the third cell under electrode 1. Thus, when clock pulses are applied, the charge moves down the channel switching between two electrodes.

The charge-flow directionality from the first to the second part in each cell, also, can be provided by a stepped oxide.

The proposed CCD can be called "Meander Channel CCD", because the charge is transferred along a meander channel which is defined by interdigitated channel stops.

III. DEVICE FABRICATION

32 bit linear devices with a meander channel were fabricated. A photograph of a fabricated device is shown in Fig. 2. The electrodes are made of stripes of polysilicon and aluminum, and overlap each other to decrease the instability associated with gaps. The substrate used was 10 - 20 ohm-cm p-type (100) silicon. The channel stops were formed by thermal diffusion of boron. Phosphorous ions were implanted into the channel to form a stepped potential in a cell. The doses were estimated to be $1 \times 10^{12}/\text{cm}^2$ and $2 \times 10^{12}/\text{cm}^2$ in the first and second parts, respectively. After removing the oxide layer, a new oxide layer, 1500 Å thick, was grown which is used as a gate oxide. The device was completed by providing the striped polysilicon and aluminum overlapping gate electrodes. The cell size is $30 \times 60 \text{ cm}^2$. One bit element comprises two cells which are staggered along the device.

IV. OPERATION

Fig. 3 shows the minimum potentials under the first and second parts of the polysilicon gate as a function of a gate voltage. The potentials were measured on MOS FETs formed on the CCD chip. The potential difference between the two parts limits the charge capacity. The difference in the device of Fig. 2 was about 10 volts and the charge capacity was about $6.5 \times 10^{11}/\text{cm}^2$ which corresponds to one half of that for a surface channel device.

The fabricated devices were successfully operated in both one and two phase modes. The one phase mode operation is shown in Fig. 4 on the device of Fig. 2. Clock pulses of rectangular waveform were applied to the aluminum electrode and the polysilicon electrode was connected to the earth potential. A 30-volt clock varying between -15 to +15 resulted in satisfactory operation and could handle a charge capacity of about one-third of the implanted level without going into a surface channel mode.

The efficiencies of 99.95 and 99.98 % were obtained at 1 MHz in one and two phase clockings, respectively. The efficiency at higher

frequency was limited by the size effect of cell, which was the same as that of conventional CCDs.

V. DISCUSSIONS

The preliminary experiments of the proposed CCD exhibited that it has performances comparable to conventional CCDs for transfer efficiency, speed and charge handling capacity. The CCD could also be fabricated with a higher yield as compared with conventional CCDs. The reasons are supposed to be due to the simple electrode structure without bus lines for clocking and contact holes for them, less interelectrode overlapping, and large photolithographic tolerance.

The proposed CCD has some important merits other than a high fabrication yield on device organizations for the applications. The features are summarized as follows with some illustrations,

1. In devices constructed of plural lines (tracks or channels), each line can be clocked independently to the other lines by a simple electrode structure and with a high packing density.
2. The direction of line along which a charge is transferred is alterable without crossovers of gate electrodes and/or diffused regions (see Fig.5),
3. Bus lines for clocking are not required for each line.
4. Contact holes for clock lines are not required.
5. Charges can be picked up and put in at any points along the line (see Fig.6).
6. A signal, therefore, can be refreshed at any points along the line by a simple electrode.
7. Overlapping of gate electrodes can be reduced.

These features promise organizations of a line addressable memory of high packing density, a simple line and area sensors, and simple signal processors, with a low cost.

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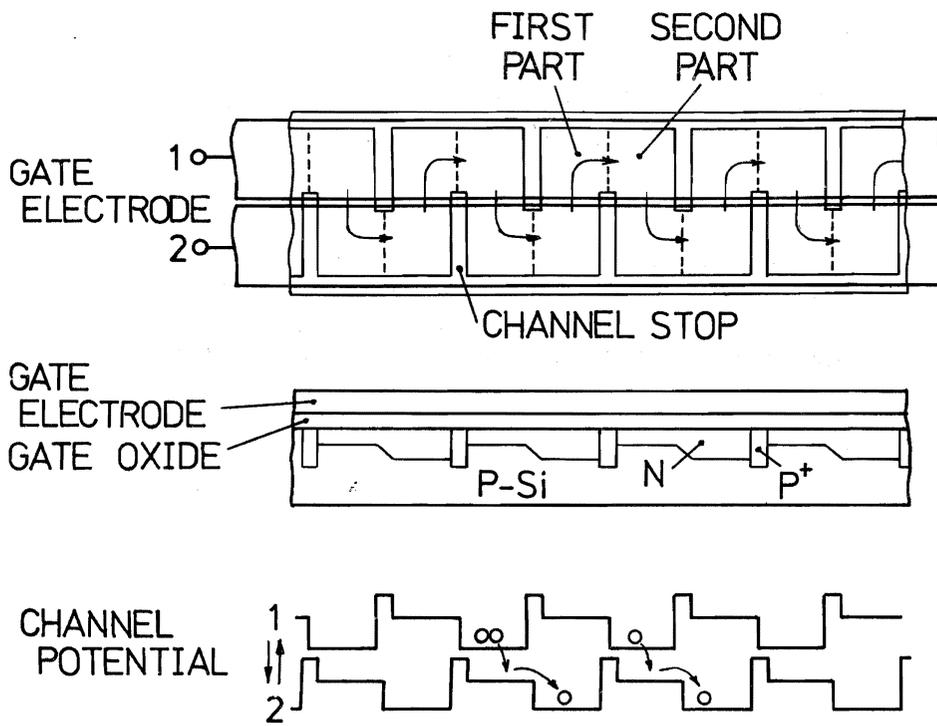


Fig.1 The basic structure of the proposed CCD.



Fig.2 Parts of 32 bit CCD with a meander channel.

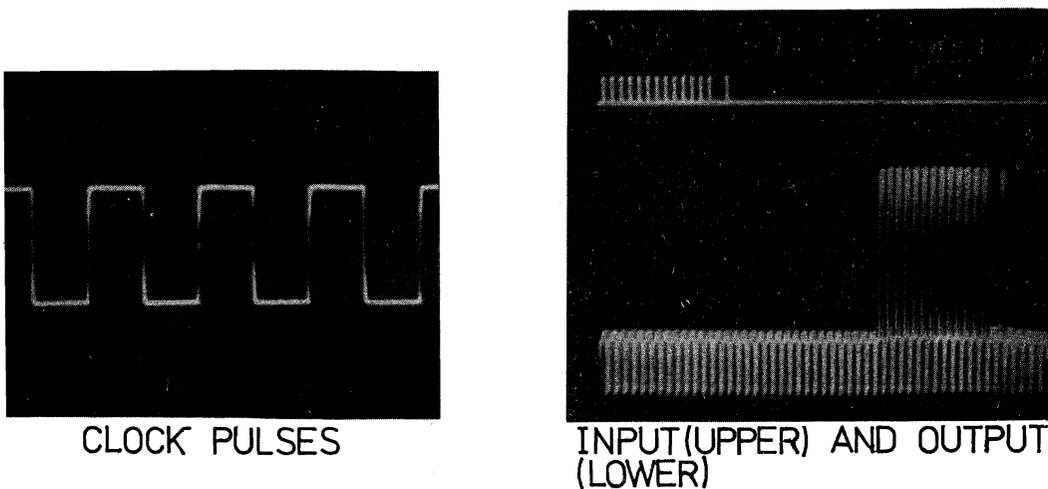


Fig.4 Operation of the fabricated device of Fig.2

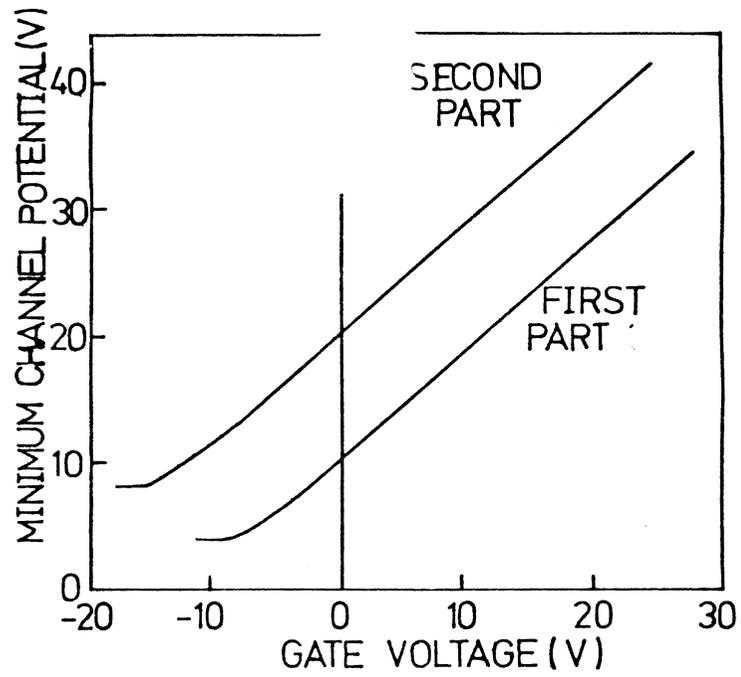


Fig.3 Channel potentials of the first and second parts under the polysilicon gate.

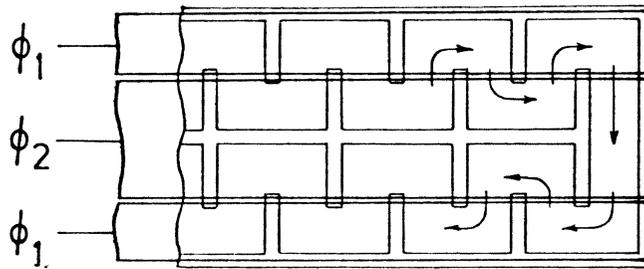


Fig.5 An example showing a reverse of charge flow.

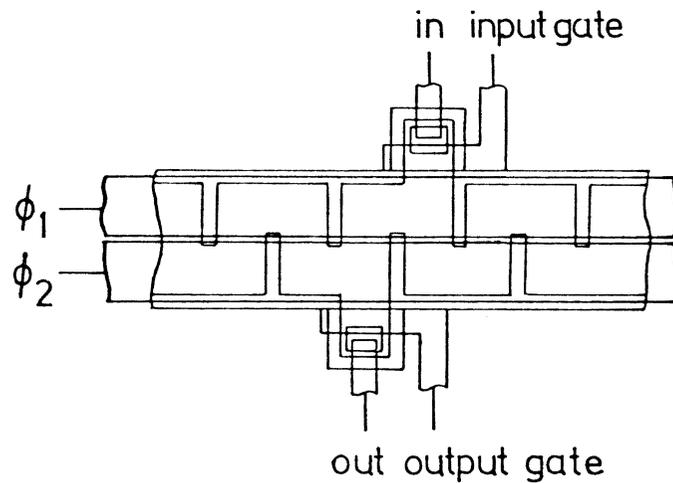


Fig.6 An example of put-in and pick-up of a signal charge.