EVALUATION OF LOW DARK CURRENT CHARGE -COUPLED DEVICES

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ABSTRACT

Surface channel CCD delay lines, analog memories and image sensors are fabricated using a three phase overlapping polysilicon electrodes technology with a gate insulator consisting of 900 Å TCE-SiO₂ and 400 Å Si₃N₄. Growing the gate in an appropriate chlorine containing ambient considerably increases the imaging and analog storage capabilities of these devices. Of great importance is the extremely low and homogeneous dark current which directly influences the photosensitivity and noise of the CCD imager. This paper describes the relation between observed dark currents and the different bulk and surface generation mechanisms.

The measurements which are performed on the CCD in order to characterize the generation mechanisms are : the pulsed capacitance measurements as a function of time, which give the bulk lifetime τ_0 and the surface generation velocity s, secondly direct dark current experiments to obtain the surface generation velocity s_0 of a depleted surface and finally gate controlled diode experiments which give an independent determination of the τ_0 and s_0 parameters.

A typical bulk lifetime τ_0 of 350 μ sec, surface generation velocities s of 0.3 to 0.4 cm/sec and s₀ of about 5 cm/sec are found. This results in a dark current of 5 nA/cm² for normal CCD operation. The number of dark current spikes is strongly reduced.

INTRODUCTION

One of the major problems associated with the fabrication of charge transfer devices is the minimization of the dark current background charge and the elimination of dark current spikes. This is of particular importance for the development of analog CCD memories and of high quality CCD image sensors. Experimental evidence of some relation between these dark current spikes and stacking faults in the silicon material has recently been given by Tanikawa et al. (Ref. 1).

The mechanisms of several gettering techniques are relatively wellknown. Phosphorus gettering is widely used throughout silicon device manufacturing. Preoxidation gettering techniques are now under extensive investigation (Ref. 2,3,4). The increase of minority carrier lifetime during HCl-oxidation has been reported by Robinson and Heiman (Ref. 5). Moreover, Shiraki (Ref. 6) has recently demonstrated the dissolution of stacking faults by using HCl oxidation.

As previously described, the use of an appropriate amount of trichloroethylene (TCE) in the oxidizing atmosphere improves the characteristics of Si-SiO₂ structures, similar to HCl-oxidation, (Ref. 7,8). The purpose of this paper is to prove that the application of the TCE-SiO₂/ Si₃N₄ technology to CCD-processing gives excellent dark current performance by reducing the surface generation rate, by increasing the bulk generation lifetime and finally by strongly reducing the number of dark current spikes.

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HCL?

The measurements which are discussed in order to characterize the generation mechanisms are : first the pulsed capacitance C-t plots, giving bulk lifetime τ_0 and surface generation velocity s of an inverted surface. Secondly, direct dark current measurements on the CCD's are presented yielding the surface generation velocity s_0 of a depleted surface which is of extremely high importance for normal CCD operation. Finally gate controlled diode experiments give an independent determination of τ_0 and s_0 parameters.

CAPACITANCE RESPONSE EXPERIMENTS

All the measurements described here are done on a 64-bit CCD shiftregister. It is an N-type surface channel device, consisting of three overlapping polycrystalline siliconlayers and built with a 900 Å TCE silicondioxide - 400 Å siliconnitride gate insulator. The gate oxide is grown at a temperature of 1100°C. The molar ratio of TCE in the oxidizing atmosphere is around 0.1 %. The CCD has gatelengths of 10 μ m and a channel width of 200 μ m. The substrate is p-type, (100), 15-25 Ω cm material.

In the first set of experiments the CCD was pulsed as a MOS capacitor. The input and output diodes were floating, while the input and the output gates were held in accumulation in order to isolate the diodes from the CCD gate area. All the transfergates were tied together and pulsed from flatband voltage (-1 V) into deep depletion (+15 V). Fig. 1a reveals a C-t plot performed on the CCD. During the transient response thermally generated minority carriers are swept to the Si-SiO₂ interface where they build up the inversion layer. The equilibrium high frequency inversion capacitance is reached after a typical thermal relaxation time of 340 sec or about 5 1/2 min.

The shape of the C-t curve depends on the generation mechanisms and can be analyzed by Zerbst-techniques. This analysis yields a curve which is represented in Fig. 2. The slope of the straight line is inversely proportional to the generation lifetime τ . The intersection of the line on the vertical axis is proportional^g to the surface generation velocity s of an inverted surface (Ref. 9).

The calculations performed on this curve give a surface generation velocity s of 0.33 cm/sec and a generation lifetime τ_g of 700 μ sec. The generation lifetime τ_g is given by equation (1)

$$\tau_{\rm g} = \tau_{\rm po} \exp\left[\left(E_{\rm T} - E_{\rm i}\right)/kT\right] + \tau_{\rm n_o} \exp\left[-\left(E_{\rm T} - E_{\rm i}\right)/kT\right]$$
(1)

where τ_{p_0} and τ_{n_0} are the lifetime of the holes and electrons respectively, E_i^{-1} is the semiconductor intrinsic energy level and E_T is the bulk generation-recombination energy level. For recombination centers with an energy level at midgap and if we assume the capture cross sections σ_p and σ_n the same, we find a bulk lifetime $\tau_0 = \tau_{p0} = \tau_{n0}$ of 350 μ sec. In this paper and for reasons of convenience we will refer to a bulk lifetime τ_0 in accordance with previous assumptions, although we know from other experiments that the recombination lifetime can be about a factor of 10 less than the here defined bulklifetime.

The average dark current found from the C-t response is 1.3 nA/cm^2 . It is interesting now to compare this experimental value with the dark current components as given by the generation parameters found from the Zerbst-analysis. The contribution of the bulk generation and surface generation current can be calculated from the following expressions :

$$I_{bulk} = q n_i (W - W_F) / 2 \tau A / cm^2 : bulk component$$

 $I_{surf.} = q n_i s A/cm^2$: surface component

Inserting the τ_0 and s-values in the simple expressions for bulk and surface generation yields a bulk component of 0.65 nA/cm² and a surface component of 0.63 nA/cm² respectively. In these formulas q is the electron charge, n_i the intrinsic carrier concentration equal to 1.2 x 10¹⁰ cm⁻³, W_F is the width of the depletion layer in equilibrium and W is the average width of the depletion layer during the C-t response.

In order to demonstrate the effect of the surface generation velocity s_0 of a depleted surface, C-t plots are recorded for one phase of the CCD, the two other phases being held in depletion or accumulation. Fig. 1 gives three different C-t responses measured on the same CCD. The figure at the top is given as a reference, it is the previously discussed response when all the phases are pulsed together, resulting in a thermal relaxation time of 340 sec.

The C-t plot 1 of Fig. 1b is recorded when only one phase of the CCD is pulsed while the two other phases are held in depletion (O V). A considerable smaller storage time of 32 sec is now found. This reduction indicates that the surface has a strong influence on the carrier generation. As reported in the literature (Ref. 10) longer storage times can be obtained by holding two phases in accumulation (-6 V), while the third one is pulsed. This response is represented by curve 2 of Fig. 1b. This gives a storage time of 180 sec. This value is not so high as the one measured with all the gates pulsed together because of the fact that small portions of the surface between the accumulation and inversion layers are still in depletion, where an enhanced surface generation rate exists.

CCD DARK CURRENT EVALUATION

Another set of results is obtained by direct CCD dark current measurements on CCD's operating in respectively the low frequency mode and the integration mode. In these experiments the voltage is measured at the output of the on-chip preamplifier. Our maximum charge packet, which is determined by the high level of the clock and a DC-gate at the output, consists of 5.2 pC. The top curve of Fig. 3 shows the output voltage of the CCD when the device is clocked at very low frequencies. This output which is entirely due to dark currents is plotted versus the equivalent integration time T , which is the time spent by each charge packet in the shift register. Each output charge packet corresponds to the sum of the dark current contribution generated under each electrode. Saturation is reached after 12.5 sec. The bottom curve represents the output when the CCD is operating in the integration mode : the clocks are stopped, one phase remains at the high level (15 V) and the other two remain at the low resting level (3 V). This response illustrates how a charge packet in a given bit position grows as a function of the integration time T_{int}. The linear slope of these curves proves our previous assumption that a constant generation (q $n_i s_o$) at the depleted surface gives the greatest contribution to the dark current. According to the method described by Dewitt G. Ong and R. Pierret (Ref. 11) one can calculate from these results, a surface generation parameter s_0 of 5.4 cm/sec.

The surface generation velocity s_0 is proportional to the product of the density N_{SS} of fast surface states and their capture cross section. Independent transfer loss measurements on two differently processed wafers give N_{SS}-values of 7 x 10⁹ and 2.0 x 10¹⁰ cm⁻² eV⁻¹ respectively. Fig. 4 shows the transfer loss of the first "one" as a function of the number of zeros preceding that first "one". The difference in ϵ and N_{SS} is due to different annealing techniques. Dark current measurements however indicate that s_o decreases in a smaller degree than N_{SS} does. This gives some indication that the capture cross section increases slightly as N_{SS} decreases.

The saturation time in the integration mode can be considerably enhanced by holding the non-integrating electrodes in accumulation, as was also done in the C-t experiment. The resultant output voltage versus integration time curve is depicted in Fig. 3b. Curve 1 represents the output when the non-integrating electrodes are in depletion and curve 2 gives the output when holding the non-integrating electrodes in accumulation. The shape of curve 2 indicates that the bulk generation give a considerable contribution to the dark current. The saturation time increases from 13.5 sec up to 59 sec. This corresponds to a dark current of 1.5 nA/cm², averaged over the whole CCD gate area. It should be remarked that this saturation time is not so large as the thermal relaxation time of 180 sec measured on the C-t plots because the maximum charge packet in the CCD is smaller during the dark current experiments.

The minority carrier bulk lifetime is also determined from the gate controlled diode measurements. All the CCD electrodes are connected together and the input and the output diode are biased at the same reverse potential. The leakage current of the diode is measured as a function of the gate voltage applied to the electrodes. Fig. 5 gives a representation of the measurements. Calculations give a bulk lifetime of about 300 $\mu \rm scc$ (Ref. 12). The gate controlled diode experiment normally gives both bulk lifetime and surface generation velocity $\rm s_{o}$. However the drop in the curve due to the surface generation component is too small to explain the so value found during the dark current measurements. This is due to the fact that a great portion of the surface is weakly inverted during the gate controlled diode experiments (Ref. 13), which results in a strongly reduced surface generation. Pierret gives a correction factor which allows us to calculate the correct surface generation rate. The value of $\rm s_{o}$ deduced from this method is 5 cm/sec.

DISCUSSION

A fairly good agreement is obtained between the results of the different experiments. A bulk lifetime τ_0 of 300-350 µsec is derived from both the Zerbst-analysis and the gate controlled diode experiments. Surface generation velocities of 0.3 - 0.4 cm/sec for s and 5-6 cm/sec for s₀ are found. These high bulk lifetimes and low surface generation velocities result in a dark current of about 5 nA/cm² for normal CCD operation. When holding the non-integrating electrodes in accumulation, dark currents of 1.5 nA/cm² are obtained.

It must also be emphasized that the number of dark current spikes has been strongly reduced by this process. As an **example** we show first the dark current output of a CCD, having a high number of spikes (Fig. 6). By the use of etching techniques we were able to find a 95 % relationship between dark current spikes and stacking faults.

This means that the stacking faults were found on exactly the same place as the spikes, observed during CCD dark current experiments. By an optimized TCE oxidation and an excellent control of the various annealing treatments an extremely low and very uniform dark current could be achieved. Fig. 7 gives a typical CCD dark current output, corresponding to about 40 % of a full charge packet and obtained at room temperature

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after an integration time of 7 sec.

It has to be pointed out that these results are very well reproducible which makes the TCE-SiO₂/Si₃N₄ technology suitable for the fabrication of low noise imaging devices and of analog processing structures where long storage times are required. Preliminary results on a 256-bit linear imaging array and on a 128 x 18 bit analog SPS-memory will be presented. Operation of these devices at room temperature with integration or storage times of 100 msec and with a dark current contribution of only 1 % of a full charge packet seems achievable in the near future.

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Voul (V) 3-Fig. 3a 2 1 5 10 Tint (sec) \cap 10 5 (clock (Hz) Vous (\mathbf{V}) 3 Fig. 3b 2 1 Tint (sec) 20 40 60

<u>Fig. 1</u>: C-t plots of the CCD : (a) all the gates pulsed; (b) phase 1 pulsed with phase 2 and 3 in depletion (1) or in accumulation (2). $T = 23^{\circ}C$.

Fig. 3 : CCD dark currents : a) low frequency mode b) integration mode. $T = 25^{\circ}C$



Fig. 2 : Zerbst plot derived from Fig. 1a.











Fig. 6 : CCD-dark current output after integration time of 3 sec. Hor. : 100 usec/dev.; Vert. : 1V/dev. V_{max,out} = 2.8 V.



Fig. 7 : CCD-dark current output after integration time of 7 sec. Hor. : 50 usec/dev.; Vert. : 0.5 V/dev. V max,out = 2.8 V.