THE USE OF PLASMAS IN CCD PROCESSING

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ABSTRACT

Any semiconductor devices including oxide layers in its structure is susceptible to degradation in processing, many such problems being associated with mobile charge in the oxide layers, interface states, etc. In particular, devices using active oxide layers, CCDs being the most relevant of these for the purposes of this conference, can be rendered unusable by subtle processing problems.

Plasma processing in various guises is becoming more popular, in the form of sputter-deposition and sputter-cleaning in particular. Sputter deposition is one of the easier ways to deposit refractory gate materials, RF sputter cleaning (either in a system using external RF excitation or one using sputter electrodes in the plasma) offers the advantages of an "in-situ" cleaning process. RF sputter-systems have also been touted as an ideal photo-resist removal method, and indeed, this is one of the few ways to remove photo-resist residues.

These processes have, however, subtle problems associated with them. Several such problems will be discussed in this paper. These include fixed and mobile charge redeposition processes, heavy metal contamination and ion-burial processes, and some subtle dielectric breakdown processes which may occur in certain plasma systems. Suggestions for "cures" will also be made.

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RADIATION EFFECTS IN CCD PROCESSING

Charge Coupled Devices, in common with other devices using oxide layers as part of their structure depend upon the excellent interface properties of the SiO_2/Si interface for their successful operation. Interface fixed charge of the order of 2×10^{11} cm^{-2} or less, and interface state densities of 10^{10} cm^{-2} or less, together with low values of mobile contaminant ions are required for most devices using active oxides; CCDs are particularly susceptible to high interface state density (N_{SS}) and of course to non-uniformity in flatband voltage (V_{FB}). It must be borne in mind of course, that usually on any chip including CCDs will be found other devices in input and output circuitry, usually MOS devices, which are also susceptible to the factors mentioned above. The objective of a good oxide processing technology is to (i) minimize the interface state density of the MOS or CCD devices, (ii) have a stable oxide with minimum mobile contaminant level and "slow trapping" instability and (iii) have a stable value of turn on voltage ie a flatband voltage certainly less than 2 volts (on 1200Å gate oxides say). Conventional processing ie straightforward chemical deposition of polysilicon layers, thermal evaporation of aluminium layers, with precautions ensuring low contaminant level in processing usually leads to appropriately low values if N_{SS}, V_{FB} and mobile contaminant levels (Q mobile). Newer technologies, such as the use of plasmas in processing, can lead to high values of interface state density, fixed charge and mobile charge in oxide films, and leave residual effects, even after the apparent annealing out of high values of these parameters, which can subsequently render processed devices useless.

It might first be appropriate to summarize the uses of plasmas in CCD device processing, and indicate the types of plasma systems either in use or proposed. Plasma processing has two basic purposes viz (i) removal of material (some sort of "sputtering" "cleaning" or "backsputtering" operation) and (ii) deposition of material, ("forward sputtering" "sputtering" or "sputter deposition"). The former is used in several applications, in removal of photoresist or photoresist debris, where it is known as "ashing" or "plasma etching" and in substrate "in situ" cleaning prior to a metallization step, for example. The latter, sputter deposition, is primarily employed in deposition of metal layers, particularly refractory metals which are difficult to deposit by other means. "Reactive sputtering" is also used in deposition of compound materials such as tantalum-silicon for example, where the plasma excitation is used to cause chemical interactions between the gaseous material and the substrate. This principle is also used in many "plasma asher" systems, where oxygen or halogen-containing electronegative gases are employed.

Problems in devices primarily arise when bare oxide films are exposed to the plasma environment. It has been known for some years that SiO_2 films on silicon are grossly affected by exposure to a plasma environment (ref 1). It is only relatively recently that mechanisms for these degradation effects have been explained in any detail (refs 2-5).

The interaction between a plasma and a surface has to a large degree been thought of over the years in macroscopic terms. Parameters such as "wall potential" ie the potential which is reached by the wall of a plasma system in equilibrium due to the ambipolar diffusion of ions and electrons in the plasma, and the ion and electron "temperatures" ie energies have been measured and documented (see eg ref 6). In the interaction of a plasma with a solid, however, it is not necessarily the macroscopic parameters which are of most significance in the subsequent behaviour of the surface, particularly if the surface is that of an insulating film. The macroscopic effects such as wall potential build-up may influence such effects as film dielectric strength in sputtering or backsputtering, but the microscopic effects of ionized and neutral particles and electrons in their interaction with the solid may dominate the substrate properties subsequent to the plasma exposure.

The macroscopic effect which dominates is that of wall potential since it determines the ion and electron energies at the substrate, and the gross potential which is reached by the surface of an oxide film in a plasma. Figure 1 shows the effects of backsputtering on oxide films 1000Å thick in a low voltage triode system whose wall potential is of the order of 30-40 eV. Regions of gross dielectric breakdown may be observed, where weak points have occurred in the oxide. When such breakdowns occur, large areas of charge over the surface discharge through the breakdown region, leading to gross damage. The damage effects occurring in this way are determined by oxide thickness (refs 2, 5, 7) since the potential which an oxide film can sustain is determined by its thickness, ie at a given oxide field strength (up to 8-9 x 10^6 V cm^{-1}) the potential at the surface is determined by thickness. A 1000Å SiO_2 film can sustain 40-90 volts, depending on weak points but a 5000Å oxide may sustain up to 450 volts or so (see eg ref 2 (b) for a detailed example). Thus care must be taken in backsputtering and plasma exposure of thin films to ensure that the breakdown voltage of the oxide film is not exceeded.

In the case of sputter deposition under conditions such that the oxide surface may charge to an appreciable voltage, there is an additional mechanism which may cause gross breakdown effects. As the oxide surface becomes conductive, as metal is deposited on it, any localized breakdowns (as photo in figure 1) may cause the charge over the <u>entire</u> slice to be discharged through such regions, leading to non-annealable breakdown pheonomena, giving metallization to substrate shorts. It is clear in Figure 1 (b) that the area around the gross breakdown spots is clear of defects showing how all the charge in that region discharged itself through these spots. Contrast areas not showing gross breakdown (Fig 1 (a)) where uniform effects may be observed. It should be emphasized that Fig 1 (a) and (b) shows gross effects, under conditions calculated to show those effects to advantage.

The microscopic effects are those of ions, electrons, neutral atoms (metastable and ground state) and photons, and the effects of these particles in combination. That the individual particle interactions are of prime importance is shown by the recent work of McCaughan and Kushner refs (3-5, 7, 8) and that of Powell and Derbenwick (ref 19) which demonstrates that ion-insulator and photon-insulator processes dominate the plasma-solid interaction. It has been demonstrated that (i) ion bombardment of SiO_2 films by ions of various species leads to increased interface fixed charge, oxide mobile charge and interface states, as well as dielectric breakdown effects, even at very low ion doses and energies, (ii) neutral atom bombardment leads primarily to interface state build-up (ref 10) (iii) electron bombardment at low energies leads to interface state and fixed charge increases but not to significant mobile charge effects (ref 11), and (iv) photon bombardment also gives increased interface state and fixed charge increases and low mobile charge effects (ref 9 and 12). What is significant in plasma processing is the effect of these species in combination. It might be thought, for example, that ion-oxide interactions might be irrelevant when oxides are maintained at a negative wall potential in a plasma so that electrons are available at the surface for neutralization. RF sputtering of SiO_2 indeed depends on this kind of principle. An assymetric RF voltage is applied to an SiO_2 film on silicon, the idea being that the electrons follow the RF signal (if of high enough frequency, $\approx$ 500 khz), while the ions follow the RF average DC potential (negative) and thus sputter off material from the surface. The electrons would thus neutralize the effects of the ions or "neutralize" the surface (ref 13). One would assume then that RF sputtering of 500Å of material from a 500Å thick sample would remove surface contaminants. In fact it does not. McCaughan and Kushner showed (ref 3) that if 4×10^{11} cm^{-2} NaCl containing ^{22}Na was deposited on the surface of an SiO_2 sample, and 500Å were removed from the sample by RF backsputtering, the contaminant, rather than being removed, was driven into the oxide to the interface, Figure 2. This is exactly the same effect as is observed by simple ion bombardment (ref 8). Similar effects are found in RF sputter deposition (ref 14). It has also been observed that contaminants from the surrounding metalwork or other samples can be redeposited on plasma-exposed samples (refs 3, 15). The explanation is relatively simple. Let us assume the average negative DC potential in such an RF backsputtering experiment is 100 volts. Then approximately 4×10^{12} electrons per cm^2 are required at the surface to maintain that potential. The sputtering rate in such a system is of the order of 200Å/minute ie approximately 2×10^{15} atoms per second are removed. The interaction time for the Auger and Resonance processes undergone by these ions at the surface is of the order of 10^{-14} to 10^{-15} sec, and the neutralization processes at the surface are fairly localized (refs 4, 7, 8). Thus the probability that an ion will interact with the surface at a region where an electron already resides is very low. Hence the effects of the ions from the plasma on the oxide properties will not be greatly affected by the presence of the electrons. This has been demonstrated in independent experiments (ref 10). Thus plasma exposure and RF backsputtering in particular, is hazardous to device stability, certainly if annealing temperatures of less than 750-800°C must be used subsequently. The deleterious effects of ion bombardment on the mobile charge level in oxides can, fortunately, be removed by high temperature annealing ($\approx$ 900°C), (ref 2(b)).

Another effect of ion bombardment is interface state production, as also is true of energetic neutral atom bombardment (which can occur in plasma systems, ref 16). An example is given in Figure 3 (ref 10). Here an SiO_2 film was bombarded by 10^{15} cm^{-2} N_2^o at 2 KeV under conditions where positive self-bias at the surface existed (ie if any mobile positive charge were so produced it would have gone to the interface and caused a lateral voltage shift; such did not occur). Here the interface state density produced is greater than 10^{13} cm^{-2} eV^{-1}. Similar effects are shown under ion bombardment, Figure 4, even when phosphorus glass passivation is used to prevent ion transport effects (ref 17). Interface state effects anneal out easily, fortunately for CCD device exposure to plasmas, annealing temperatures of the order of 450°C or so being sufficient in every case, (refs 2, 10, 17) to remove such degradations completely. Electron bombardment at low energies can cause both interface charge and interface state effects (ref 11), figure 5. Again these effects may be annealed out at temperatures below 500°C. Photon induced interfaced states and charge also anneals out at similar temperatures.

It thus appears that, for CCD devices, plasma exposure may not pose too many problems in interface state and interface fixed charge production since these may be annealed at relatively low temperatures. Problems may arise from the mobile charge effects, however, since some of these are subtle and hard to spot. Bias temperature stressing, using the quasistatic C-V method for detection, may be revealing (ref 2 (b)). If the ramp itself is used for biasing the device at elevated temperature and quasistatic C-V curves taken immediately on cooling the device, transient effects are observed (Figure 6). The charge in these devices (mobile at room temperature) would not have been detected using the conventional bias stressing methods employing H/F C-V curves. This mobile charge effect is removed by elevated temperature annealing, or may be prevented by phosphorus glass passivation of the oxide film subsequent to the plasma exposure.

Information on the effects of negative ions on MOS devices is sparse. Hughes et al (ref 18) have shown that energetic O^- ions do not cause the ion mobilization processes that O_2^+ ions give. This is exactly as predicted by McCaughan (ref 19). Low energy negative ions would thus be expected to give rise mainly to interface state increases which would anneal out.

We may conclude then that plasma exposure of bare oxide films used subsequently as the gate dielectric of MOS transistors may be hazardous to their electrical properties unless high temperature annealing can be utilized to remove the mobile contaminant and subtle bias-temperature stress instabilities; the interface states would be easily annealable at low temperatures. CCD devices may be more tolerant of mobile contaminant level and no problem with interface states should exist. Indeed the common usage of phosphorus glass passivation and phosphorus gettering steps in processing may fortuitously protect oxide films against the mobile charge problem and allow easy annealing of plasma degradation at temperatures less than 500°C. In other cases "fixes" for the systems such as magnetic field protection of the substrates (refs 5, 15) or grid systems (ref 5) may be necessary.

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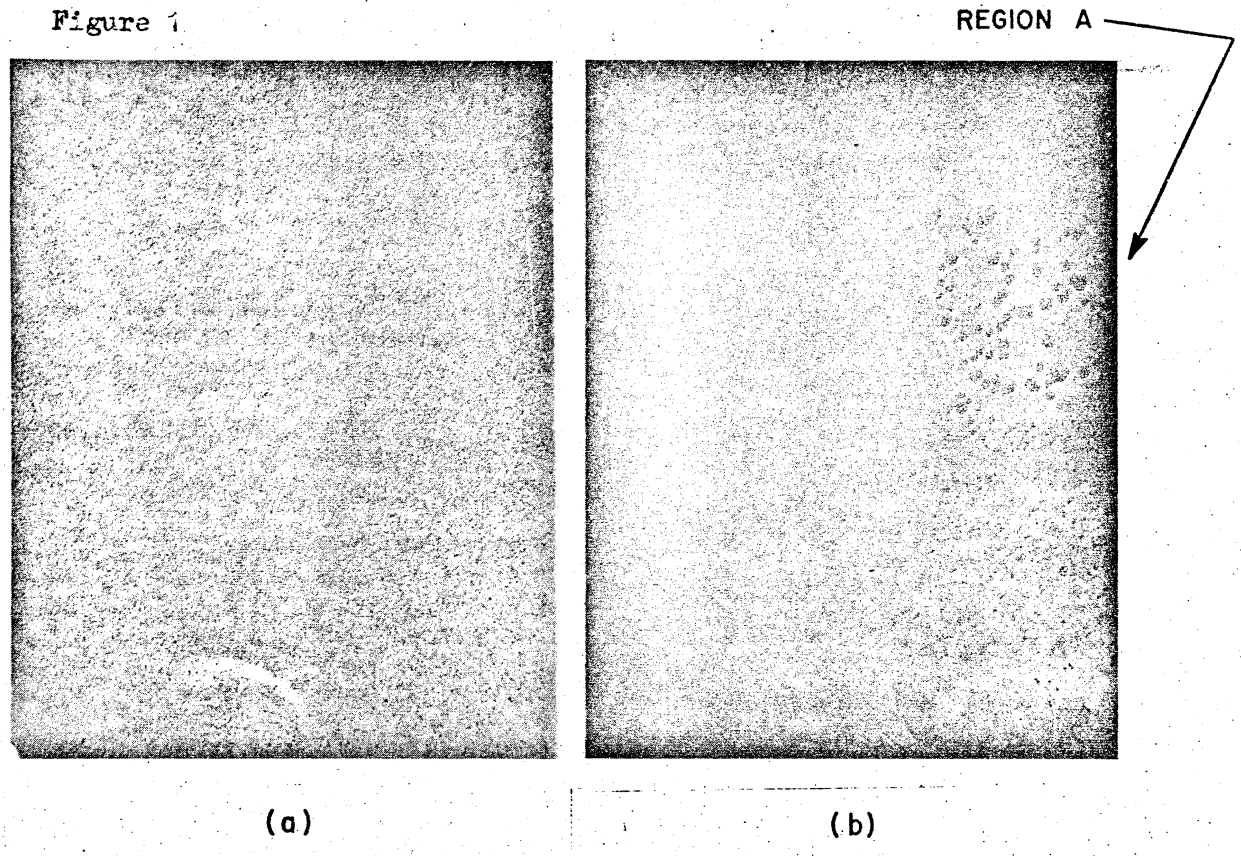
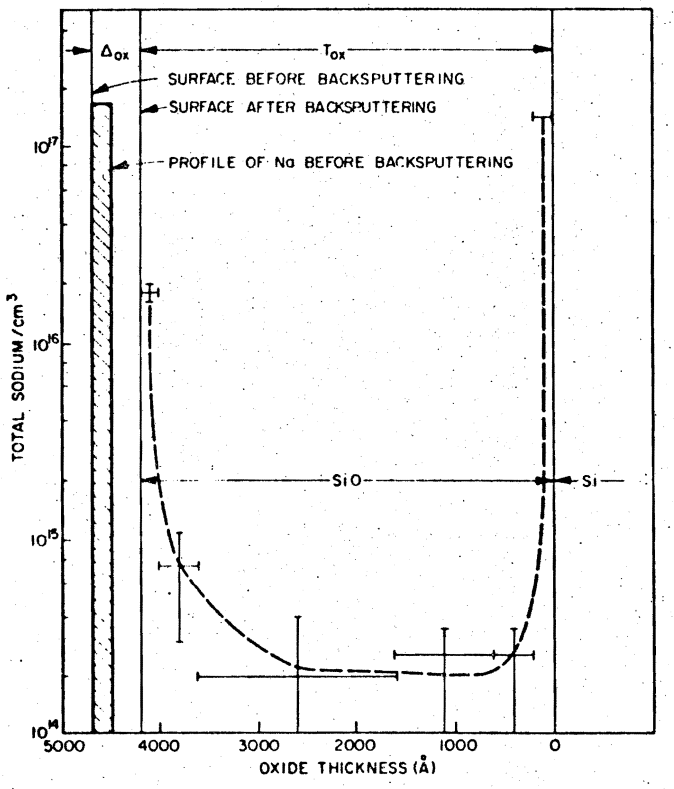
Figure 1



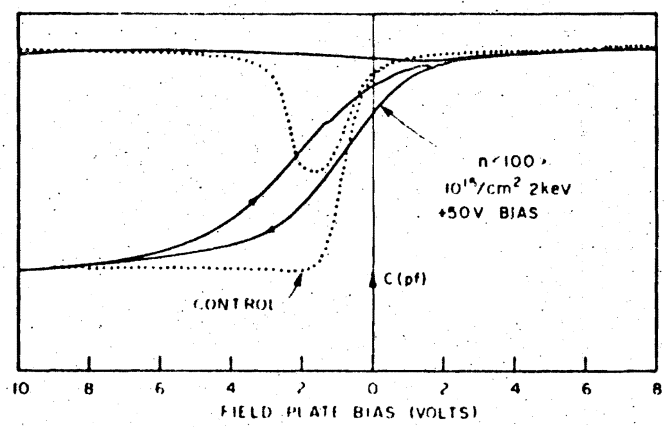
Dielectric breakdown effects over the surface of a thin SiO_2 film exposed to a low pressure plasma having high wall potential, (a) uniform breakdown effects (b) localized breakdown effects at a defect area (region A)

Figure 2



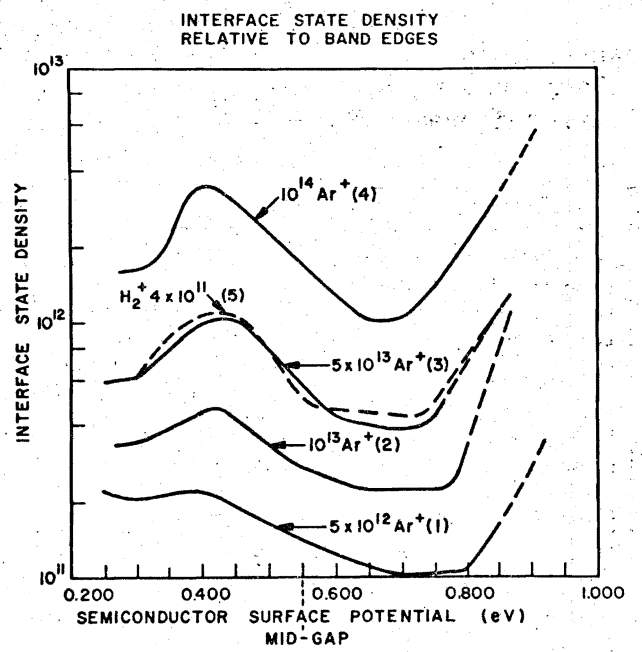
Profile of Sodium in SiO_2 before and after rf backsputtering. All the sodium is initially on the outside surface of the oxide. Note that most of the sodium is transferred to the SiO_2/Si interface by the backsputtering

Figure 3



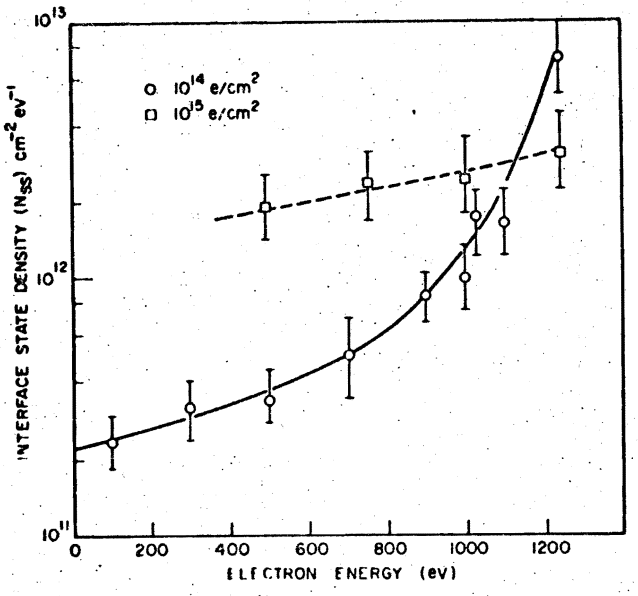
C-V Characteristics of SiO_2/Si Slices subjected to N_2^o (2000 eV) bombardment with a positive (50 volt) Bias applied to the collector (ref 10)

Figure 4



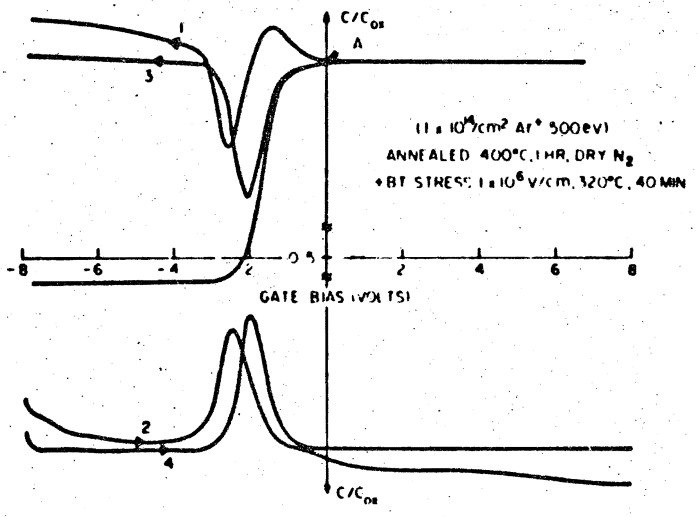
Interface states produced in PSG passivated samples. Curves (1) - (4) show N_{ss} for 5 x 10^{12}, 10^{13}, 5 x 10^{13} and 10^{14} Ar^+/cm^2, respectively. Curve (5) shows similar values for unpassivated SiO_2 bombarded by 4 x $10^{11}/cm^2$ H_2^+ ions (ref 17).

Figure 5



Effects on interface state density N_{ss} of low energy electron bombardment on SiO_2 films at 10^{14} and 10^{15} e cm^{-2}.

Figure 6



Effect of 400°C anneal in dry N_2, showing room-temperature mobile species after B-T stress, giving current superimposed on quasistatic C-V curve, The capacitance scale is really a current scale; the differences between curves 2 and 4 are, therefore, ionic currents in the insulator. Curves 3 and 4 are the quasistatic C-V curves without ionic components, and are reached after several cycles, ie, the ions are trapped at the electrodes (ref 2 (a)).