NON-VOLATILE CCD-MEMORY WITH MNOS CAPACITORS

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ABSTRACT

The volatility of information stored in a Charge Coupled Device (CCD) can be avoided by storing the information in MNOS capacitors added to a CCD. In the following the function, the layout, and the measured results of test circuits are described and different layouts of such memory circuits are discussed.

INTRODUCTION

Charge coupled devices (CCD) (ref.1.) like nearly all MOS memories, have the disadvantage of volatility. The volatility problem can be overcome by transferring the information from the CCD to the MNOS capacitors (refs. 2,3,4). The layout of the prototype circuit and results obtained are described.

STORING IN MNOS CAPACITORS

In this new device, the MNOS storage capacitors, connected to a common address line, are placed beside a CCD array so that they are related to the CCD electrodes of the same phase line. Schematic cross-sections of the CCD and of the MNOS capacitors are shown in Fig. 1, in which the charge distributions during the read-write cycles are indicated for the following limited conditions: (i) with an inversion layer under the electrode of the CCD, (ii) with a depletion region only (Fig. 1a).

For write-in, a high negative voltage is applied to the electrodes of the MNOS capacitors (Fig. 1b), so that the existing carriers are transferred from the CCD to the MNOS capacitor according to the same principle as in CCD (ref. 1). Only those MNOS capacitors to which carriers are transferred have their threshold voltages shifted.

The shift of the threshold voltage of a MNOS capacitor largely depends on the amount of charge under the metal electrode. Where an inversion layer exists, the capacitance is large, and where it does not exist it is small (the ratio of the capacitance values between both cases is about 1:5 using a substrate with a resistivity of 10 ohm.cm). This means that, the voltage being the same, the electrical field in the gate insulator of the MNOS capacitor is high in the first case, and it is low in the second case (for the given example the field strengths also have a ratio of about 5). The operating range of the threshold voltage versus the applied gate-field hystersis loop (ref. 2) is chosen so that when the field is high, a large shift of threshold voltage will occur and when

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the field is low, there will be little or no shift. Thus the signal in the CCD can be stored in the MNOS capacitors, by means of a shift or no shift in the threshold voltage (Fig. 1c). This action however, requires that the time taken for storage is short so that the number of positive carriers being created in the depletion region by thermal generation is negligible. Generally this condition is met since the time constant to form an inversion layer from thermal generation is of the order of seconds; otherwise there would be a shift of threshold voltage in all MNOS capacitors.

For read-out of the information, the voltage at the address line is chosen so that in an MNOS capacitor with high negative threshold voltage only a depletion region is formed, whereas that with a low threshold voltage only an inversion layer is formed (Fig.1d). The formation of the inversion layer can be accelerated if the carriers are delivered not only from the thermal generation but also from the CCD. By applying a high phase voltage at the electrodes of the CCD and by reducing the voltage at the address line of the MNOS capacitors the charge in the inversion layers is transferred from the MNOS capacitors to the CCD (Fig. 1e). In this case however, the stored information is inverted in comparison to the state during writing (Fig. 1b and c).

EXPERIMENTAL RESULTS

A micrograph of a test circuit representing a CCD with thirteen electrodes and three MNOS capacitors is shown in Fig. 2. For improving the transfer properties of the p channel CCD realised in a standard Al gate technique the gaps (6 um wide) between the electrodes are implanted with boron (ref. 5). The gate dielectric in the CCD is a Si_3N_4 layer about 50 nm thick and a SiO_2 layer of the same thickness, the gate dielectric in the MNOS capacitors consists of the same Si_3N_4 layer and an additional SiO_2 layer about 2 nm thick.

The experimental results are shown in Fig. 3. In addition, the waveform of the pulses on the address line are shown in the sequence of write-in, reclear, read-out and erase. The signals are shown for the following three cases:

- The input signal appears at the output before a write pulse is applied (Fig. 3a), so that no information is stored during write-in and therefore no output signal appears during read-out.
- The input signal is shifted from the input to the third electrode of the first stage and then stored in the first MNOS capacitor S_1 during write-in. After reclear the stored information and output signal are observed at the third sample during read-out (Fig. 3b). This part of the output signal is shown in a larger scale (Fig. 3d).
- The input signal is very low, so that no charge is fed in and therefore no shift of threshold voltage at the first MNOS capacitor S_1 occurs during write-in. During read-out no output signal appears as in the first case (Fig. 3c and e).

These experimental results confirm that the proposed CCD with MNOS

capacitors operates as expected.

CONCLUSION

This memory circuit allows a storage system which combines the advantage of the high packing density of a CCD with the advantage of non-volatility of MNOS circuits. In the example mentioned above this advantage is, however, achieved by the expense of reduced packing density, since the MNOS capacitors are placed beside the CCDs. This arrangement has the advantage that the information stored in the MNOS capacitors is not degraded by the pulses applied to the CCD without this advantage the CCD capacitors can be combined with the MNOS capacitors, so that nearly the same packing density is attained as in usual CCD arrangements. There are two possibilities to do this. Either every third of the CCD capacitors is made of the MNOS type and the phase line to these CCD electrodes is also used as an address line or the MNOS capacitors are placed in the gaps between the CCD electrodes using an address line in a second layer about the CCD electrodes.

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FIGURES

Figure 1

Schematic cross-sections of the CCD with MNOS capacitors for the two different cases. At the beginning (a) there is an inversion layer below the CCD electrode (left) and there is no inversion layer (right).

a) Starting point
b) The charge is transferred from the CCD to the MNOS capacitors.
c) Due to the charge the electrical field is high in the gate insulator, without charge it is low.
d) For reading an inversion layer is only induced if the taps are neutral.
e) The charge is transferred back from the MNOS capacitors to the CCD.

Figure 2

Photomicrograph of a realised CCD circuit with MNOS storage capacitors S_1, S_2 and S_3.

Figure 3

Experimental results measured at the circuit in Fig. 2 and the waveform at the address line.

a) The input signal (above) appears at the output (below arrow) before write-in.
b) The input signal is stored in the first MNOS capacitor and appears during read-out (arrow).
c) The input signal is too low, no output signal appears during read-out (arrow).
d) Part of the output signal (Fig. 3b) in a larger scale.
e) Part of the output signal (Fig.3c) in a larger scale.

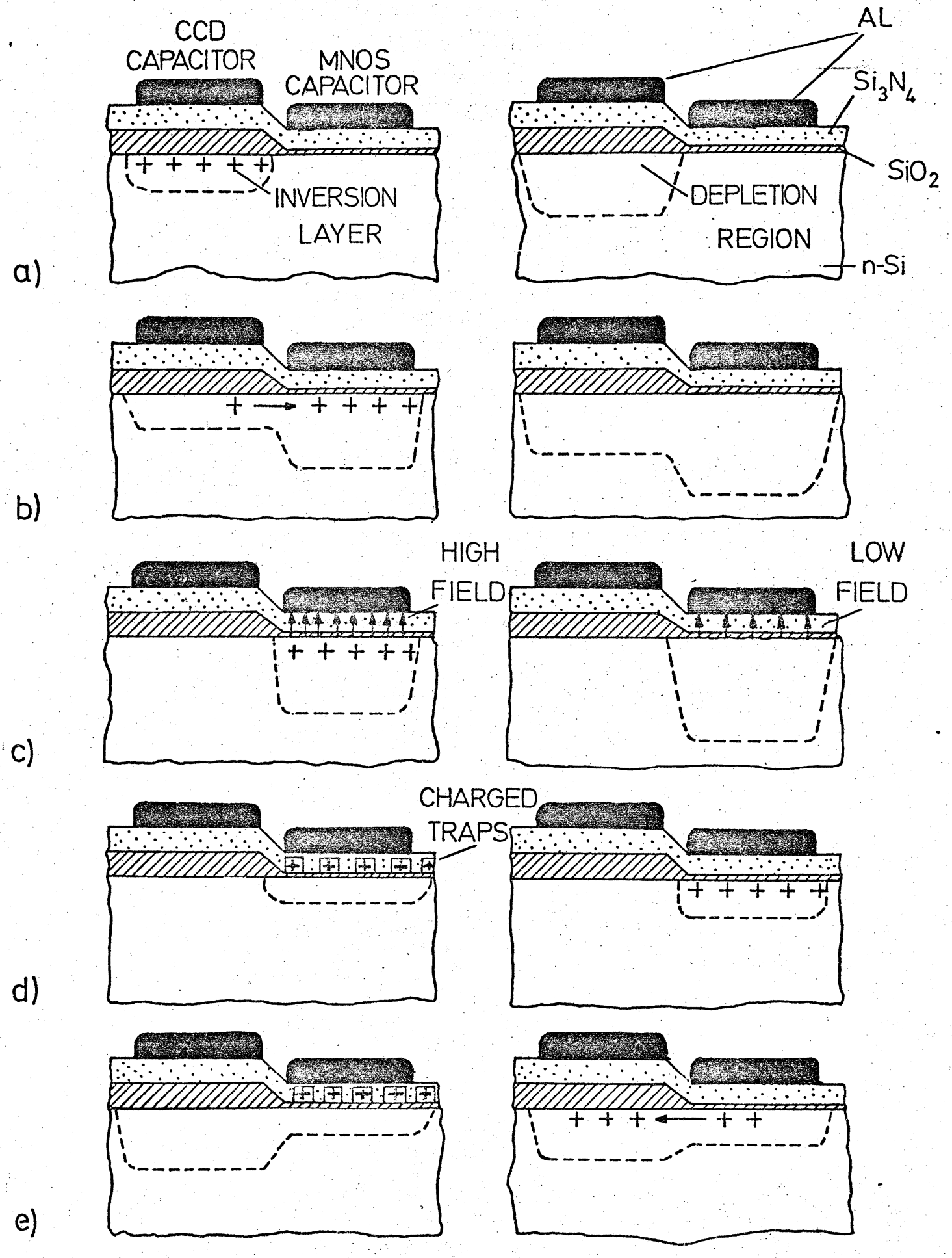
CCD
CAPACITOR
MNOS
CAPACITOR
INVERSION
LAYER
AL
Si_3N_4
SiO_2
DEPLETION
REGION
n-Si
a)
b)
HIGH
FIELD
LOW
FIELD
c)
CHARGED
TRAPS
d)
e)

FIG 1

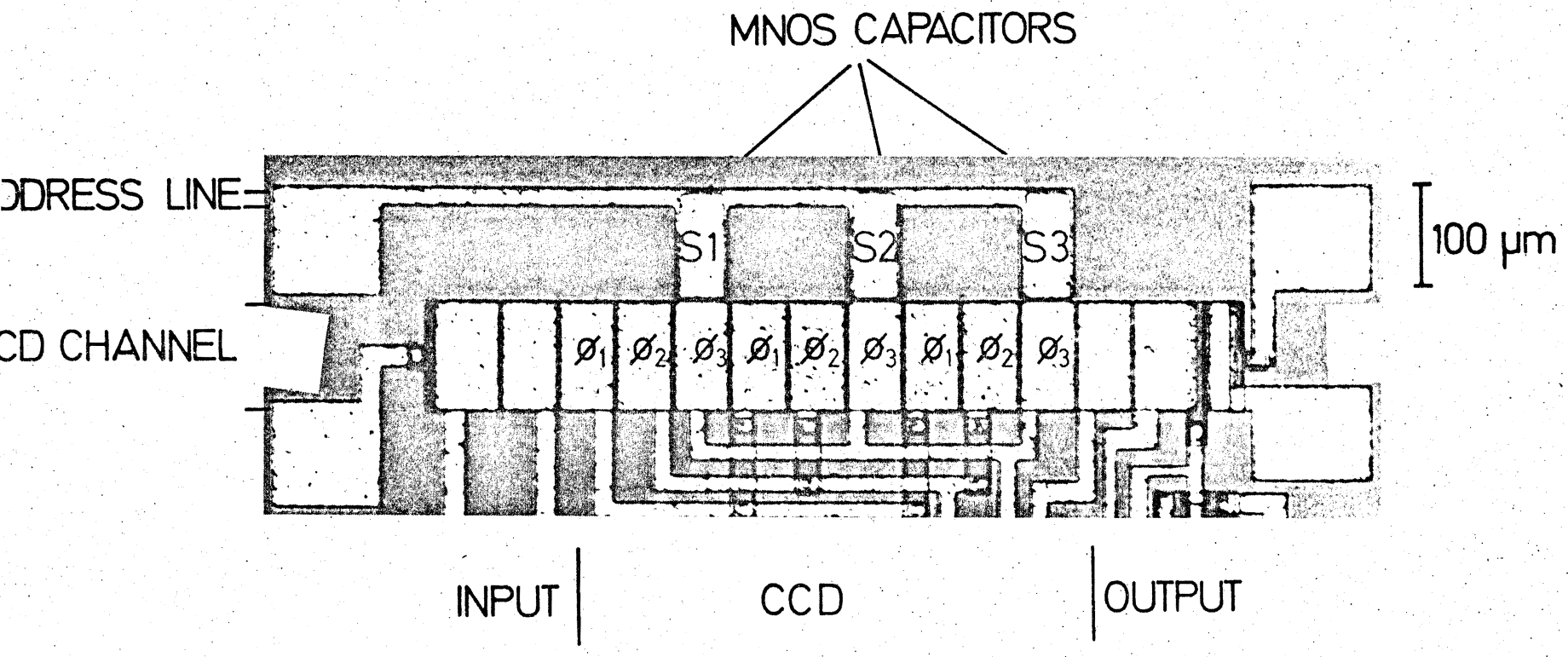
MNOS CAPACITORS
DDRESS LINE
CD CHANNEL
S1
S2
S3
100 µm
Ø1 Ø2 Ø3 Ø1 Ø2 Ø3 Ø1 Ø2 Ø3
INPUT
CCD
OUTPUT

FIG. 2

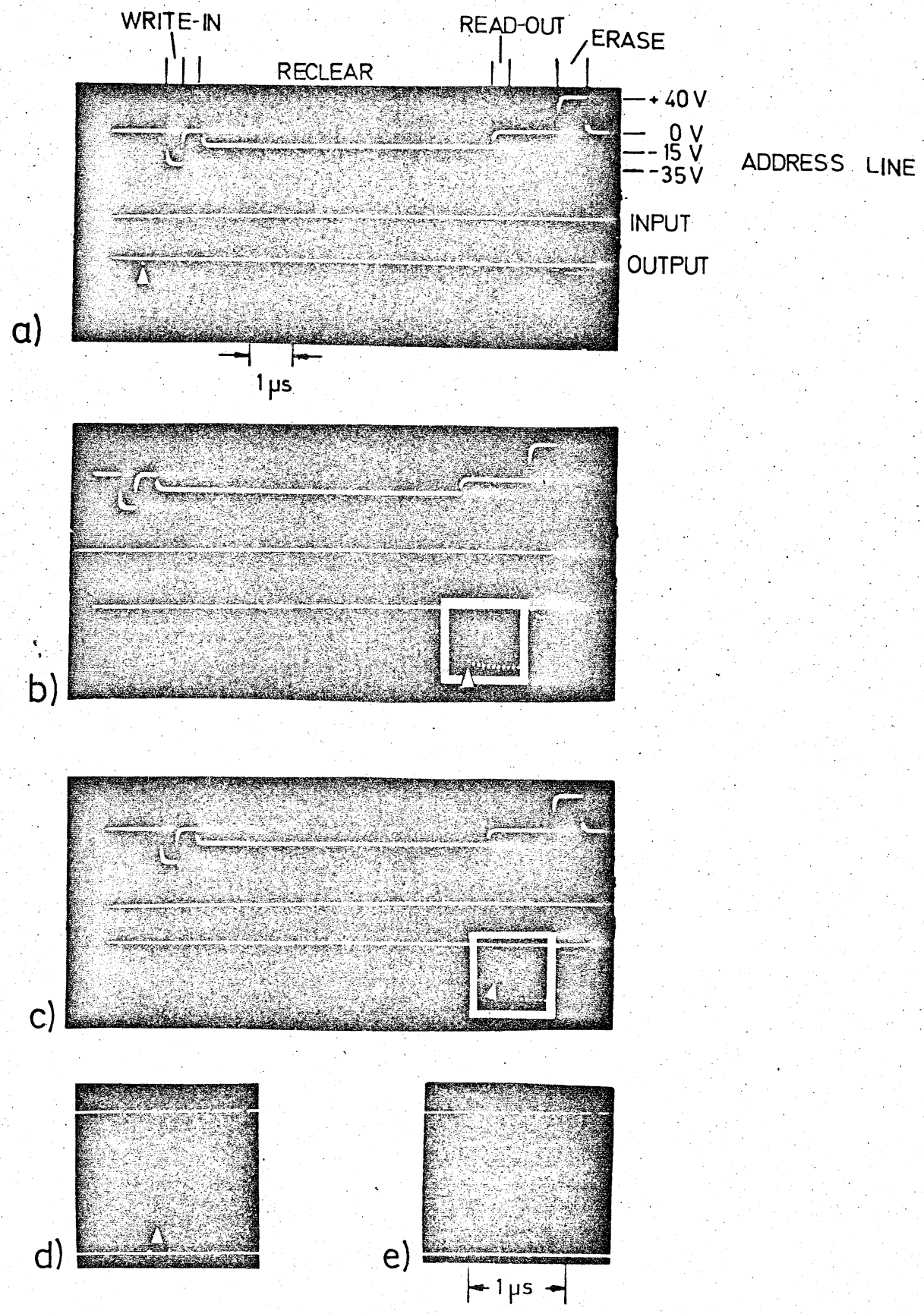
WRITE-IN
READ-OUT
ERASE
RECLEAR
+40 V
0 V
-15 V
-35 V
ADDRESS LINE
INPUT
OUTPUT
a)
1 µs
b)
c)
d)
e)
1 µs

FIG. 3