A CCD ON GALLIUM ARSENIDE

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ABSTRACT

A novel form of charge-coupled device based on gallium arsenide is proposed. The device is of the buried channel type, employing reverse-biassed Schottky barrier electrodes and a stepped-surface two-phase structure. By using the preferential etching properties of the (100) face of GaAs zero gap, automatically isolated electrodes are obtained, overcoming a major problem of more conventional buried channel structures.

1. INTRODUCTION

One of the major problems involved in the development of the charge coupled device since its introduction in 1970 has been the difficulty of obtainting narrow inter-electrode gaps reliably with conventional photo-lithographic techniques. This paper describes a technique by which this problem may be overcome by taking advantage of a preferential etch on GaAs which gives self-aligned, self-isolating electrodes with practically zero inter-electrode gap. Furthermore, the structure of this device allows two phase operation to be obtained very simply.

2. DEVICE STRUCTURE

The proposed device is to be a two-phase, buried channel structure fabricated on GaAs using Schottky barrier electrodes. The use of GaAs imposes several technological limitations compared with silicon, including the difficulty of making diffusions and of growing oxides. The latter difficulty means that the usual MOS capacitor electrode structure cannot be used, hence the decision to use reverse-biassed Schottky barriers. This has the disadvantage that the Schottky barrier leakage current injects charge into the channel, and so the minimum clocking frequency is determined by the time taken by this leakage current, integrated over the transit time of the device, to take up an unacceptable proportion of the charge storeage capacity at the output. This is expected to be about two orders of magnitude worse than a conventional silicon CCD, which is limited in a similar manner by thermal generation.

In avoiding the use of diffusions, two problems arise:- Firstly, the conventional diffused input and output contacts cannot be used. Instead it is proposed to use Ni-Au-Ge ohmic contacts, as is common practice in GaAs FETS. Secondly, there is the problem of lateral channel confinement, usually achieved by "channel-stopping" diffusions. It is proposed to overcome this problem by the use of a Schottky barrier guard ring (fig 1) The aluminium Schottky barrier is buried in the epitaxial layer, totally encircling the device. To allow contact to be made between the electrodes and the external clock rail, the surface of the guard ring is anodised. Channel confinement is then achieved by applying sufficient reverse bias

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to pinch-off the epitaxial layer under the guard ring.

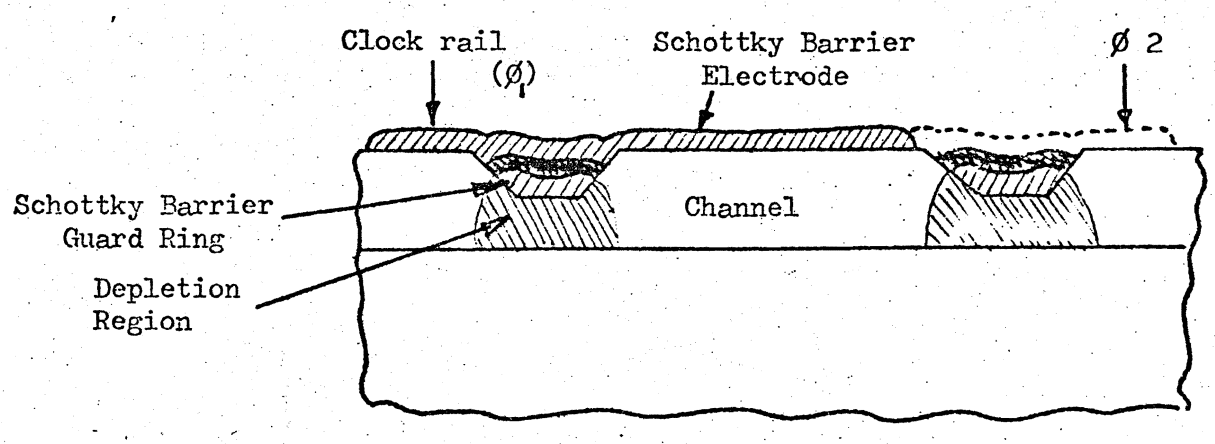

FIG 1: SCHOTTKY BARRIER GUARD RING

Inter-electrode isolation is achieved by making use of a preferential etch which undercuts correctly aligned lines on (100) surface GaAs at an angle of about 45° (fig 2) while in the perpendicular direction shallow sloped edges are obtained. Although the specific directions in the lattice in which these preferentially etched planes lie have not been identified at this stage they can be identified for the purpose of alignment on a particular slice by means of a trial etch: sloped edges show up as broad lines when viewed from above (fig 2) while undercut edges show up as fine lines.

To define the electrodes, a stepped structure is formed by conventional photoengraving, aligned so that the edges of the steps are undercut. Aluminium is then evaporated over the entire area to form the Schottky barrier electrodes, using the float-off technique to define the ends of the electrodes. Providing the metal thickness is less than the step height, then 'shadowing' due to the undercutting ensures that the electrodes are isolated from each other (fig 3)

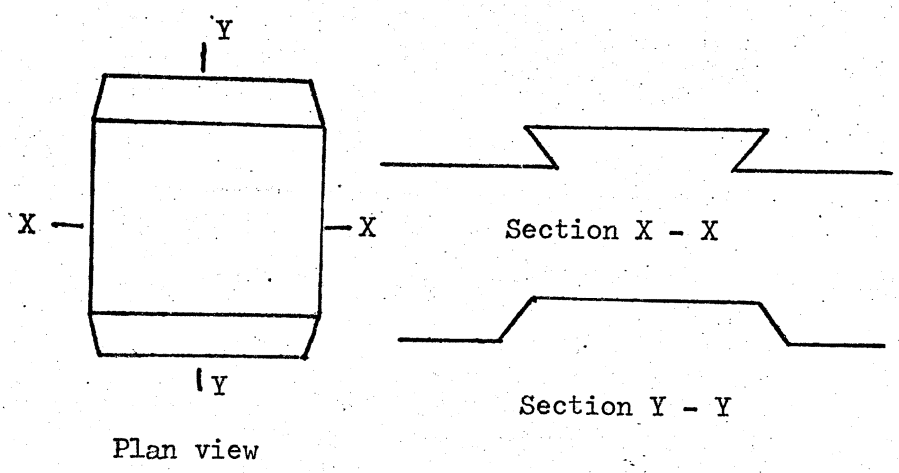

FIG 2: PREFERENTIAL ETCH PROFILES

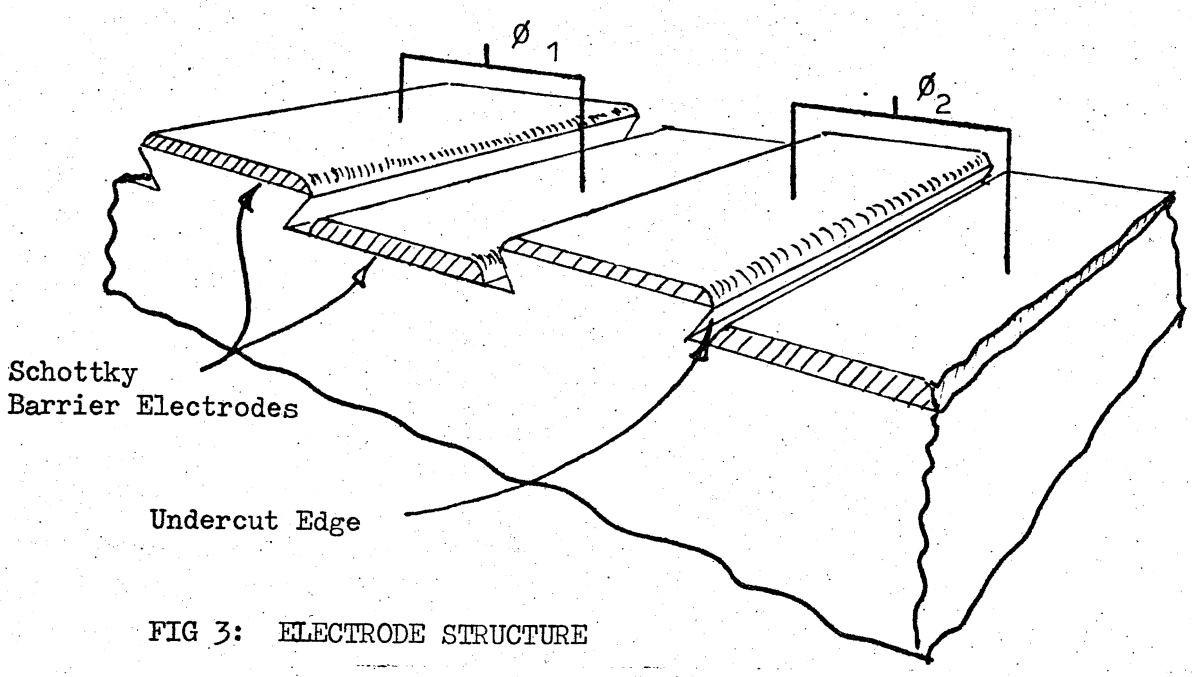

FIG 3: ELECTRODE STRUCTURE

Idealised one-dimensional plots of potential variation with depth under the centres of the electrodes of a device with a 2 μm n-type epitaxial layer with $N_D = 5 \times 10^{15}$ cm^{-3} and p-type substrate with $N_A = 1 \times 10^{15}$cm^{-3} are shown in fig 4 for 0v and 10v gate potentials.

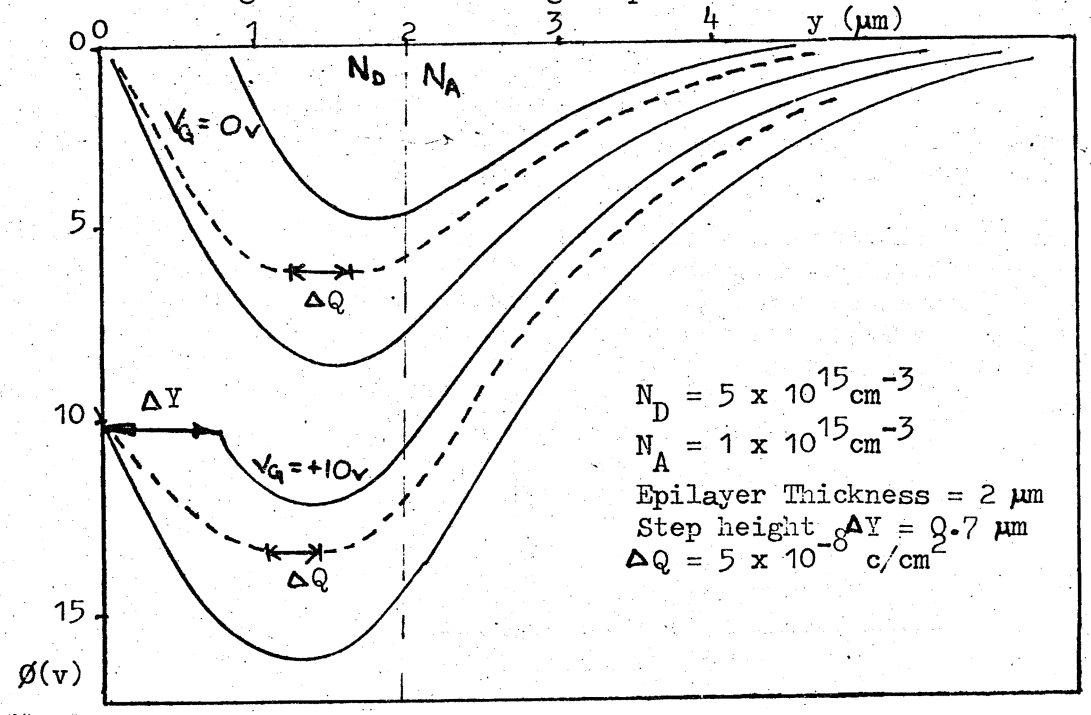

FIG 4: VARIATION OF POTENTIAL (Ø) WITH DEPTH (Y)

The epitaxial layer is initially assumed to be totally depleted, and then the effect of introducing 5×10^{-8} C/cm^2 of charge into the channel is calculated. Note that with 0v on the gate and no stored charge the 'high' Schottky barrier electrode is under an effective reverse bias of about 8v and that this reverse bias is reduced both by the application of positive voltages on the gate and by the introduction of charge into the channel.

The clocking sequence is illustrated in fig 5, which gives the approximate variation of potential along the device. Note that the 'low' electrode

. provides the blocking potential which gives the two-phase action, and charge is stored under the 'high' electrode - the reverse of stepped-oxide two-phase structures.

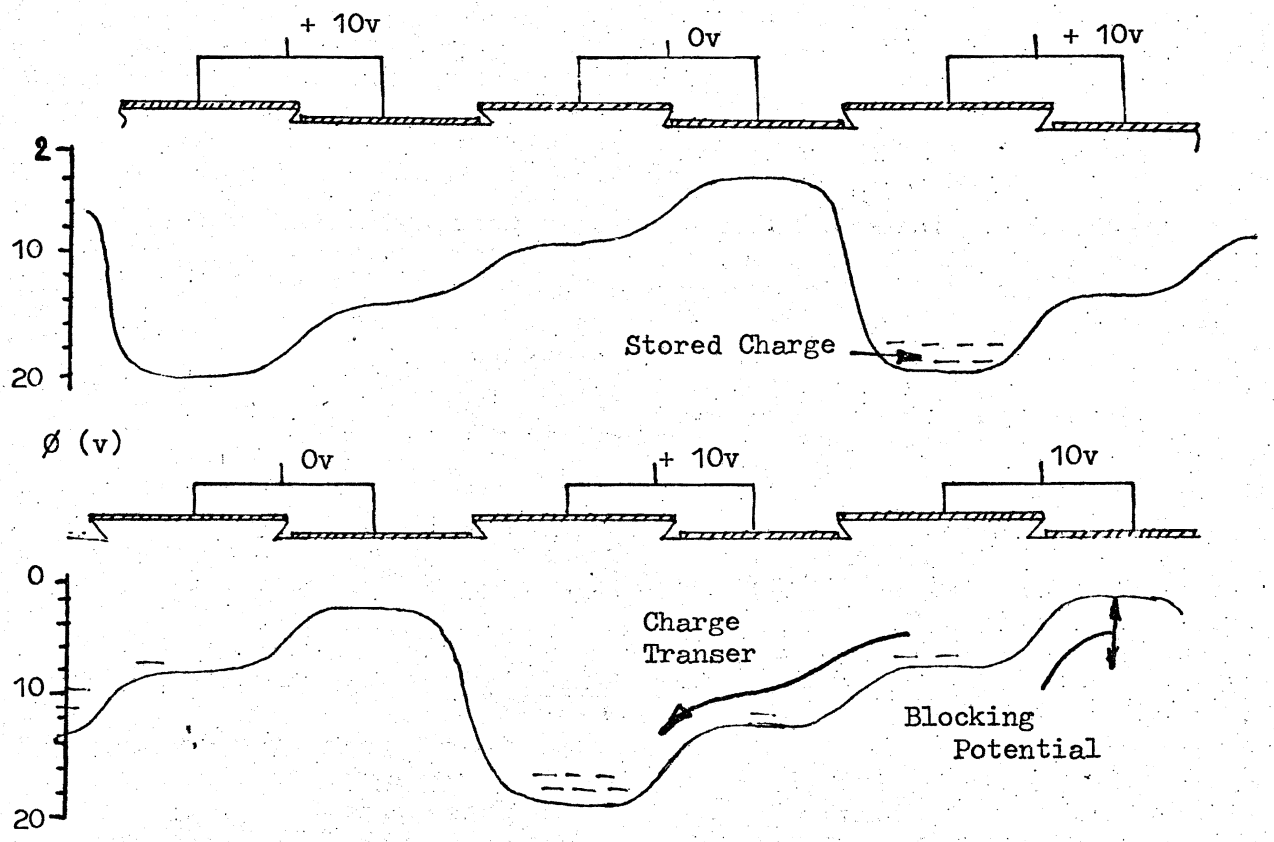

FIG 5: CHARGE TRANSFER PROCESS

SUMMARY OF IMPORTANT PARAMETERS OF GaAs CCD

Doping density:	$N_D = 5 \times 10^{15}$ cm^{-3} $N_A = 10^{15}$ cm^{-3}
Epilayer thickness:	2 µm
Step height:	0.7 µm
Schottky barrier reverse voltage (max)	8.3v
Charge capacity:	5×10^{-8} C/cm^2
Clock voltage swing:	10 v

CONCLUSIONS

A technique for the fabrication of a CCD in GaAs has been presented. Principal features of this device are the use of Schottky barrier gate electrodes in contrast to the usual MOS structure; a method for obtaining self-aligned, self-isolating electrodes with the added bonus of a simple two-phase structure; and the use of an anodised Schottky guard ring for channel confinement.