FUTURE DEVELOPMENTS IN CHARGE COUPLED DEVICES

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ABSTRACT

Factors such as commercial confidentiality and a poorly developed technique in clairvoyance limit this exercise in prediction to a fairly conservative approach. Potentially useful but difficult applications are used to illustrate the progress in technology, design and theoretical understanding necessary in order to meet the likely device requirements. Examples are taken from the three main application areas, imaging, signal processing and memories.

INTRODUCTION

Charge Coupled Devices have reached the most critical stage in any new device or system development, the transition from the research to the production environment. Research programmes have been conceived and sustained on the basis of the brilliant simplicity of the original idea, the rapid increases in array sizes and the potentially wide range of applications. Customers in the market place are not so easily persuaded to part with their money by these arguments which have been used to convince research managers. Their requirements are more definite, they want devices which are easy to use and which reliably meet certain specifications at a low cost; most of all, they want to be convinced that products based on CCD's can create new markets or be competitive in existing ones.

A CCD development programme will require close-co-operation between the research, production and system design areas. It is likely that many devices will be custom designed, to make maximum use of the flexibility of CCD operation, and there will only be a small range of standard circuits. Another already existing trend likely to be extended by CCD's is for system and product production to take place within the device manufacturer's organisation; in medium volume markets there is more profit to be made from selling systems than just devices. In the near future then much effort will go into identifying markets for CCD based systems and to developing devices with the required parameters. Therefore most of the future research work will be directed towards supporting the production areas.

The particular demands placed on the research and development team by production requirements can be summarized as:-

(1) Development of a high yield/low cost technology.

(2) Improvement in device parameters, such as, transfer efficiency, dark current, linearity etc.

(3) Establishing long term reliability particularly in hostile environments.

(4) Integrating peripherals on the CCD chip such as input linear compensation circuits, output amplifiers and clock drivers.

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(5) Establishing better theoretical models so that an improved understanding is obtained of both device and system operation.

(6) Devising new system techniques and device structures to take advantage of the data handling flexibility of CCD's.

Beyond this work there will be a body of research devoted to examining more exotic CCD structures, eg using other semiconductor materials. Also undoubtedly CCD research will continue to evolve new devices which can no longer be termed CCD's because they do not depend on the charge transfer process; an example here is the charge injection device (Ref 1).

Considering the various application areas, some likely future device requirements can be identified and we can discuss the progress necessary in the research areas in order to realise these structures in production.

IMAGING

This application area has received most attention in CCD research and not surprisingly it is imaging arrays that are the first CCD's to become available commercially. To highlight future research topics three different imaging array types will be considered:-

(a) Standard TV array

(b) Low-light level imaging Array

(c) Infra-red imaging array

Standard TV Imaging Array

The initial market for this array will be the replacement of the vidicon in TV cameras for broadcasting, security surveillance, industrial process control, facsimile transmission, traffic control etc. Here the aim would be to exploit the hoped for advantages in terms of small size, low power consumption, improved reliability and low cost. Other market areas could open up for a low cost and portable camera particularly if it could be combined with a cheap, portable video recording system (yet to be invented!).

The array parameters will vary from one application to the next depending on TV format, required resolution etc. Table 1 lists a possible array specification which could be aimed at.

The development of very large chips will raise a number of serious problems. Starting with mask making, it is not possible at present to produce arrays of these dimensions using a single step and repeat process. The typical maximum chip size produced by a modern step and repeat camera is 0.75 cm x 0.75 cm, less than one quarter of the area of a likely large imaging array. It will be necessary, therefore, to develop accurate photo-composition techniques where large arrays are composed in the camera using perhaps four or six different reticule plates to provide different parts of the array.

A common objective in both mask making and photolithography processes will be the reduction of random faults, in particular any faults which might produce pinholes in the thin oxide region. In large area CCD's about 90% of the chip area will be thin oxide covered by metal electrodes, it is not possible to permit a single short circuit, through a pinhole, and still produce reasonable picture quality. Those of us who have used large area

capacitors for C-V plots know that it is quite possible to grow pinhole free oxides. In producing CCD's the main problem is to avoid introducing pinholes during post-oxidation processing, particularly the contact hole etching stage. Using negative resist, pinholes can result from any dark spots on the mask; with positive resist, holes in the emulsion will have the same effect. Particles in either photoresist can result in oxide faults. It is virtually impossible to eliminate such faults completely in the normal simple photoresist processes.

Imaging elements	500 x 500
Total array size	1000 x 500
Dimensions (frame transfer)	2.0 cm x 1.0 cm
Transfer inefficiency	$\sim 1 \times 10^{-4}$
Operating frequency	Output array 7.5×10^{6} Hz
	Store array 1.5×10^{5} Hz
	Image array 3×10^{5} Hz
Uniform dark current	$< 4 \times 10^{-9}$ Acm^{-2}
Power consumption	< 1 W
Interlace facility	
Anti-blooming facility	
Temperature stability	

TABLE 1

Two methods being tried at GEC, Hirst Research Centre are the double exposure and double photoresist techniques. In double exposure two separate identical masks are used to expose the same resist twice, hopefully random particles on the mask do not coincide and so are eliminated. The effect of resist particles is not reduced however. In the double photoresist process, the photolithography is performed first using a negative resist (say), then a positive resist is spun on top and the process repeated using the opposite type of mask.

It may be that even the use of modified photolithography processes such as those described will not be enough to eliminate oxide faults entirely. The development of production techniques based on such instruments as the laser pattern generator or the scanning electron microscope might prove economical and necessary for very large arrays.

Two important parameters in imaging arrays are transfer efficiency and dark current. Their effect on picture quality can be seen in Fig 1. Poor efficiency produces smearing effects whilst non-uniform dark currents result in bright spots around the array. As we have heard in a number of papers at this Conference, under the best conditions it has proved possible to achieve both the inefficiency value of $\sim 1 \times 10^{-4}$ and the dark current of

$< 4 \times 10^{-9}$ Acm^{-2} specified in Table 1. However a major problem in large arrays will be maintaining these values uniformly over the whole of the chip area.

Two of the parameters which characterize dark current are lifetime τ (bulk states) and surface recombination velocity, So (surface states). In order to obtain dark currents of $< 5 \times 10^{-9}$ Acm^{-2} it is necessary to have $\tau > 200 \times 10^{-6}$s and So < 4 cm s^{-1} (Ref 11), at present these limits are beyond what can be obtained after processing in production. High lifetime, $> 500 \times 10^{-6}$s, starting material can be obtained but it is found that this average figure is degraded in processing to values of $10 - 100 \times 10^{-6}$s and the reasons for this are not completely understood. In addition dislocations can be formed by thermal stresses during the high temperature processing, and metal precipitates can accumulate during the chemical processing, these features can act as localised centres giving much lower values of τ than the degraded average. Some research is in progress using such techniques as x-ray topography, electron microscopy etc. to study the formation and location of these defects and to correlate the information with electrical results. This is obviously an area of research which will receive considerable attention in the future since the attainment of uniformly low dark currents without cooling will be a difficult task.

With the present 20 volt, truncated waveforms used to drive CCD's the power required by the clock drivers would be nearer 6 - 10 W than the figure of <1 W quoted in Table 1. The development of CCD structures which can utilise low voltage sine wave drive is a desirable aim to reduce power requirements and this would also permit the tuning out of the reactance presented by the CCD electrodes.

Low Light Level Imaging Array

This type of device is obviously aimed mainly at military requirements, although there could be some commercial applications eg night time security surveillance systems. Devices to be used here require ideally all the parameters listed in Table 1 but in addition the ability to process the signal levels of 10^{-12} Acm^{-2} or less obtained under starlight conditions. In this case to give a reasonable signal/noise ratio the noise levels need to be of the order of $10^{-13} - 10^{-14}$ Acm^{-2}.

Some progress has already been made, with front face imaging, by using signal processing techniques to extract small signals from fixed dark current background levels several orders of magnitude greater than the signal (Ref 2). This approach will require considerably more research into characterizing the various noise sources in CCD's (Ref 3) and developing both the technology to limit the effects of these sources, and the output signal processing to extract the wanted signals from high levels of fixed pattern noise.

A further technique being considered is back face electron injection of the signal. In this imager the input light pattern is focussed onto a photocathode and the emitted electrons are accelerated and injected into the back of a thinned silicon slice ($10 - 20 \times 10^{-4}$ cm). If the back face of the slice is suitably treated to give a low surface recombination velocity, electron amplification of the signal can occur by avalanching in the silicon to give a gain of $2 - 3 \times 10^3$. Such an amplification, if it can be achieved without serious loss of resolution due to charge spreading, will obviously alleviate the signal/noise problems considerably. There are several areas of technology and theory which need to be tackled in

developing such an imager, for example:-

(a) Thinning techniques to produce uniformly thin silicon slices without introducing defects. The imaging regions need to be selectively etched to avoid thinning under bonding areas etc.

(b) Experiments to see if electron injection is possible without increasing bulk trap or surface state densities by electron or x-ray damage.

(c) Provision of a low surface recombination layer on the back, after thinning.

Infra-Red TV Camera

Applications in the field of industrial control, medical electronics etc could utilise an imager sensitive to infra-red, but the main impetus is again likely to come from military requirements. There are two approaches to this type of imager, one uses the infra-red sensitive material as part of the CCD structure and in the other separate detectors are multiplexed using a parallel-serial CCD array.

Steckl, Nelson and French have already outlined some of the problems encountered when an infra-red material is used in place of Silicon. Growing insulating layers on these materials with low interface state densities is difficult but by no means impossible provided care is taken in low temperature annealing. As an alternative, as Hughes et al describe later, a buried channel structure removes this problem.

The presence of large dark currents in IR materials is a more formidable obstacle to their adoption.

The dark current $I \propto \frac{n_i}{\tau}$

where n_i is the intrinsic carrier concentration and $n_i \propto \exp\left(-\frac{E_g}{2KT}\right)$

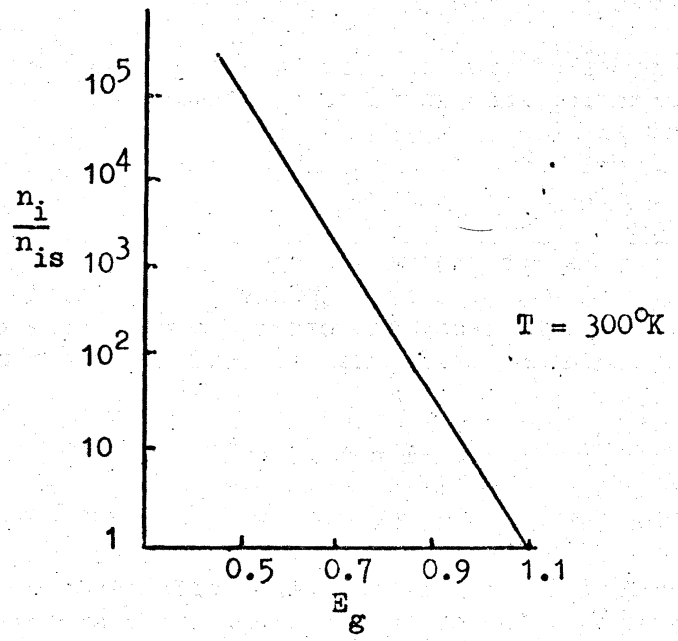

Fig 2

Figure 2 indicates how the intrinsic carrier concentration, normalised to the silicon level varies with band gap energy (E_g) assuming that the density of states, etc are the same.

Increases in I also arise from the much lower minority carrier lifetimes in materials other than Silicon and Germanium. For example in PbTe and GaAs τ is typically 10^{-7} - 10^{-8}s compared with 10^{-3}s in Silicon. By cooling the material n_i can be decreased and τ increased, however, it would need liquid cooling to obtain a large change in these parameters. There is therefore room for some research on improving lifetime in these materials together with tackling other problems such as provision of diodes, channel stop regions etc.

SIGNAL PROCESSING

The papers in session 4 of this Conference will have already indicated the range and depth of interest in using CCD's for signal processing. Because of the many different system requirements there is probably even more scope in this area for future developments in terms of new device and circuit structures.

The reasons why CCD's are potentially important in signal processing have already been discussed in previous conference papers, but they are perhaps worth re-emphasizing.

(a) Good analogue dynamic range ($>$ 60dB) results in a simpler, more compact processor than is possible with equivalent digital systems e.g. no A/D conversion, fewer registers.

(b) Time quantization gives a flexibility in this domain which is not available in purely analogue systems.

(c) Large time-bandwidth products ($>10^3$) are potentially achievable.

(d) High bandwidth operation ($>10^8$ Hz).

(e) The ability to re-order data in two dimensions.

By considering several different types of processor it will become clear that there are still a number of developments required before we can realise all these potential advantages.

Recursive Filters

These types of frequency filters can be constructed using relatively small ($< 10^3$ bits), untapped delay lines. The main improvements awaited concern the dynamic range, transfer inefficiency and other device parameters, and also eventually progress in integrating peripheral circuits on the same chip as the delay line.

Dynamic range and transfer inefficiency are still not adequate for many filter applications. Dynamic range is essentially being limited by two factors at the moment, a lack of satisfactory methods for providing linear electrical input and output with CCD's and the presence of both coherent and incoherent noise sources. Present levels of transfer inefficiency ($\sim 1 \times 10^{-4}$) are sufficient for many applications; however, there are

processors, such as a video integrator with many integrations, which will require much lower inefficiency values, $< 1 \times 10^{-5}$. The development of very low inefficiency devices will involve research into the detailed mechanisms which introduce charge smearing effects. This is where improved models of the charge transport and trapping processes will become important. It needs to be established as to whether the dominant loss mechanism at this level is due to surface states, bulk states, driving techniques, transit time effects, input/output circuits etc, before launching into detailed research programmes aimed at improving any one of these items.

Progress in integrating peripheral circuits is going to assume considerable importance in signal processing devices. For recursive filter systems the need is for the development of fast sample-and-hold and operational amplifier circuits on chip. This may be possible using MOS/CMOS technology for frequencies up to 10^7 Hz but it may eventually involve establishing a mixed bipolar/CCD process for high frequency operation.

Transversal Filters/Correlators

This class of processors require multiple non-destructive tapping combined with either a fixed or electrically programmable weighting technique. The 'split-electrode' method (Ref 4) has proved successful in providing fixed tapping for matched filters, and there are a number of approaches to electrically variable weighting (Refs 5, 6 and 7).

The ultimate development of the transversal filter is the correlator, one type is shown schematically in Fig 3.

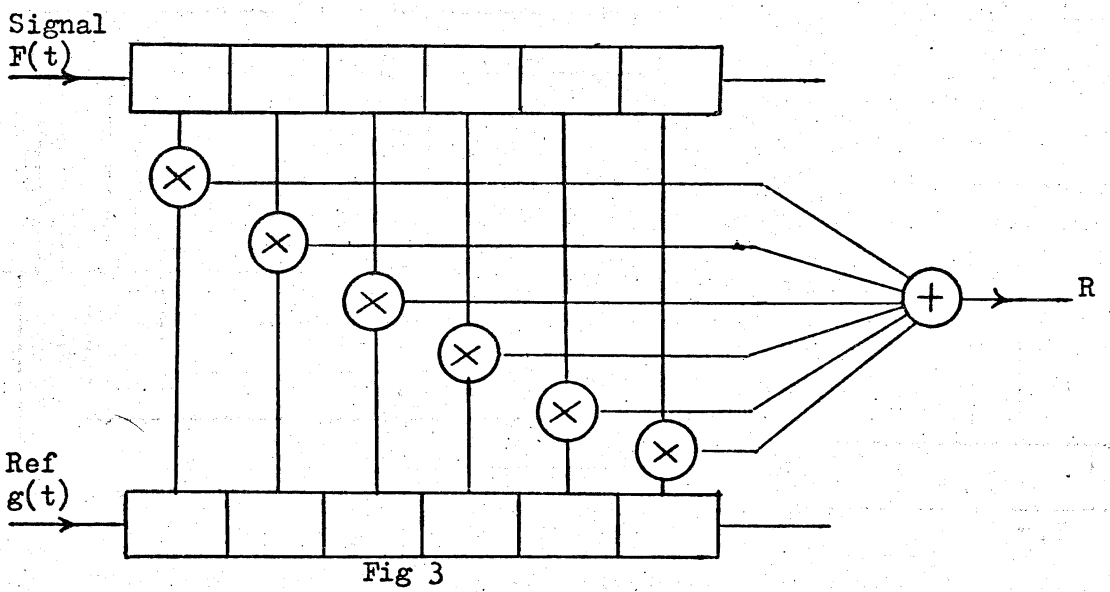

Fig 3

The input signal waveform F(t) is correlated with the reference waveform g(t) to give the cross-correlation function $R = \Sigma F(t)g(t)dt$. An integrated analogue correlator with its code-handling flexibility could find many applications in military and commercial signal processing.

The development of such a signal processor will probably evolve through several stages. Initially we need to extend tapped delay lines to at least several hundred bits, this would be followed by the construction of

a hybrid correlator using separate chips to provide the tapped delay lines, analogue multipliers and summation circuits, wide dynamic range multipliers and operational amplifier peripherals need to be developed on chip to produce the fully integrated analogue correlator. The 'charge sloshing' correlator being developed by Tiemann et al (Ref 8) is the most advanced development so far using CCD type devices to produce a processor of this class.

Data Re-Ordering

It is possible using matrix CCD arrays to store, recirculate and re-organize data in two dimensions to provide quite a different information sequence at the output from that which entered at the input. The present serial-parallel-serial array is an example where data is re-ordered within the array but in this case the input and output sequences are identical.

Devices of the type shown in Fig 4 (a) can multiplex a number of parallel channels to provide a serial information sequence. If there are n channels the output data rate is n times that at each input. Such devices could be operated in reverse to allow serial to parallel conversion. If more control is required over the output data rate extra buffer storage is needed together with some multiplexing of devices at input and output. One possible example is shown in Fig 4 (b); here serial information is loaded into parallel store 1, when this is full the incoming data stream can be switched to a second store. Whilst loading of store 2 takes place the parallel registers in the second store can be unloaded at any convenient data rate. The output sequence will now be in an interrupted form.

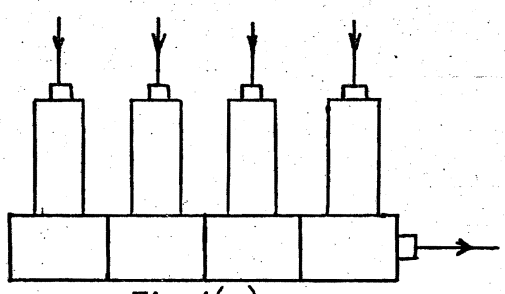

Fig 4(a)

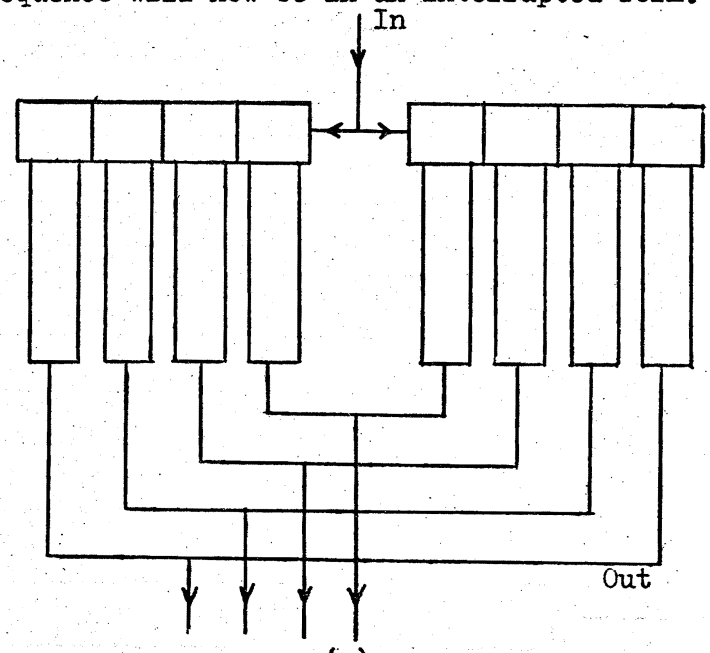

Fig 4 (b)

Another possible requirement is serial-parallel conversion and then sequential readout of each parallel store. One way of achieving this would be to simply provide separate clock lines for each parallel register rather than the combined clock usual in SPS arrays. A more compact approach would be provided by the device shown in Fig 5. Here the parallel stores can be clocked in the X as well as the Y direction so that each parallel array can be sequentially unloaded into an output serial array.

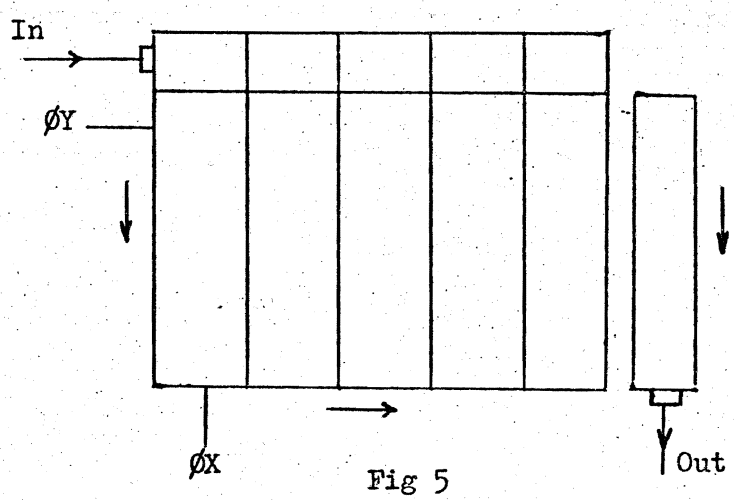

Fig 5

High Bandwidth Processors

The ultimate data rate of CCD arrays will depend fundamentally on the carrier mobility and the electric field in the channel region. As we have heard in session 1 present surface channel devices become transit time limited because of the very low field regions underneath the electrodes. Between electrodes high fields of 10^5 Vcm^{-1} can exist and these can accelerate carriers to the saturation drift velocity of $10^7 cm\ s^{-1}$. What is required are developments in CCD structures which remodel the channel potential to provide continuously an electric field $> 5 \times 10^3$ Vcm^{-1} along the array. Operation at the saturation drift velocity would mean a maximum data rate of $\sim 5 \times 10^9$ Hz, other factors permitting! The buried channel structure is one development towards such a structure but there is still scope for much future research in this area.

DIGITAL MEMORIES

Although these devices are potentially the most lucrative commercially, so far they have received the least attention in CCD research. The problem is that conventional magnetic and semiconductor devices are already well established in mass storage and significant advantages have to be demonstrated by the CCD before a market will develop. The subject of memories has already been well covered by Dr Zaininger and so I propose to mention just a few speculative future developments.

The great potential of CCD serial memories lies in the very high packing density which can be achieved relative to conventional semiconductor stores. This density could effectively be increased further by operating in a multi-level digital mode. Here different sizes of charge packet could be used to represent a binary word as opposed to a single bit of information. The flexibility of CCD's in terms of data re-ordering, non-destructive tapping and recirculation may be used to access information streams at different parts and lead to new methods of structuring data in serial memories.

The random access of CCD memories has not been achieved so far but may not by any means be impossible. One can envisage for example using a buss-bar approach, similar to that used for anti-blooming techniques, (Ref 9) in order to remove data from any part in the array, together with double electrodes to access a particular storage element.

Long term and non-volatile storage may prove possible by using the type of mixed CCD and MNOS approach advocated by Knauer and Goser.

The development of large memory arrays will be equally dependent on progress in the research areas which have been discussed in relation to imaging and signal processing arrays.

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(a) (b)

Fig 1

(Published by C H Sequin et al Ref 10)

(a) Effect of poor transfer efficiency

(b) Effect of dark current spikes