

TWO CLASSES OF CHARGE TRANSFER DEVICES FOR SIGNAL PROCESSING

R. D. Baertsch, W. E. Engeler, H. S. Goldberg, C. M. Puckette, J. J. Tiemann *

ABSTRACT

Charge transfer devices offer new opportunities in analog signal processing, since they provide analog memory with non-destructive read-out. The classic serial transfer architecture provides precision signal processing circuits at low cost. The number of signal samples that can be handled is limited only by charge transfer efficiency. The parallel transfer architecture provides a flexibility and programmability not obtained with serial transfer devices. In addition, the number of signal samples is not limited by charge transfer losses.

I. INTRODUCTION

Both analog and digital methods have been used for analog signal processing. In the analog approach, a desired response (specified in the frequency domain) is approximated by a number of poles and zeros in the complex frequency plane, and these are implemented by passive discrete components and possibly some operational amplifiers. This approach has two important advantages:

1. Negligible power is consumed.
2. Very low minimum cost.

Unfortunately, there are also some disadvantages:

1. Separate filter hardware must be dedicated to each channel. That is, a single filter cannot be multiplexed between several channels.
2. The only designs that can be implemented are those which require a modest number of poles and/or zeros.
3. The values of the discrete components must be very precisely determined. Often they must be individually adjusted and temperature drift and aging can be a problem.

In the digital approach, the signal is sampled and digitized and is processed numerically. This approach solves the problems; while losing the advantages cited above.

The importance of Charge Transfer Technology for analog signal processing is that it combines the best features of both approaches. Namely, it permits an arbitrary impulse response to be implemented easily, it provides high precision without requiring individual adjustment of components, and the cost and power consumption are comparable or lower than for previous analog methods.

II. SERIAL TRANSFER STRUCTURES

There are two distinct approaches for applying charge transfer techniques to signal processing which can conveniently be called Serial Transfer and Parallel Transfer. In the Serial Transfer approach, charge

* General Electric Corporate Research and Development, P. O. Box 8, Schenectady, New York USA

packets representing sequential samples of the input signal are clocked along an analog shift register which provides a variably weighted non-destructive readout at each stage. (ref 1,2) This approach permits a direct implementation of any impulse response. This simplifies the design of filters specified in the frequency domain, since the desired impulse response is the Fourier Transform of the specified frequency response, and it also permits implementation of matched filters whose impulse response is specified in the time domain. The variable tap weights can be determined by splitting the electrodes and sensing the charge transferred to each portion separately. The precision of the tap weights is determined by the accuracy with which the cuts in the electrodes are located. Since these are determined by a photographic mask, high precision can be obtained. The objective of this approach is to provide a component whose cost is commensurate with previous analog methods but which provides the design flexibility and the precision of digital methods. To this end, a mask set was developed for a basic charge transfer structure which serves as a vehicle for an entire family of filters. This two phase overlapping gate structure is similar to devices previously described (ref 3) except that both sides of the Φ_2 electrodes are brought out to contact pads. This was done so both portions can be separately contacted after the cuts are made.

A program was also written for generation of the masks used to define the locations of the electrode cuts. Since these are the only masks that need to be changed for a new impulse response, very little effort is required to provide a new member of the family. An example of this approach is shown in Fig. 1.

In the case shown, a low pass filter was designed by a computer program which computed the tap weights that give the minimum value of worst case ripple for a fixed number of taps, fixed ratio of pass band to stop band ripple, and fixed locations of stop band and pass band edges. Also shown in Fig. 1 is the resulting impulse response. Note the one-to-one correspondence between the locations of the cuts, which are visible on the photomicrograph of the chip, and the resulting impulse response.

Since the pattern generator used to make the masks has a minimum coordinate spacing of .0005", the tap weights had to be rounded off to one part in 600, and as a result, the frequency response is not as good as the computer designed optimum. The theoretical response of the filter as computed from the actual tap weights is shown in Fig. 2a, and the observed frequency response of the experimental filter is shown in Fig. 2b.

Note that the observed frequency response follows the computed response very closely. This indicates that the largest error in the experimental device is less than the roundoff error of one part in 1200 caused by the coordinate quantization of the artwork generator.

Other applications which appear well suited to this approach include:

1. The real and imaginary parts of complex linear chirps for performing the Discrete Fourier or Cosine Transforms via the Chirp-Z-Transform algorithm.
2. Broadband 90° phase shifters for single sideband systems.
3. Broadband differentiators and integrators for synthesizing sampled data control loops.

III. PARALLEL TRANSFER STRUCTURES

Although the Serial Transfer approach outlined above achieves the goal of combining the advantage of both analog and digital methods and applies to a large class of applications, there are some applications for which it is not suited. For example, since charge transfer losses are cumulative in the serial transfer approach, accuracy cannot be maintained for impulse responses that extend over a large number of samples. This problem can be alleviated (if the charge transfer inefficiency is accurately known in advance) by compensating the tap weights to correct for the charge transfer errors. (ref 2) But since transfer losses depend on rather subtle details of the fabrication process, it does not appear feasible at present to rely on a precisely controlled transfer loss. Also, the filters discussed above are not reprogrammable and cannot be shared by more than one channel. Some approaches have been suggested for providing programmable tap weights on Serial Transfer structures (ref 4,5), but none has yet been proposed which provides real-time programmability for continuously variable tap weights. Transfer losses would presumably still be cumulative in such a structure in any event.

A second approach which overcomes these specific problems is therefore desirable. Specifically, the desired characteristics are:

1. Much lower cost and complexity than the digital approach.
2. Not limited by charge transfer losses.
3. Fully reprogrammable at high speed.
4. Able to leap tall buildings at a single bound.

A new approach (Parallel Transfer) has been developed which provides these features with one exception--namely that continuous tap weights are not provided. The architecture of the chip is shown in Fig. 3, and a photomicrograph is shown in Fig. 4.

In this chip, charge packets are not clocked along as they are in the Serial Transfer approach. Instead, each charge packet is placed in an isolated region where it stays until replaced. This is accomplished by the scan shift register, which sequentially opens the gate regions between each of the isolated cells and the analog input bus. A single binary "one" in this shift register causes each gate to be opened as it progresses down the shift register. Once a charge packet has been inserted into a storage reservoir, it is non-destructively read by controllably transferring it back and forth under three readout electrodes which serve all cells in the system and which provide a choice of two tap weights. The displacement currents that accompany these transfer operations are sensed by external circuits, and in this way, multiplication by binary tap weights, which are normally chosen to be ± 1 , followed by a summation over cells is accomplished. The operation of this device has been more completely described in several recent papers. (ref 6,7,8)

It is possible to extend the polarity coincidence function performed by the structure described above to a large number of chips without degrading accuracy. The interconnections required are shown in Fig. 5. The active bit in the scan shift register is simply passed from one chip to the next so that analog samples will be inserted in the following chip as soon as each chip is full, and the binary signals are similarly passed from chip to chip. Summation of the input signal from several chips is accomplished simply by connecting the corresponding output electrodes of all chips together. Since the analog samples remain fixed in position and only the digital signals propagate from stage to stage and from chip to chip, and since these are regenerated at every stage, there is no degradation in signal accuracy in the Parallel Transfer approach as more

samples or more chips are added.

IV. APPLICATIONS AND DISCUSSION

Although the correlator shown in Fig. 5 only performs a polarity coincidence correlation, it is possible to implement a full correlation of one analog waveform against another by extending the digital resolution by adding modules in parallel. This is shown in the right hand portion of Fig. 6. In this instance the binary signals $B_0 \dots B_3$ are derived from an A/D converter.

Note that many more chips are required than in the Serial Transfer structure described in Sec. II to implement an impulse response with comparable resolution and that an external source for the tap weights is also required. One concludes that the Serial Transfer approach is preferred on the basis of cost. But in applications where the volume is too small to justify fabrication of special devices, or where programmability is necessary, the relative efficiency of the Parallel Transfer approach is not the question but rather its cost compared to conventional digital implementation. Unfortunately, such comparisons are highly dependent on the details of the assumptions made, and are therefore difficult to make in a general context. Nonetheless, tests to date have shown that a system consisting of 24 correlator modules and a like number of conventional IC's can perform approximately 300 multiply-accumulate-shift operations per microsecond with 8 bit accuracy for both input signals and about 10 bits of dynamic range at the output.

Thus, it appears that the combination of a simple digital system and a programmable transversal filter such as Fig. 6 can (in some instances) outperform a completely digital system of several orders of magnitude greater complexity.

Thus, even though the cost of a minimum system using the Parallel Transfer approach requires more chips than is required for a Serial Transfer chip of comparable accuracy and number of stages, it can still be much less complicated and much faster than a completely digital approach.

REFERENCES

1. F.L.J. Sangster, Philips Tech Rev. 31, 92 (1970).
2. D.R. Collins, W.H. Bailey, W.M. Gosney, D.D. Buss, Elect. Letters 8, 328 (1972).
3. W.E. Engeler, J.J. Tiemann, and R.D. Baertsch, J. Appl. Phys. 43, 2277 (1972).
4. D.R. Lampe, M.H. White, J.H. Mimms and J.L. Fagan, Proc of CCD Appl. Conf., pp 111 Sept (1973), San Diego.
5. T.A. Zimmerman and R.H. Bower, Proc. of CCD Appl. Conf., pp 141 Sept (1973), San Diego.
6. J.J. Tiemann, W.E. Engeler, R.D. Baertsch, and D.M. Brown, IEEE Trans. on Elect. Dev. ED-21, 300 (1974).
7. J.J. Tiemann, R.D. Baertsch and W.E. Engeler, Int. Solid State Ckts Conf. Digest, pp 154 (1974), Philadelphia.
8. J.J. Tiemann, W.E. Engeler, and R.D. Baertsch, IEEE J. of Solid State Ckts SC-9, Dec (1974).

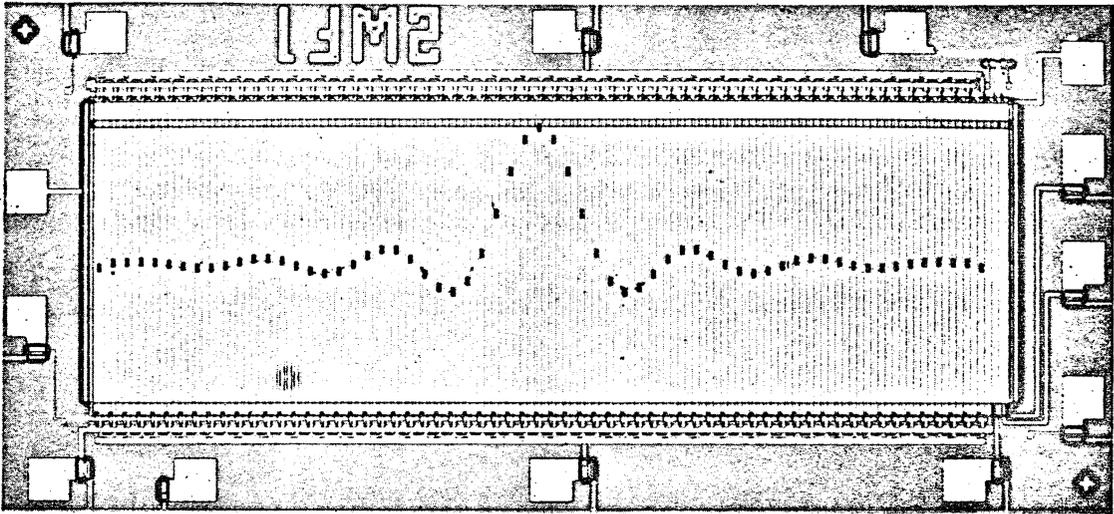


FIG. IA: PHOTOMICROGRAPH OF LOW PASS TRANSVERSAL FILTER

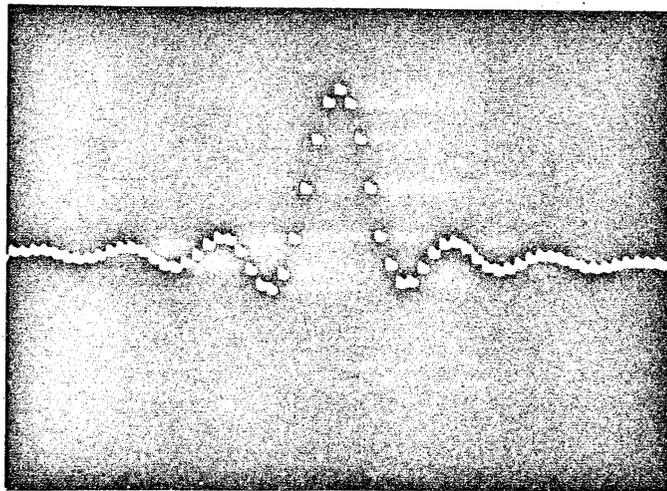


FIG. IB: OBSERVED IMPULSE RESPONSE

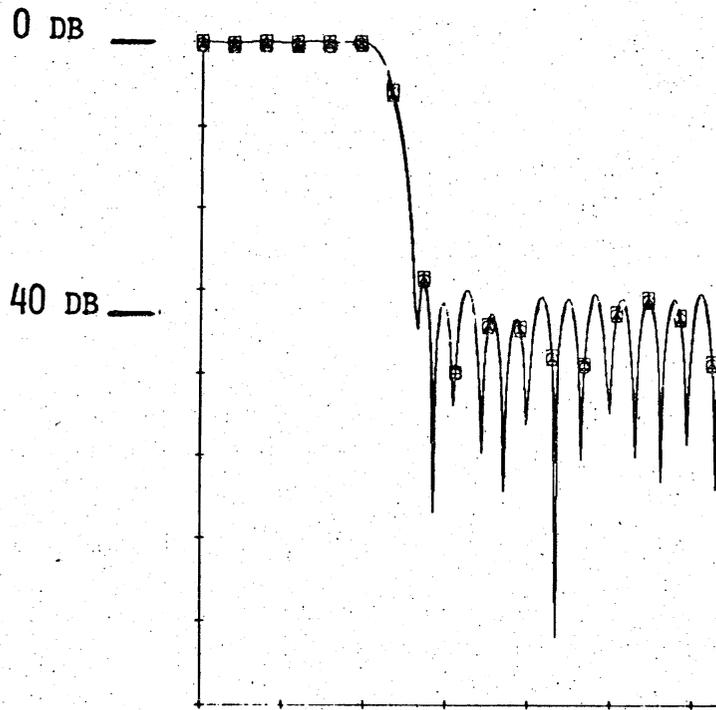


FIG. 2A: CALCULATED FILTER RESPONSE

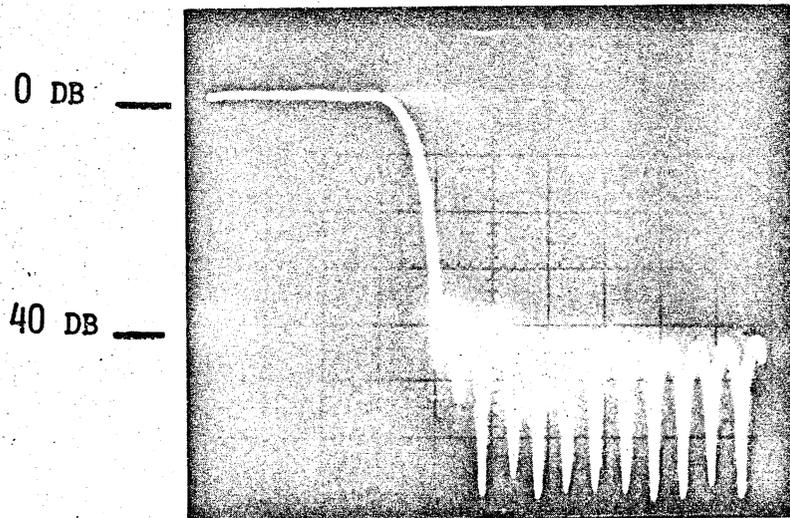


FIG. 2B: OBSERVED FILTER RESPONSE

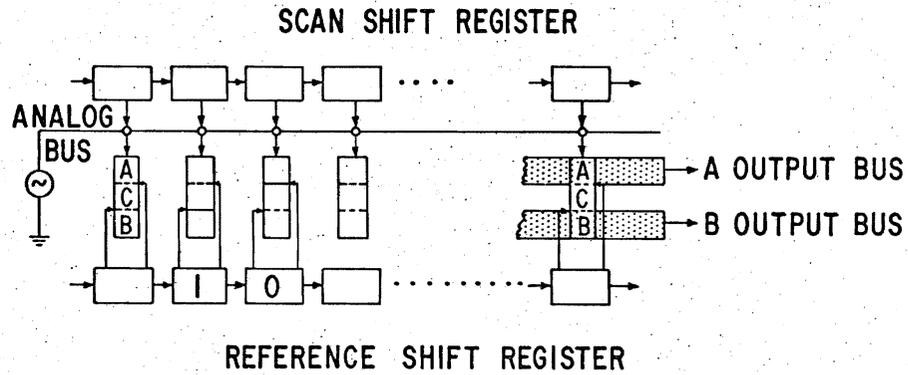


FIG. 3: ARCHITECTURE OF PROGRAMMABLE DEVICE

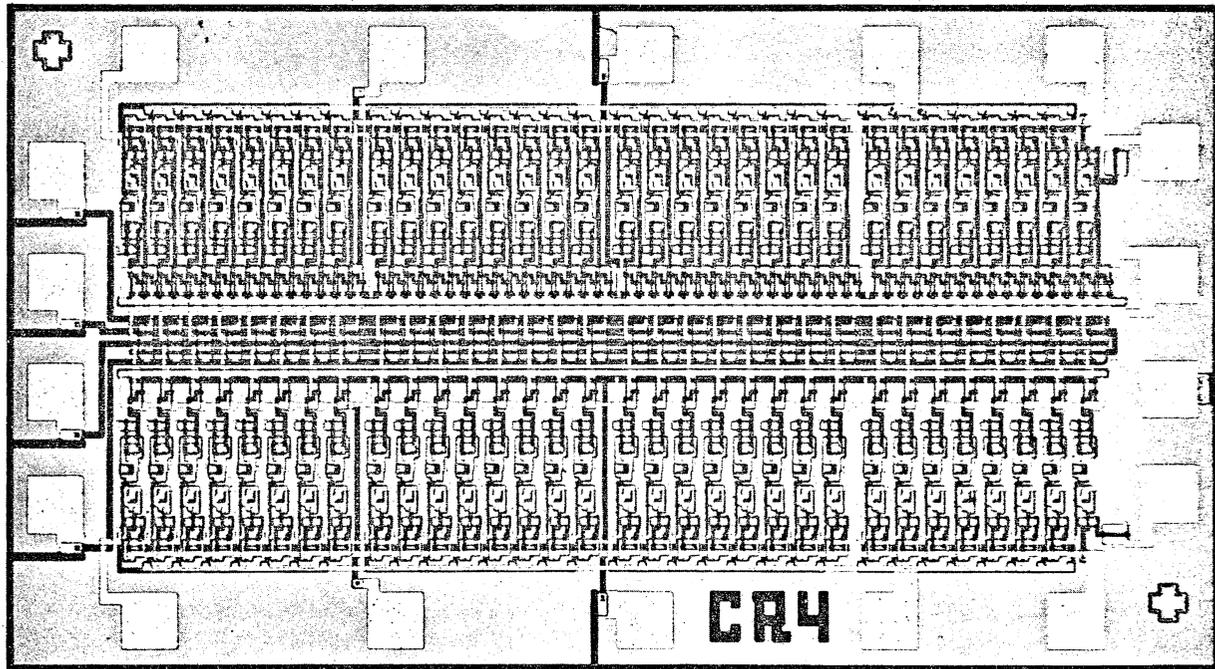


FIG. 4: PHOTOMICROGRAPH OF PROGRAMMABLE DEVICE

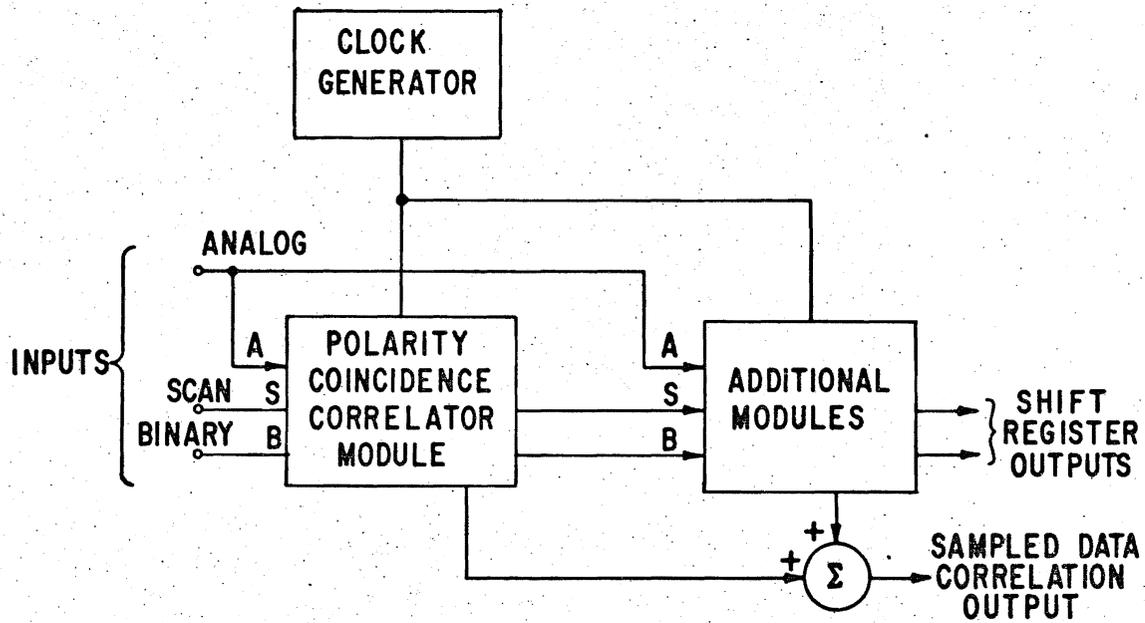


FIG. 5: CHARGE TRANSFER CORRELATOR

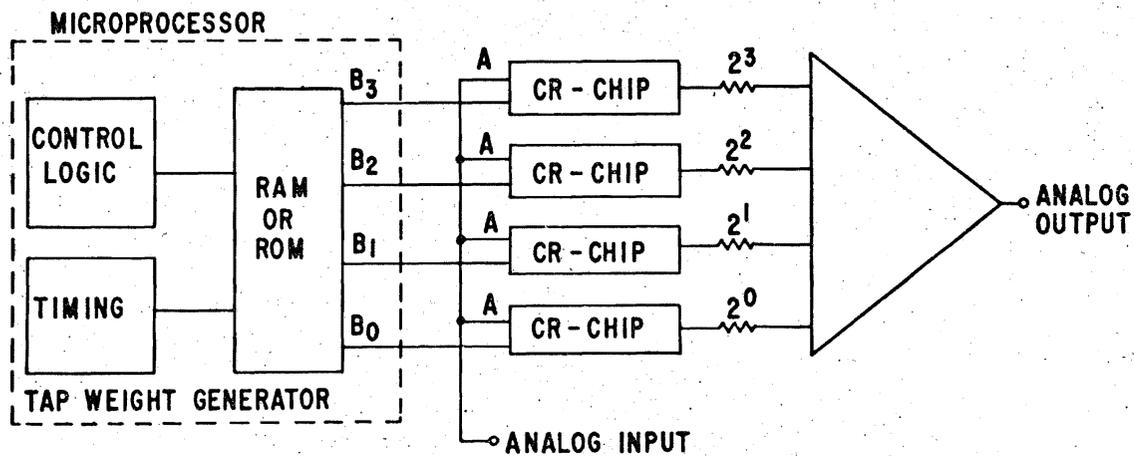


FIG. 6: PROGRAMMABLE TRANSVERSAL FILTER