

VIDEO INTEGRATION WITH CCD DELAY LINES

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ABSTRACT

The principle of enhancing the signal to noise ratio of repetitive signals by integration using a recirculating delay line is well known. CCD analogue shift registers promise a convenient way of implementing this configuration in a way which copes easily with non-uniformly spaced signal repetitions and strobed time intervals. However, the multiple recirculations necessary test the linearity and charge transfer efficiency of the CCD rather stringently, and maintaining a loop gain close to unity without risking instability is difficult. Techniques are described and experimental results shown which justify some optimism that CCD based video integrators will be useful in improving radar displays and reducing noise in television format pictures. A further bonus is the ease with which bandwidth compression is possible, taking advantage of the sampled data nature of the device to slow the time scale and permit transmission of radar or television data through narrow band channels.

INTRODUCTION

Amongst the first system applications of CCD we can expect to find those where a controlled delay function is required. CCD will be especially competitive where the delay is measured in ms and the delay-bandwidth product is less than a few thousand, and where precise and adaptable control of the time variable by clocking is an advantage. Such an application is signal averaging for distinguishing repetitive or quasi-repetitive waveforms from noise or interference. Examples of such signals include 'A-scan' waveforms from a slowly scanning radar, which recur at the pulse repetition rate, and TV-type raster scanned video which recurs at the frame rate. In each case several repetitions can be integrated to enhance the signal to noise (S/N) ratio for stationary components of the waveform.

PRINCIPLES

An estimate of the signal over a frame time is preserved and re-circulated for addition to each new frame as it becomes available. Old data may be 'forgotten' continuously by gradual attenuation or periodically through a 'clear' operation. In contrast with a canceller, which suppresses stationary (ie. repetitive) components to show fluctuations, an integrator uses positive feedback to accumulate recurring features whose repetition rate is known.

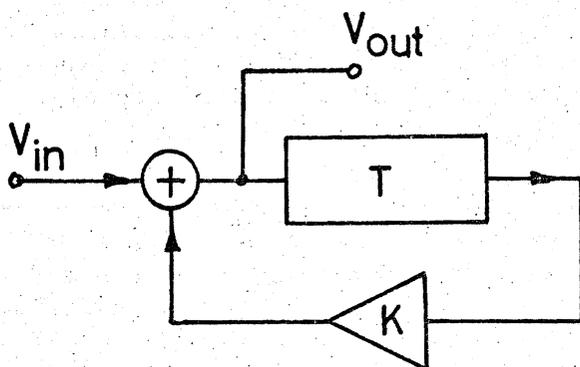


Fig 1
Simple video integrator

The delay T matches the system frame rate. The loop gain K determines the 'memory' of the integrator, ie. the number of recirculated versions of the waveform which contribute significantly to the current output. Since the version which has recirculated n times is attenuated by K^n , ($K < 1$), the impulse response of the network is defined by the sequence

$$\{ 1, K, K^2, K^3, \dots, K^n, \dots \}$$

which shows an exponential fall off with a time constant

$$T_m = T / \ln(1/K) \approx T / (1 - K) \quad (1)$$

when K is near unity. The effective number of repetitions averaged might be taken as $T_m/T = M'$ but a more careful analysis (ref 1) shows the (power) S/N improvement to be

$$(1 + K) / (1 - K) \approx 2 / (1 - K) = 2M' \quad (2)$$

so that it is more useful to take $M = 2M'$ for this purpose.

A CCD seems a particularly convenient form of delay line for a video integrator, since the duration of the delay is under control and can be synchronised easily to a system clock. It combines the simplicity of handling analogue signals, which can be stored over many ms with little attenuation, with the kind of flexibility normally obtained only through digital techniques; including for example coping with strobed time

intervals and non-uniformly spaced repetitions. K controls the integration time constant and if the data is to be treated in discrete blocks we can 'integrate and dump' simply by setting $K = 1$ except during the dump cycle, when the feedback loop is opened ($K = 0$). Also, since CCD delays are determined by a clock waveform, it is particularly easy to compress the bandwidth of the output by a factor $N + 1$, where N is a multiple of the number of samples stored, by arranging the output sampling to access successive values after one or more circulations have taken place. None of these available bandwidth compression ratios may be appropriate to the amount of integration performed. More flexibility is possible using the integrate and dump system since the accumulated result can be transferred to an auxiliary CCD for subsequent readout at any speed. Such schemes will allow low bandwidth channels to carry the integrated information, for example high resolution radar data might be relayed via communication channels.

CCD IMPLEMENTATION

We have realised the arrangement of Fig 1 using as the delay element a p-channel silicon 3-phase CCD storing 64 samples. Operational amplifiers are used to sum the input and recirculating signals and to set the loop gain K . A simplified circuit diagram appears in Fig 2.

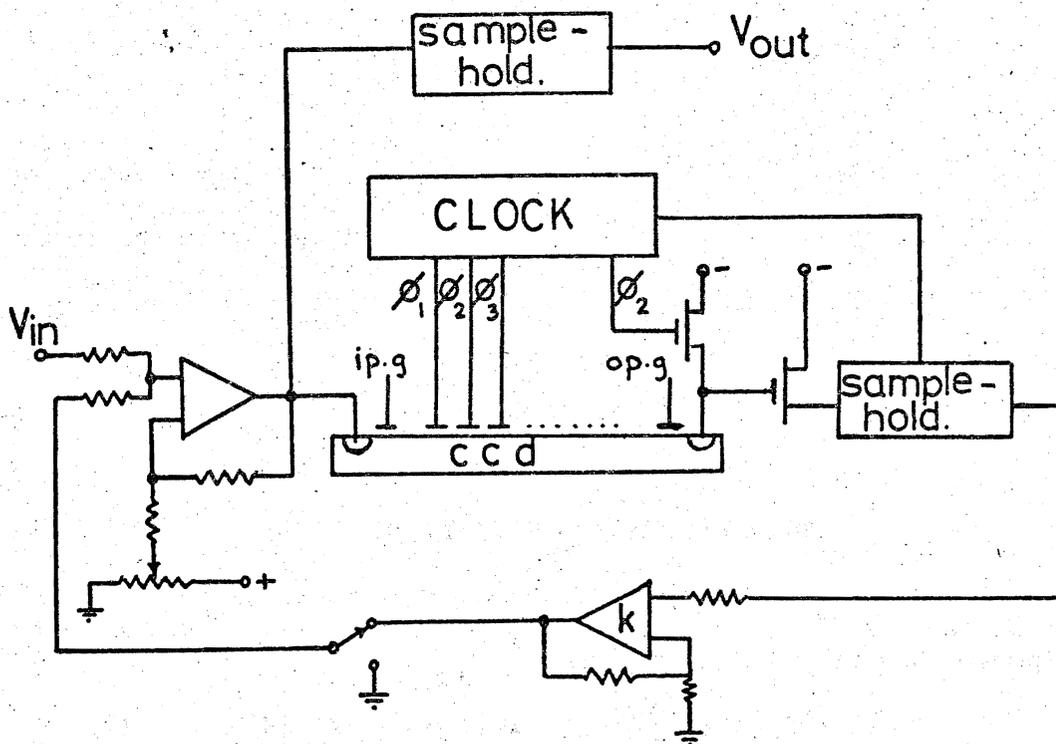


Fig. 2 CCD Video Integration

An external MOST driven by phase 2 of the clock waveform is used to reset the output diode after the sample extraction during phase 1. A sample-hold circuit stretches the output pulse over the intersample period, typically $10\mu\text{s}$ for the experiments reported here, and a switch is provided to break the loop to compare finite and zero loop gains.

Since the effective number of frames integrated is $2/(1 - K)$, it is important to determine what limits the closest possible approach of K to unity. As we approach this condition, the increasing number of recirculations of each signal exaggerates the inevitable distortions which occur at each pass through the device, chiefly non-linearity and smearing.

Non-linearity is evident in Fig 3 which shows the response to a linear ramp input which is progressively distorted at each circulation. Linearity is important because when $1 - K$ is small it is necessary that each input, although much smaller than the recirculating signal, makes its proper contribution to the output. At present the linearity of our system is governed by the input circuitry. This is under development and will be evaluated in due course.

Meanwhile a more serious defect in the present integrator is the signal smearing due to charge transfer inefficiency. This introduces important performance limitations for an integrator, which can be understood in the same way as multipath secondary outputs (eg triple-transit) which have been described in conventional analogue delay lines. Urkowitz (ref 2) shows that for an infinitely repeated data stream, the amplitude of a secondary signal is exaggerated by the square of the build-up factor for the wanted signal. Even when the integration is incomplete, the integrator enhances secondaries considerably more than primaries, the qualitative reason being that the secondaries not only integrate in the normal way, but also feed on the primary signal during each circulation. We can roughly determine the charge transfer efficiency (CTE) needed for a particular application as follows. Suppose that an improvement of I_{dB} in S/N ratio is required, while keeping spurious outputs below a level of D dB with respect to the wanted signal. The integrated signal builds up as the sum of the series

$$1 + K + K^2 + \dots = 1/(1 - K) \quad (3)$$

while the secondary, or residual, from a single circulation is built up by the factor $1/(1 - K)^2$. The rms noise at the output is proportional to

$$\sqrt{1 + K^2 + K^4 + \dots} = 1/\sqrt{1 - K^2} \quad (4)$$

from which it follows that

$$I = 10 \log \left[\frac{1 + K}{1 - K} \right] \approx 3 - 10 \log (1 - K) \quad (5)$$

for $K \approx 1$. Comparing the S/N ratio at the input and output, when a signal of amplitude S gives rise to a one-pass residual SR , shows that we require

$$20 \log \left[\frac{SR}{(1 - K)^2} \right] / \left[\frac{S}{1 - K} \right] \leq D \quad (6)$$

ie that

$$20 \log R \leq D + 20 \log (1 - K) \quad (7)$$

combining (5) and (7) gives

$$R_{dB} = 20 \log R \leq 6 + D - 2I \quad (8)$$

as the first upper limit on R. For example, if a S/N improvement of 20dB is required with spurious signals kept below -30dB, we must keep the residuals below $6 - 30 - 2 \times 20 = -64\text{dB}$ or 6.3×10^{-4} in amplitude. This R results from a complete pass of the CCD. Assuming that a 'frame' of F samples is delayed in a p-phase CCD array with approx. \sqrt{F} fast transfer stages.

$$R = \sqrt{F} p \epsilon \quad (9)$$

where ϵ is the charge transfer inefficiency so that with $F = 1000$ and $p = 3$ we require a very high CTE of $1 - 6.6 \times 10^{-6}$.

We must also check that the integration does not proceed past the useful limit when the secondaries appear above the noise level, ie that

$$\frac{SR}{(1-K)^2} \leq \frac{SN}{\sqrt{1-K^2}} \quad (10)$$

or

$$R^2 \leq N^2 (1-K)^3 / 2 \quad (11)$$

Expressing this in decibels and using (5) we obtain

$$R_{\text{dB}} \leq N_{\text{dB}} - 3 I + 6 \quad (12)$$

which is a more exact expression than was previously given (ref 3). Using our earlier example and assuming an input S/N ratio of say 0dB, this requirement demands

$$R_{\text{dB}} \leq 0 - 3.20 + 6 = -54\text{dB} \quad (13)$$

which is less stringent than the first condition which in this example therefore still determines the CTE requirement.

The K value in our experiments was limited by the rapid growth of secondary signals. As devices with higher CTE become available however, we expect to be limited by the precision with which $1 - K$ can be maintained small but finite. A CCD implementation seems well suited to precise control of the loop gain since it should be possible to reserve one of the 'sample slots' for a reference signal which is monitored after a complete circulation and the loop gain servo controlled to keep the ratio (or difference) constant. Alternatively, operation in the integrate-and-dump mode with $K = 1$ would relieve the criticality of the K value.

RESULTS

Fig 4 shows an improvement in S/N ratio obtained using a 64 - sample CCD video integrator operating on a repetitive ramp signal (trace a) immersed in noise (b) with $K \approx 0.85$. The output (c) clearly shows the recovered signal which disappears when the loop is opened ($k = 0$) at (d). These traces also illustrate bandwidth compression, here by a factor of 65, obtained by allowing a complete circulation of the loop (plus 1 clock period) between taking output samples.

CONCLUSION

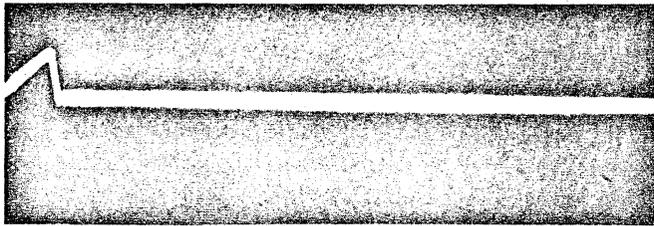
Although the performance of the present CCD video integrator is very limited, especially by charge transfer inefficiency, the development of more efficient CCD should soon make it possible to apply the principles described here in a variety of systems where signals are to be averaged or integrated out of noise or non-synchronous interference. In general, radar and raster scanned imaging systems will require very high CTE (approximately 10^{-5} or 10^{-6} residual per transfer) but there are applications where only a moderate number of signal transfers are involved. Examples may include a linear equivalent of the digital 'm-out-of-n' detector, where perhaps 10 returns are integrated before thresholding, and a signal averager for combining a few samples where too many exist to fit the output matrix in a scan converter.

The main competition is from digital integrators where unlimited recirculation is possible. However, particularly for signal bandwidths measured in MHz, it seems likely that the cost of analogue to digital conversion will make CCD systems preferable.

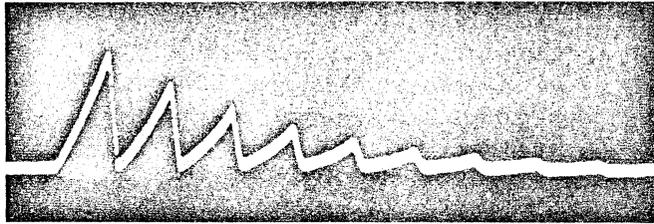
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1. D C Cooper, J Brit IRE, 25, 277 (1963)
2. H Urkowitz, J Franklin Inst. 269, 1 (1960)
Note Expression (5) should read $\frac{C_j}{C_o} \left(\frac{1}{1-K} - \frac{nK^n}{1-K^n} \right)$.
3. J B G Roberts et. al. Elec. Lett. 10, 169 (1974)

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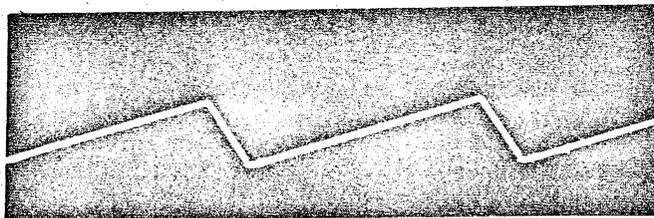


input

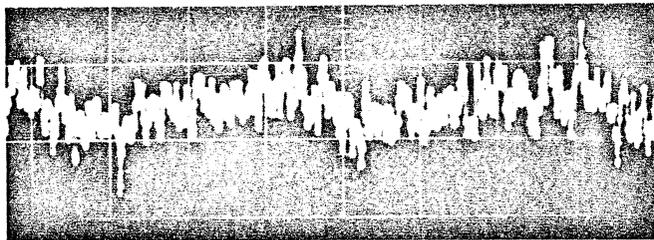


output

Fig. 3

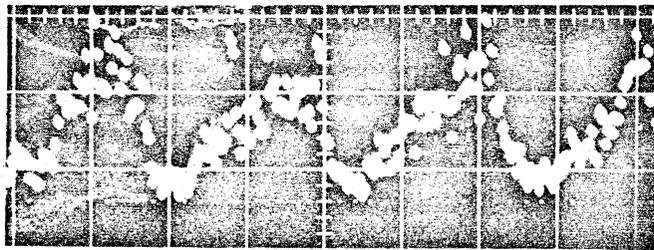


(a)

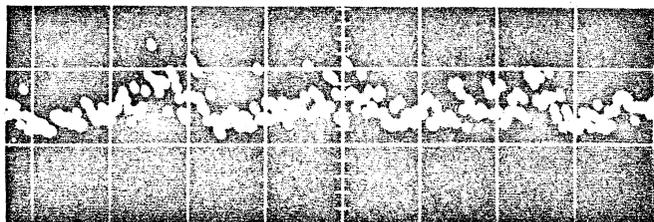


(b)

200 μ s/division



(c)



(d)

20 ms/division

Fig. 4