

CHARGE-COUPLED DEVICES FOR MEMORY APPLICATIONS: A REVIEW

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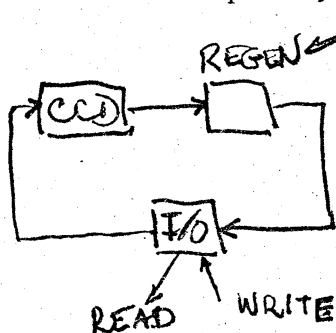
ABSTRACT

Charge-coupled devices - in their simplest form just a string of MOS capacitors - are analog delay lines without internal gain. They can be operated in a digital mode as a dynamic shift register and can, thus, be used as a digital serial memory. In this application, the CCD is used in a memory loop - with the information, i.e. the charge packets representing zeros and ones, constantly being recirculated.

Because the charge transfer efficiency is not 100% the signal degrades with increasing number of transfers, i.e. the ones get smaller and the zeros get bigger. Thus, regeneration stages have to be added at appropriate places. They examine each incoming charge packet, decide whether it should be a one or a zero, and reconstitute it before reinserting it into the loop.

There are basically two routing schemes for the CCD memory loops: the serpentine and the series-parallel-series (SPS) arrangement. The decision as to which one to use and how many transfers one should make before regeneration is made on the basis of the two major trade-offs that have to be considered, namely total storage capacity vs. power dissipation, and storage capacity vs. access time.

Since the CCD memory is a dynamic shift register, it must cycle continuously, even when its stored data is not in immediate use. The power it dissipates in this stand-by mode is minimized if the clock frequency is low. But since the stored information degrades as a function of time, as well as the number of transfers, one must intersperse more regeneration stages as the clock frequency is lowered. This reduces the chip's total capacity. Also, since no bit can be read except from an input-output circuit incorporated into the shifting loop, the access time is determined by the number of input-output stages that are interspersed. Again, these stages reduce the capacity of the chip.



REGEN ← Need DC decoupling

SERIAL MEMORY

Power per bit: CV^2fc

Bell Northern: 8192 Bit Serpentine layout
with one directional flow with long AI gate

Active Area $\approx 1.4 \text{ mil}^2/\text{bit}$

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