

THE IMPACT OF LARGE CCD IMAGE SENSING AREA ARRAYS

Gilbert F. Amelio

ABSTRACT

Only a few years have past since it was realized that charge-coupled device (CCD) technology could be employed to produce solid-state image sensors with uniquely low noise properties and a large dynamic range. This paper reviews the significant technical progress which has been made in this short time to fulfill this promise.

An example of recent progress is the Fairchild 190 x 244 photoelement area image sensor. The entire device occupies a silicon-chip area of 6.15 mm x 6.30 mm. It is an interline structure with 190 columns each with 244 photoelements and 190 2-phase opaque vertical CCD shift registers. The video information is read out in two serial fields which are interlaced at the display. The device employs a buried channel design.

In addition to the standard gated-charge integrator type of detector-preamplifier, this sensor possesses a CCD-compatible, low-noise 12-stage distributed floating-gate amplifier (DFGA). The input of each stage is a floating gate which is located over the CCD channel. Charge packets passing through the channel under the floating gate are nondestructively sensed by capacitive-coupling which modulates an associated MOS transistor. The MOS transistor amplified outputs are synchronously collected in a second CCD or output channel. The performance of the sensor as well as the DFGA is described.

Large image sensing arrays of this type are expected to find substantial usage wherever such considerations as ruggedness, reliability and low television camera power are at a premium. With the inclusion of a high-sensitivity preamplifier like the DFGA, and with some cooling means, these devices will also be able to serve a large low-light-level TV market.

I. INTRODUCTION

Since the charge-coupled device concept was first conceived in 1969, there has been a dramatic and rapid evolution of area imaging devices toward the goal of achieving full television resolution on a single monolithic silicon structure. This evolution has been highlighted recently by reports of an operating 220 x 256 photo-element device in one labora-

tory by Sealer, Sequin and Tompsett⁽¹⁾ and a 320 x 512 photoelement device in another laboratory by Rodgers.⁽²⁾ This paper describes a 190 x 244 photoelement image sensor produced in our laboratory. This rapid development is even more impressive when the magnitude of the silicon chip areas which are required to accomplish this is considered. The 320 x 512 element imager, for example, is made on a 500 x 750 mil chip. The image quality exhibited by these and earlier reported CCD imagers⁽³⁾ clearly shows the viability of a large CCD imager. Not only has the image resolution been shown to be close to the theoretical limit for a given design, but also the dynamic range has been shown to be useful for many applications.

When the structural configuration and mode of operation of these CCD image sensors are compared, it becomes obvious that there are several design options which can be employed to satisfy each of a number of functional requirements or issues. These issues and design options are reviewed in this paper. Those options selected for the design of the 190 x 244 photoelement sensor are then described. A significant distinguishing feature of this device is the incorporation of a distributed floating gate amplifier (DFGA) which has a projected noise equivalent signal (NES) of less than ten electrons per picture element per frame under suitable operating conditions.

II. MAJOR DESIGN OPTIONS IN CCD AREA IMAGE SENSORS

Table I is a list of the design issues and options which have been considered as CCD area image sensors have evolved. The major issues of concern are the device organization, the illumination side and the channel mode. Of equal importance for certain applications are the low-light level mode, the method of signal detection, and the incorporation of anti-blooming control.

Three options of device organization are shown schematically in Fig. 1. These are frame transfer (FT), interline transfer (ILT) and line transfer (LT). The overriding consideration here is the impact of organization on projected device fabrication yield without compromising performance. For any of these options, the operating point on the yield versus complexity curve is low where small differences in area and in defect density have a large effect on yield and hence, cost. The experience of the semiconductor

(1) D. A. Sealer, C. H. Sequin and M. F. Tompsett, "High Resolution Charge-Coupled Image Sensors," IEEE Intercon '74 (Session 2 Digest), March 1974.

(2) R. L. Rodgers, III, "Charge Coupled Imager for 525-Line Television", IEEE Intercon '74 (Sess.2 Digest) March 1974.

(3) M. F. Tompsett, D. A. Sealer, C. H. Sequin and T. A. Shankoff, "Charge Coupled Image Sensing: State of the Art", IEEE Intercon '73 (Sess. 1 Digest), March 1973.

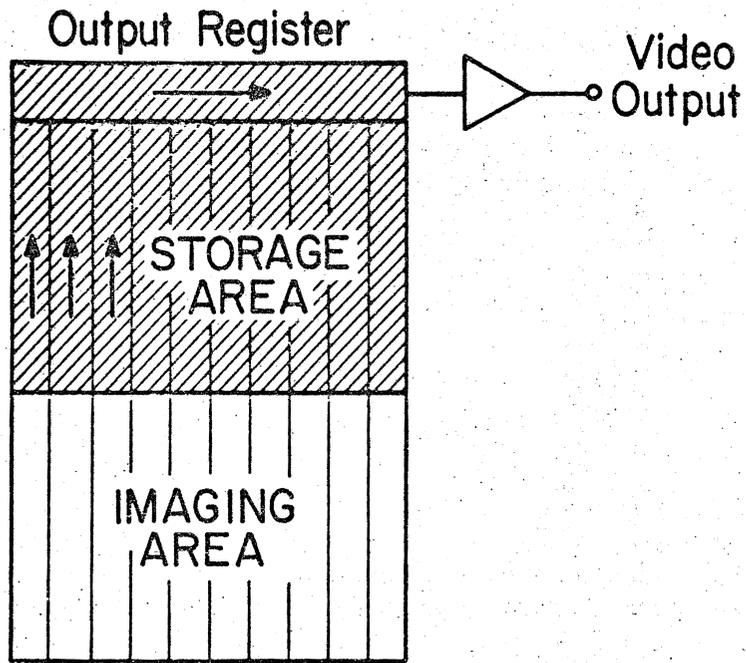
T A B L E I.

DESIGN ISSUES AND OPTIONS FOR CHARGE-COUPLED AREA IMAGERS

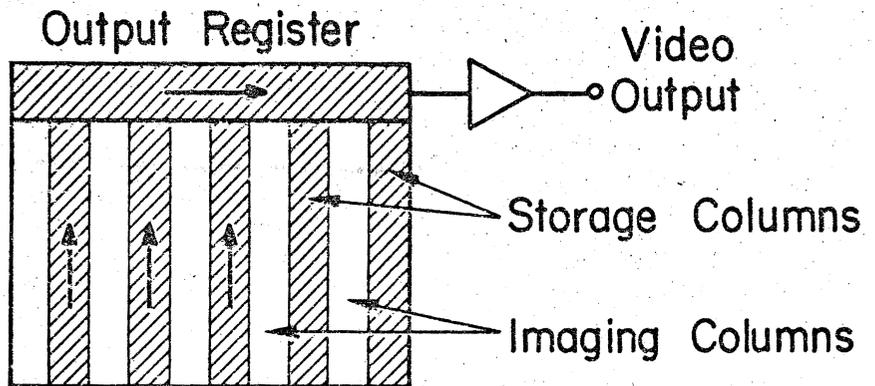
<u>ISSUE</u>	<u>OPTIONS</u>
1. Organization	Frame transfer, interline transfer, line transfer
2. Illumination side	Front, back
3. Channel mode	Surface, buried
4. Gate technology	Silicon, aluminum, refractory metal
5. Polarity	N-channel, P-channel
6. Clocking	2-Phase implanted barrier, 2-phase stepped oxide, 3-phase, 4-phase
7. Low light level mode	Electron imaging (with photocathode), direct optical imaging (with cooling)
8. Interlace mode	True, pseudo, sequential
9. On-chip preamplifier	None, GCI, FGA, DFGA
10. Anti-blooming control	None, element-type, column-type

135.

(a)
FRAME TRANSFER
(FT)



(b)
INTERLINE TRANSFER
(ILT)



(c)
LINE TRANSFER
(LT)

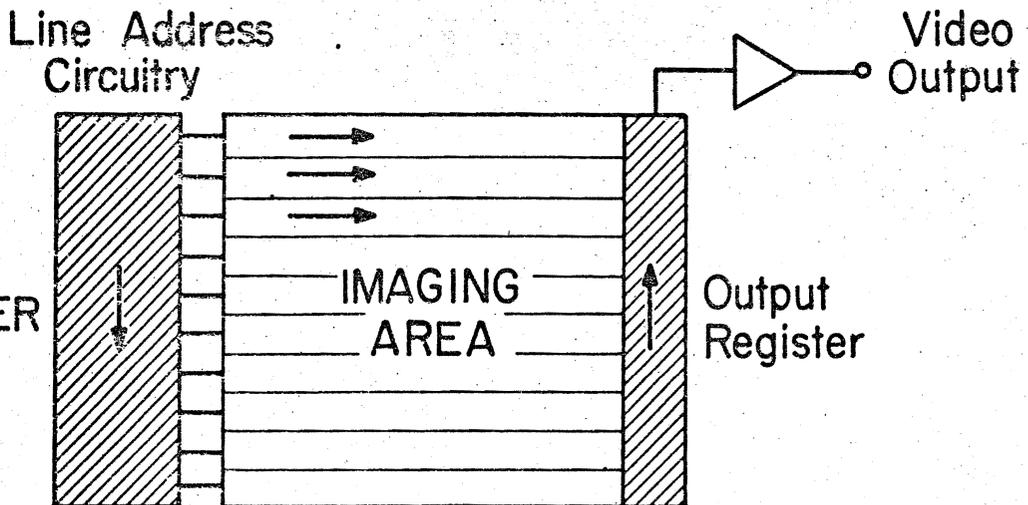


FIG. I
Three basic types of organization for a
Charge-Coupled area image sensor

industry is that the die area is the major factor in device yield. For example, when the yield for a particular integrated circuit is approximately ten percent, the yield for a device of similar complexity and twice the area is less by a factor much larger than two. Since the frame-transfer organization requires substantially more total device area to accommodate a buffer store, it has a major disadvantage compared to the other two which do not have this requirement.

Nonetheless, the issue of complexity cannot be completely ignored. The frame transfer organization is functionally the simplest. The line transfer organization employs a scan generator. The interline transfer structure requires separate photoelement sites and shift registers. This is an advantage with regard to interlace where the frame-transfer method of pseudointerlace compromises vertical resolution.

With regard to the illumination-side issue, it may appear, at first sight, that the backside option has an obvious fundamental advantage because the surface transmittance can be made substantially higher than with any of a variety of front-side CCD structures. Transmittance, however, is not the only criterion; image smearing can result by photoelectron diffusion in going from the backside point of generation to a potential well. Where infrared responsivity is not of concern, backside illumination through extremely thin substrates is optimum; relatively high modulation transfer function (MTF) and quantum efficiency can be obtained at all visible wavelengths. This problem has been analyzed by Seib.⁽⁵⁾ However, where infrared responsivity is desired, thicker substrates are required and a substantial loss of MTF is incurred for most of the visible spectrum. This loss results because photoelectron diffusion can have a large effect. Alternatively, in frontside illumination, a thicker substrate does not degrade the visible spectrum MTF, although the quantum efficiency is in general less, particularly in the blue, than for the thinned-substrate backside illumination. However, if blue response is not important, the cost and complexity of backside illumination is probably not justified.

The issue of buried channel vs. surface channel mode has been resolved. It is clear that buried channel not only provides several major advantages in performance, but also simplifies device design and operation. The charge transfer efficiency of the buried channel mode is high for the full range of electron packet size, from saturation charge of approximately 10^6 electrons to the order of ten electrons or less.⁽⁶⁾ Wide dynamic range is obtained by a straightforward design whereas with the surface channel mode, it is necessary to cope with the level of the in-

⁽⁵⁾D. H. Seib, "Carrier Diffusion Degradation of Modulation Transfer Function in Charge-Coupled Imagers", IEEE Trans. on Electron Devices, Ed.21, Mar. '74, pp.211-217.

⁽⁶⁾R. H. Dyck, M. D. Jack, unpublished.

variably required "fat zero" channel current, the means for introducing the "fat zero" and the noise sources related to the "fat zero" current. One criticism of the buried channel mode is that the saturation signal charge density cannot be made as high as with the surface channel mode and that it therefore limits dynamic range. On the contrary, the buried channel results in orders of magnitude higher dynamic range by virtue of the relatively low noise levels that have been obtained.

Image blooming in a camera is an undesirable phenomenon; under some conditions it can wash out most of the picture information. CCD image sensors also bloom unless some anti-blooming means is incorporated. The only adequate method known which accomplishes this is a charge overflow sink, (7) which for element anti-blooming must be applied to every sensor element. Considerable structural complexity is thereby involved. Even when an image is excessively intense, smearing will occur in those types of sensor where charge is transported through illuminated areas. The FT and LT device organizations have this problem; the ILT device organization does not because the photoelement sites are distinct from the transport register. Where it is a problem, the device must be designed and operated in such a way that the smear-producing charge transfer process can be carried out as fast as it is generated. Thus, after the introduction of a considerable increase in device complexity, anti-blooming control still may not be satisfactory in some applications. The performance-complexity tradeoff must be carefully weighed.

A compromise solution to the problem is to incorporate only one anti-blooming charge sink per sensor column. A device with this feature can bloom within columns, but not between columns. This feature is part of the 190 x 244 image sensor design.

III. DESIGN CONSIDERATIONS OF THE 190 x 244 IMAGE SENSOR

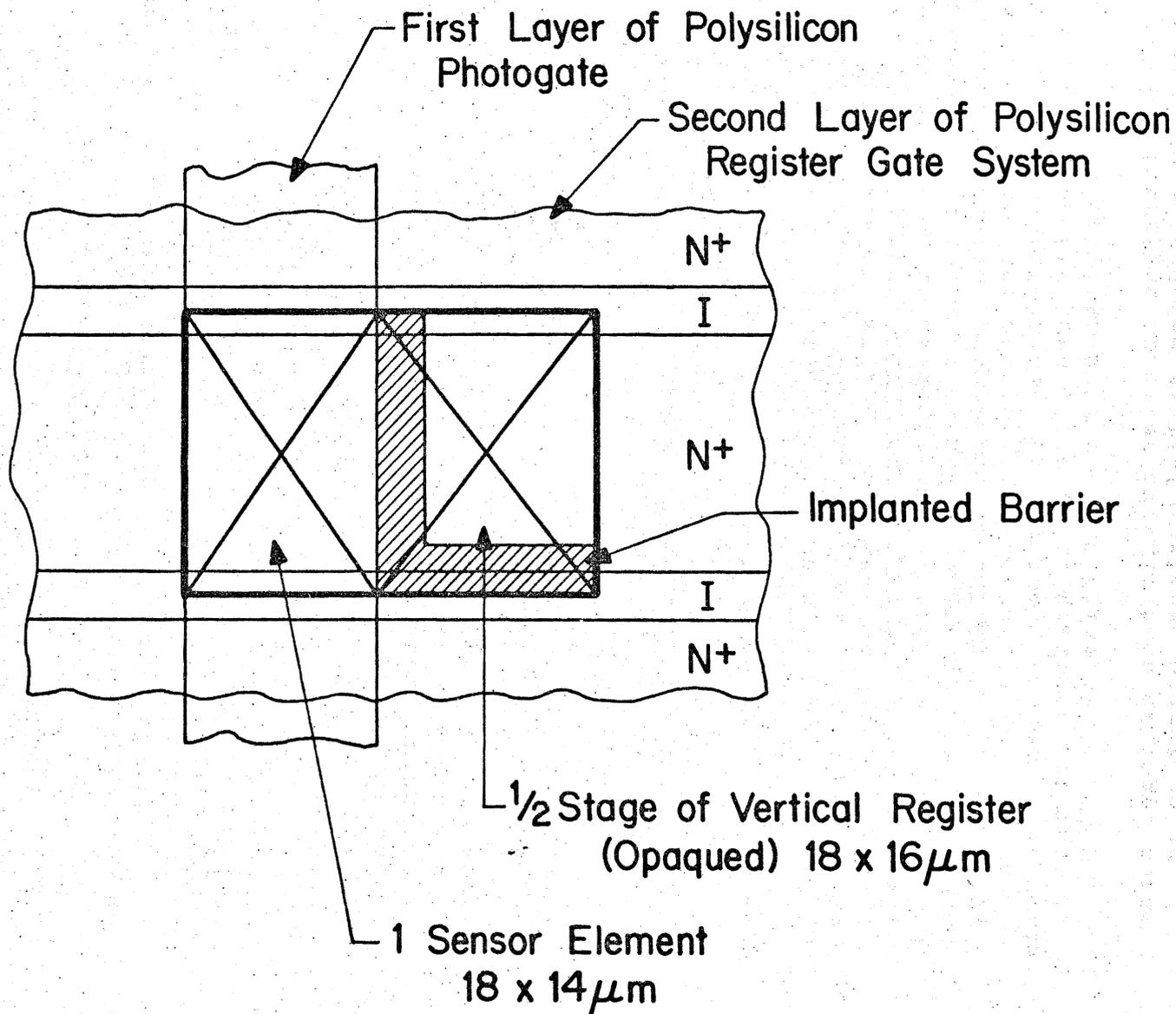
In general, the unit cell configuration of the 190 x 244 array is the same as that of the 100 x 100 element array which has been described previously. (8) Since the cell design is not new, only a brief description is given here. Fig. 2 is a plan diagram which shows how two levels of polysilicon are used to achieve the required charge control. The number of elements in the 190 x 244 array were selected to provide half the resolution in each direction relative to a corresponding NTSC-compatible, full-resolution 380 x 488 array. The 488 row count of the

(7) C. H. Sequin, "Charge Coupled Frame Transfer Imaging Devices with Interlaced Readout & Blooming Suppression" (Bell Labs) IEDM '72, (Session 27).

(8) L. Walsh, R. H. Dyck, "A New Charge-Coupled Area Imaging Device", Proceedings of the CCD Application Conference, San Diego, Sept. '73, pp. 21-22.

FIG. 2.

Simplified layout diagram of the unit cell of the Fairchild 190 x 244 area image sensor



139.

full resolution array was determined directly from the 525 line per frame standard corrected for the normal vertical blanking time. The 380 column count of the full resolution array was determined by choosing the element frequency to be a multiple of the 3.58MHz chrominance sub-carrier frequency which would have given approximately the horizontal resolution as limited by the NTSC video bandwidth of 4.2 MHz. The choice of element frequency was 7.16 MHz which resulted in a video bandwidth of 3.58 MHz and 380 elements per line between horizontal blanking periods.

The number of elements together with the effects of transfer inefficiency determine the accuracy of image sensing, that is, the MTF. The resulting MTF characteristics are shown in Fig. 3 for $N\epsilon=0$ and for an assumed $N\epsilon=0.1$ where N is the number of transfers and ϵ is the fractional loss of packet charge caused by transfer inefficiency.

The physical size of the total sensor area was also determined by consideration of a full-resolution NTSC-compatible array. An important reason for having a size requirement is that the availability of a suitable off-the-shelf lens should not be a problem. Two options are the sizes of the 2/3 inch and the 1 inch vidicon raster. There is an advantage in the design of the unit cell when a raster size close to that of the 1 inch vidicon is selected. The size of the 190 x 244 array was thus chosen to be 5.7 x 4.4 mm. This corresponds to an element spacing of 18 μ m vertically and 30 μ m horizontally. Table II shows how this device compares with two other large devices in element count and size.

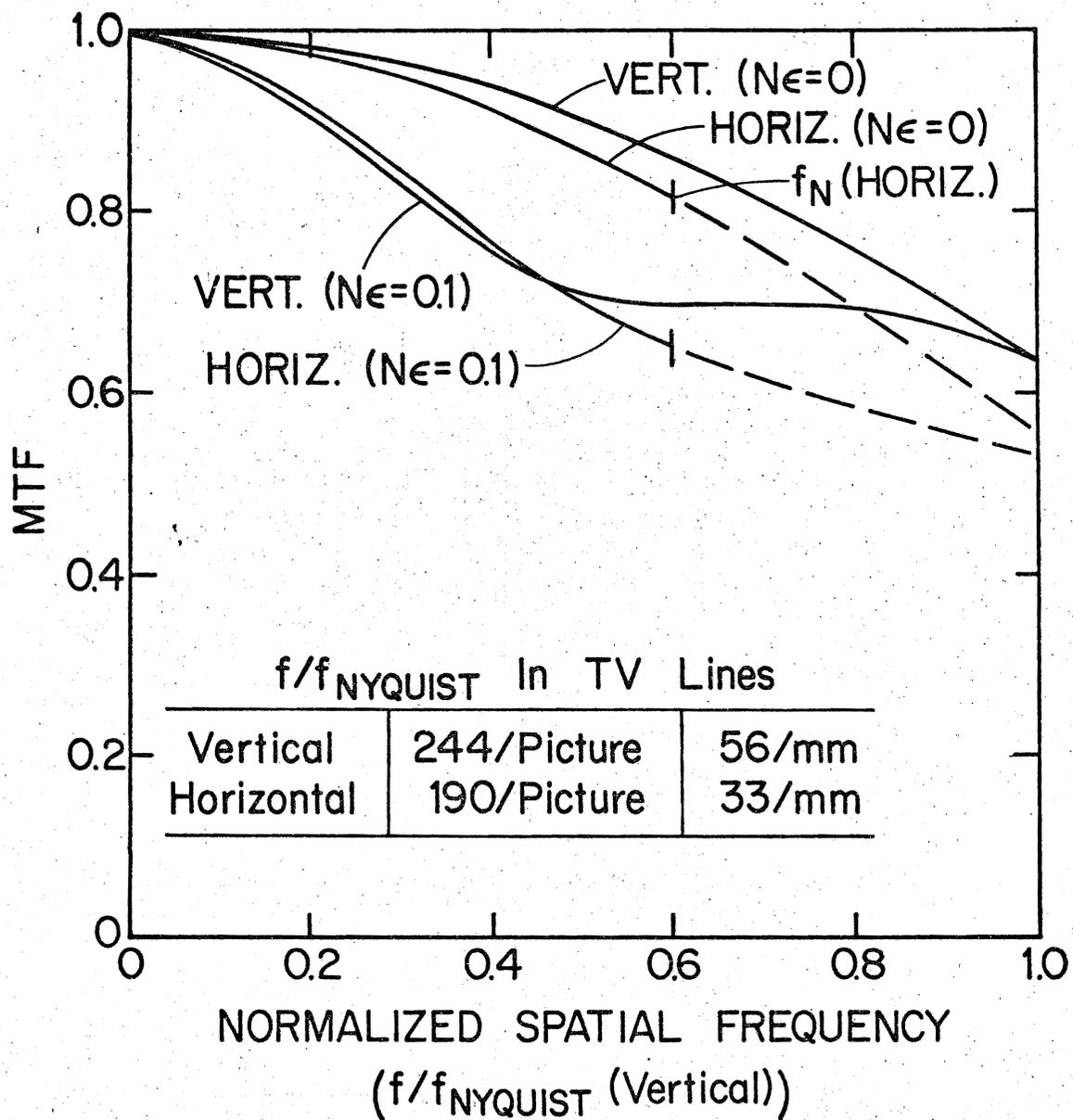
Approximately half of the unit cell is light-sensitive in this interline transfer array because the storage matrix is located within the sensing raster and must be opaqued to prevent vertical smearing of the image. In a frame transfer device the raster would be 100 percent light sensitive. It should be noted, however, that when a comparison is made where the total silicon area and the f-number of the lens are held constant, the two device organizations have approximately equal light sensitivity; that is, the product of the lens aperture area and the fractional sensitive area of the imaging raster is approximately the same for both. A general treatment of this problem has been given by Barbe and White.⁽⁹⁾

The interline transfer organization of image sensors is naturally suited for field-interlaced operation as

(9) D. F. Barbe and M. H. White, "Tradeoff Analysis for CCD Area Imagers: Frontside Illuminated Interline Transfer vs. Backside Illuminated Frame Transfer", Proceedings of the CCD Applications Conference, San Deigeo, Ca. Sept. 1973, pp. 13-20.

Fig. 3

Calculated MTF characteristics of the
Fairchild 190 x 244 array



T A B L E II.

COMPARISON OF THREE LARGE CCD AREA IMAGER SENSOR AREA

Type	Reference	Number of Non-Overlapping Sensor Elements		Nyquist Limits (TV lines per picture)		<u>Raster Size</u>			<u>Chip Size</u>		
		Horiz.	Vert.	Horiz.	Vert.	H (mm)	V (mm)	A (mm ²)	H (mm)	V (mm)	A (mm ²)
FT	Sealer, et al ⁽¹⁾	220	128	220	256	~ 6.6~	5.0	~ 33	~ 8.6~	12.4	~ 107
FT	Rodgers ⁽²⁾	320	256	320	512	9.9	7.8	~ 77	12.7	19.0	242
ILT	This paper	190	244	190	244	5.7	4.4	25.0	6.3	6.1	38.4

employed in standard television practice. Furthermore, interlacing can be accomplished in a simple way when two-phase vertical CCD registers are used. As may be seen in Fig. 2, there is one sensor element for each half-stage of the register, which gives a total of 122 stages in each vertical register. This design is attractive both with respect to the unit cell layout and with respect to device clocking requirements.

The vertical register design utilizes undoped polysilicon between doped polysilicon electrodes, and implanted barriers to provide directionality of charge flow. A comb-shaped channel-stop diffusion defines three sides of each sensor element.

A photograph of the entire device is shown at the top of Fig. 4. An image obtained with one of the earliest devices is shown in Fig. 5.

IV. THE DISTRIBUTED FLOATING GATE AMPLIFIER (DFGA)

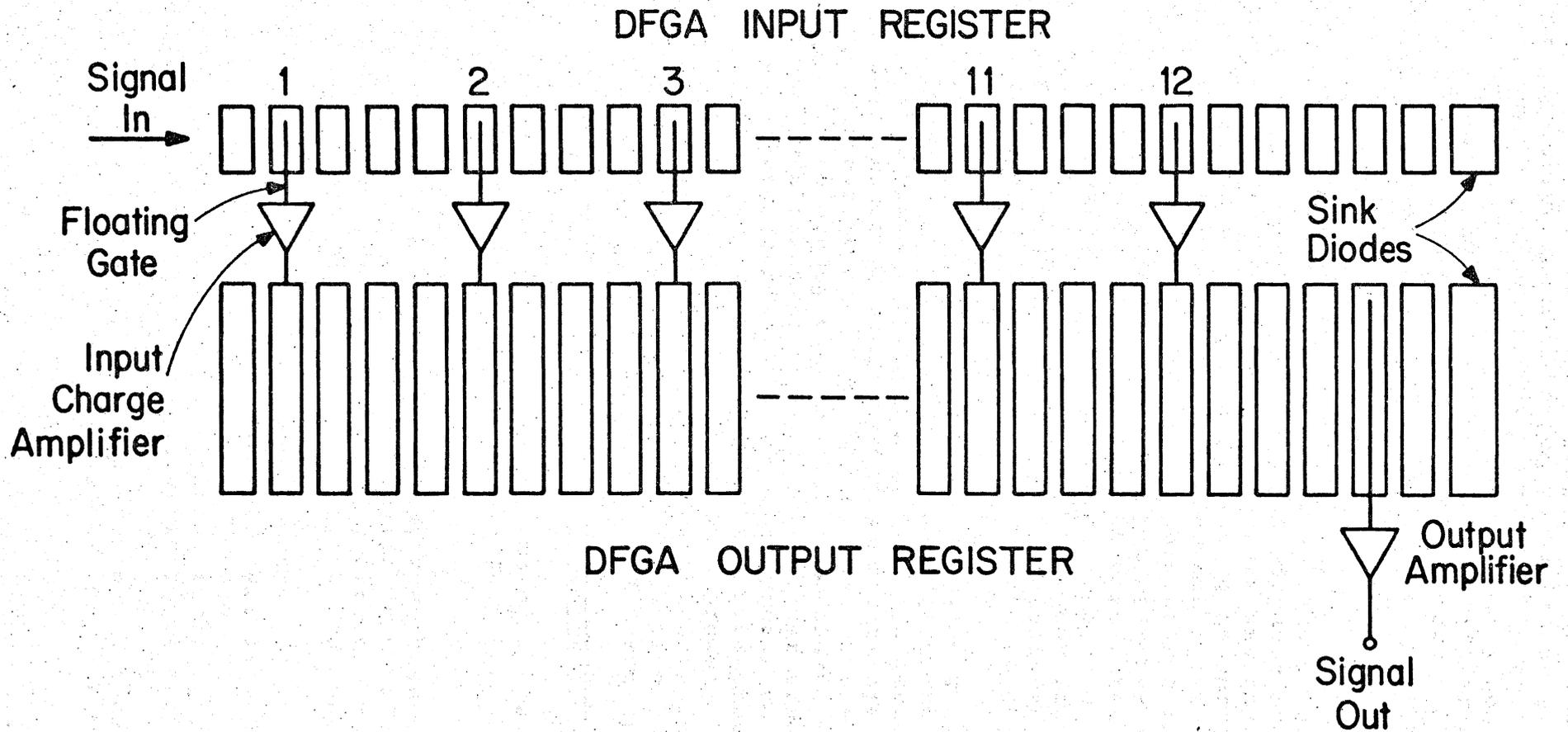
In addition to the more conventional gated charge detector preamplifier, this device incorporates a type of preamplifier which is capable of amplifying charge, a new concept in the area of semiconductor devices. The DFGA concept is based on the property of charge-coupled devices that signal charge can be passed under a sensing electrode and then further transported to other sensing electrodes with no signal degradation. By sensing the signal charge repeatedly, it is possible to improve the signal-to-noise ratio in power relative to a single stage amplifier by the number of times the signal is sensed. By summing the amplified signals in a second CCD register, proper reconstruction of the signal in the time domain is automatically obtained.

A schematic diagram of the DFGA incorporated in the 190 x 244 array is shown in Fig. 6. It consists of four functional parts: an input register, a bank of charge amplifiers with floating gate inputs, an output register, and an output amplifier. This particular DFGA has twelve stages. It uses inverting amplifiers between the two registers and has a floating gate output amplifier. A four-phase register clocking scheme is used to obtain maximum clocking flexibility; the two registers are driven by the same set of clocks. Fig. 4 (bottom) shows a photograph of this DFGA. The DFGA occupies an area of approximately 250 x 400 μm .

A single DFGA stage consists of a source, a floating gate, a bias electrode, a control gate, and a gate which serves to minimize clock coupling from the control gate to the floating N⁺ diffusion, as shown in Fig. 7. It may be seen from the potential well profiles in Fig. 7 how charge control is achieved. During the period that a signal charge packet in the input register is under the floating gate, the control gate is pulsed "on" for a precise time interval. During this time interval, a small fixed charge and a signal-dependent current flows; the larger the initial charge packet, the less current flows.

FIG. 6

Schematic of the Distributed Floating Gate Amplifier (DFGA)



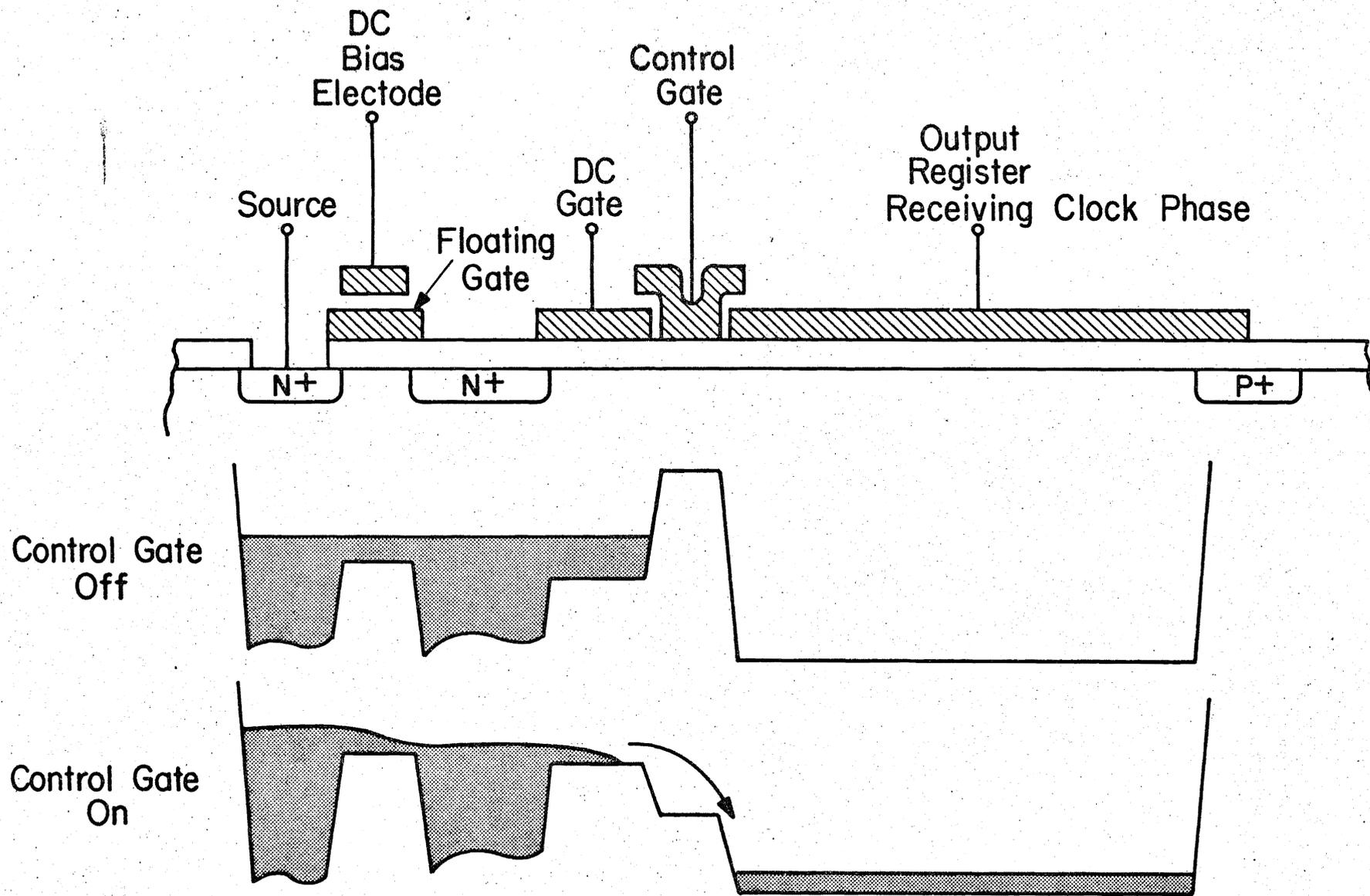


FIG. 7
Schematic cross-section-one input charge amplifier in the DFGA

The effect of signal charge level on the voltage of a floating gate is determined analytically by a capacitance network. A cross-sectional view of a floating gate in Fig. 8 identifies the several capacitances involved. The responsivity is given by

$$\frac{dV_{FG}}{dQ_s} = \left[C_2 + C_4 + C_{in} + \frac{C_3}{C_1} (C_1 + C_2 + C_4 + C_{in}) \right]^{-1} \quad (1)$$

This responsivity by design can be of the order of 5 $\mu\text{V}/\text{electron}$.

The charge gain for small signal is given by

$$A_Q = \frac{dV_{FG}}{dQ_s} g_m t \quad (2)$$

where g_m is the MOS transistor transconductance and t is the time that the control gate is on. Since g_m is in general a function of the current level of the MOS transistor and since the noise level is also a function of the current level, it is desired to establish the current level which gives the optimum signal-to-noise ratio at the output for small signal level. It can be shown that shot noise in the MOS transistor is the dominant noise source of the DFGA. Therefore, the output of a single stage in electrons is

$$n_s = \frac{dV_{FG}}{dQ_s} \left[\frac{g_m t Q_s}{q} \right] \quad (3)$$

the noise in RMS electrons is

$$n_N = \left[\frac{I_D t}{q} \right]^{1/2} \quad (4)$$

where I_D is the drain current. This gives a signal-to-noise ratio (in voltage):

$$\frac{n_s}{n_N} = \frac{dV_{FG}}{dQ_s} g_m \left[\frac{qT}{I_D} \right]^{1/2} Q_s \quad (5)$$

By making the assumption g_m is proportional to I_D and by considering that I_D and C_{in} (from Equation 1) are both proportional to the channel width of the MOS transistor, it is possible to optimize the MOS transistor geometry. Then, from a knowledge of I_D vs. V_{FG} for the particular transistor design and source bias, it is possible to optimize I_D . Fig. 9 shows how I_D and the signal-to-noise ratio (SNR) change with gate voltage. The curve of I_D vs. V_{FG} was measured and the SNR curve was calculated using this data. It may be noted that the optimum

occurs close to the end of the exponential range of the FET. Since the drop-off of SNR for increasing gate voltage is small, the dynamic range of the charge amplifier can be increased with only a minor effect on low-signal level SNR.

The size of a stage of the CCD output register is determined by the saturation input signal level of the DFGA and by the number of stages in the DFGA. In this device over half of the DFGA area is used by the CCD output register.

There is no clearly defined optimum to the number of stages. Since the fundamental principle behind the DFGA concept shows that SNR in voltage improves as the square root of the number of stages and since the size of each stage of the output register must be increased linearly as the number of stages increases, SNR increases as the one-fourth power of the output register area.

For the twelve-stage DFGA on the 190 x 244 area image sensor, the following performance has been observed. The dynamic range referred to the input is determined by a saturation level of approximately 5×10^4 electrons per picture element and by an RMS noise level in the dark of approximately 10 electrons. The resulting dynamic range, which is defined as the ratio of saturation signal to minimum detectable signal, may be estimated to be:

$$\text{D.R. (input)} = \frac{n_{\text{sat.}}}{n_{\text{min.}}} = \frac{n_{\text{sat}}}{5 r_n} = \frac{5 \times 10^4 \text{ electrons}}{50 \text{ electrons}} = 10^3 \quad (6)$$

The conditions under which this performance was observed were a 1MHz element sampling rate and a 25°C ambient. However, the measurement was made in such a way that the element sampling rate could have been increased to approximately 7 MHz without altering either the output signal or output noise level.

It may be noted that the 190 x 244 image sensor also has a gated charge-integrating amplifier which is capable of handling input signals up to the saturation level of the sensor elements themselves. This signal level is approximately 3×10^5 electrons per picture element.

V. CONSIDERATIONS FOR THE FUTURE

As is evident from the previous general discussion and the device design considerations, device architecture has evolved significantly and the central issue is not "if", but "how". The future undoubtedly holds innovations in design, processing and engineering. Nevertheless, the design options that have been discussed here form the core and future sensors will arise out of a convergence of this set. Even now the value of the buried channel mode is incontestable. High MTF combined with good quantum effi-

ciency is obtained with frontside illumination. The interline transfer organization provides a powerful means to reduce total device area and thereby to increase the feasibility of a device with full TV resolution. Specifically, a 380 x 488 element can be made on about a 10^2 mm² chip. When the recent rate of image sensor evolution is considered, a functional device with full TV resolution will probably be available in the not-too-distant future.

Beyond this goal there will be demands for additional product features and greater cost effectiveness. These demands may result in devices of yet larger total area. In any event, it is certain that future directions of development will be aimed at methods that result in cost reduction and performance improvements.

In comparison to the technological development of imaging tubes, these solid-state devices are at an early stage of evolution. It may be seen, however, from the inherent properties demonstrated by these early devices that CCD area sensors promise to play a leading role in both replacement and new camera markets.

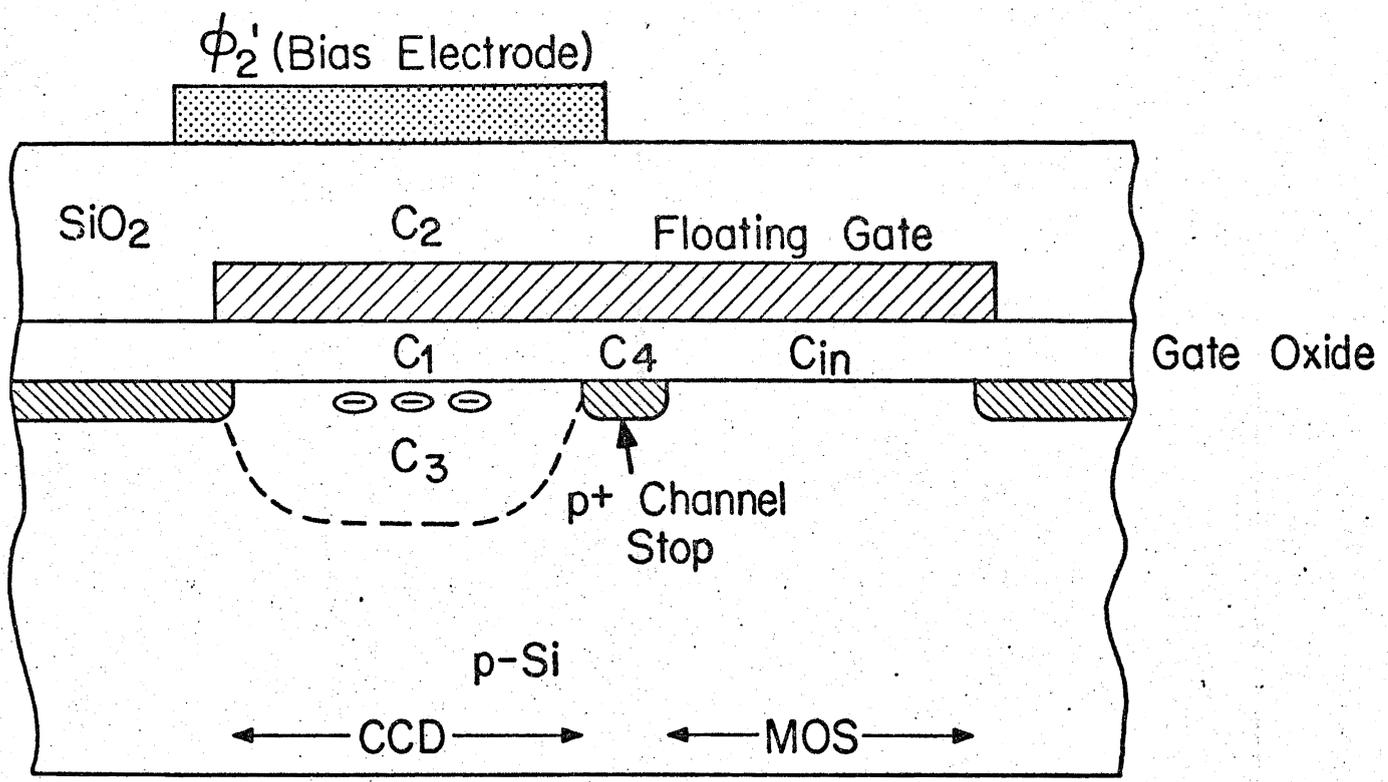


FIG. 8

Cross-sectional view of the floating gate input structure showing the several capacitances used in the analysis.

FIG. 9

The dependence of drain current and signal-to-noise ratio on the voltage of the floating gate in the DFGA.

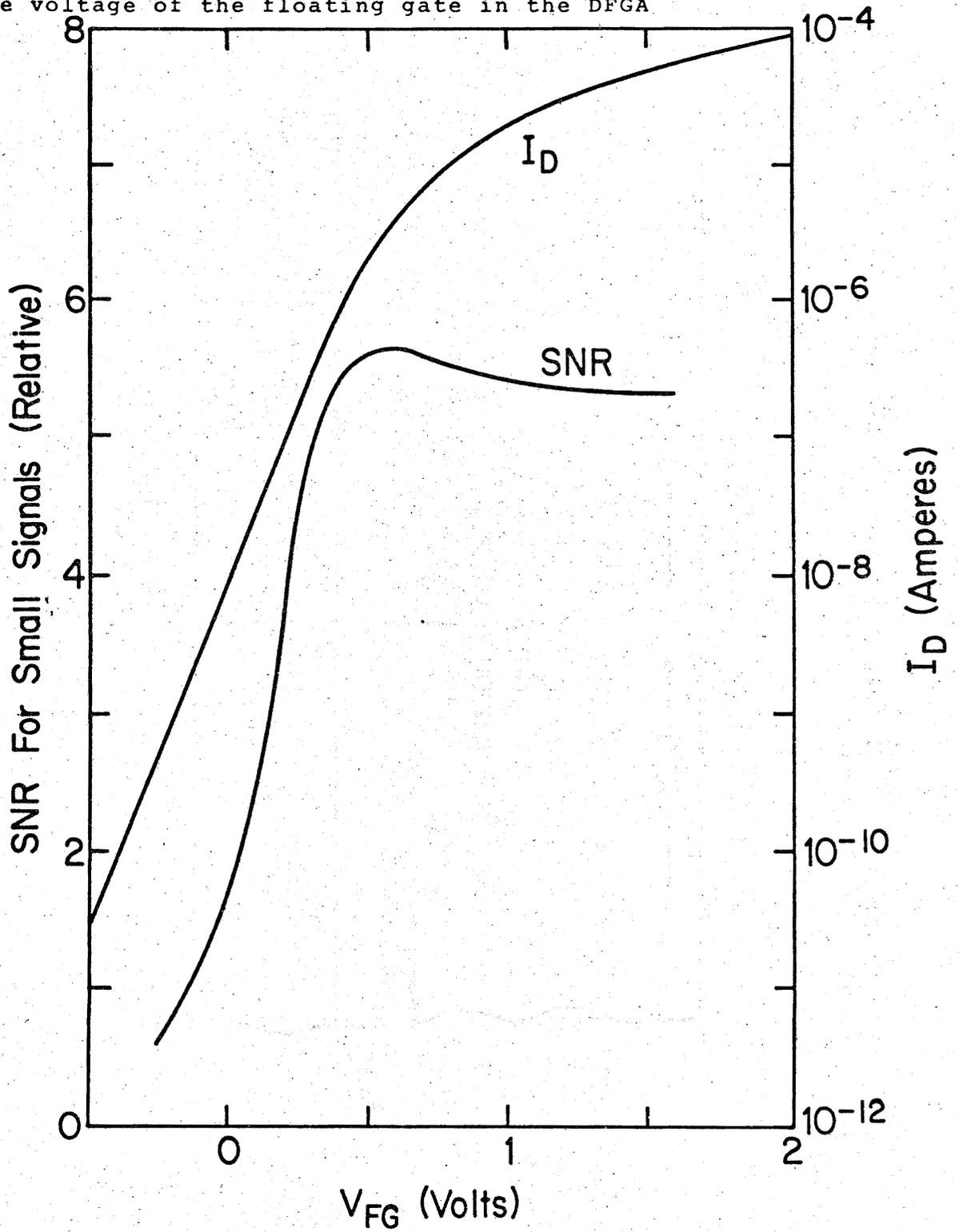
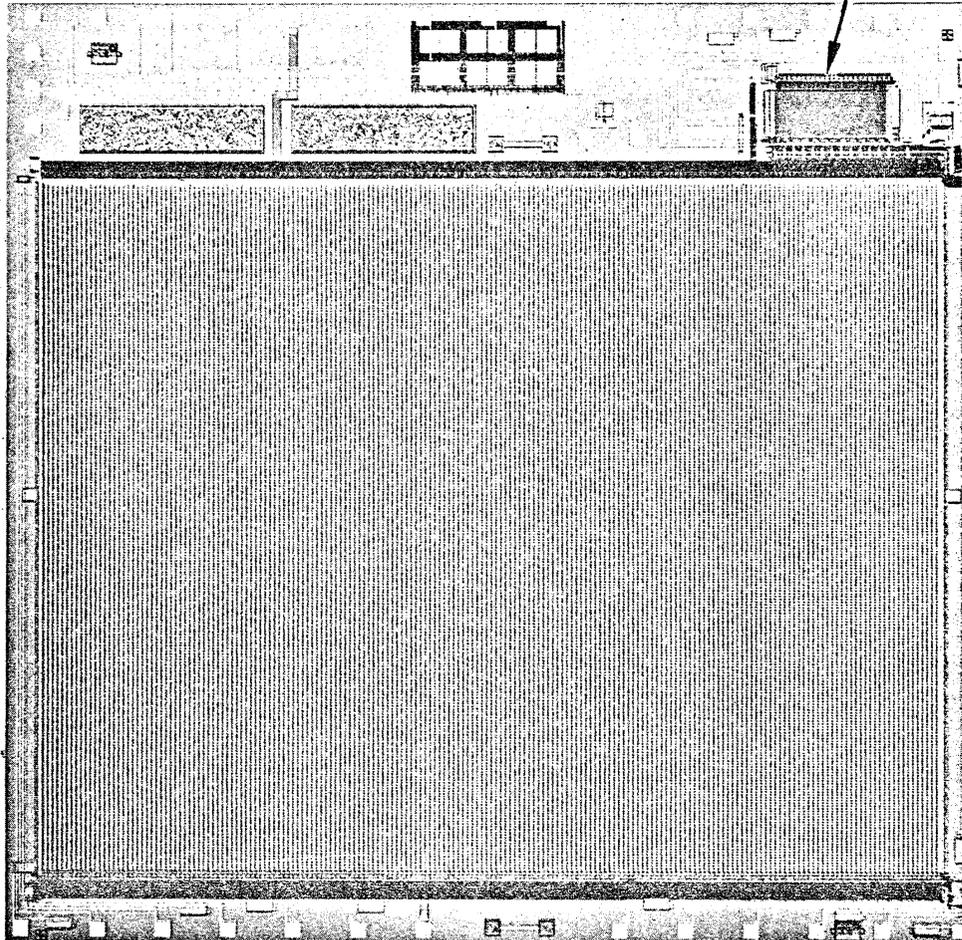


Fig. 4 (top)

Fairchild 190 x 244 area image sensor

DFGA

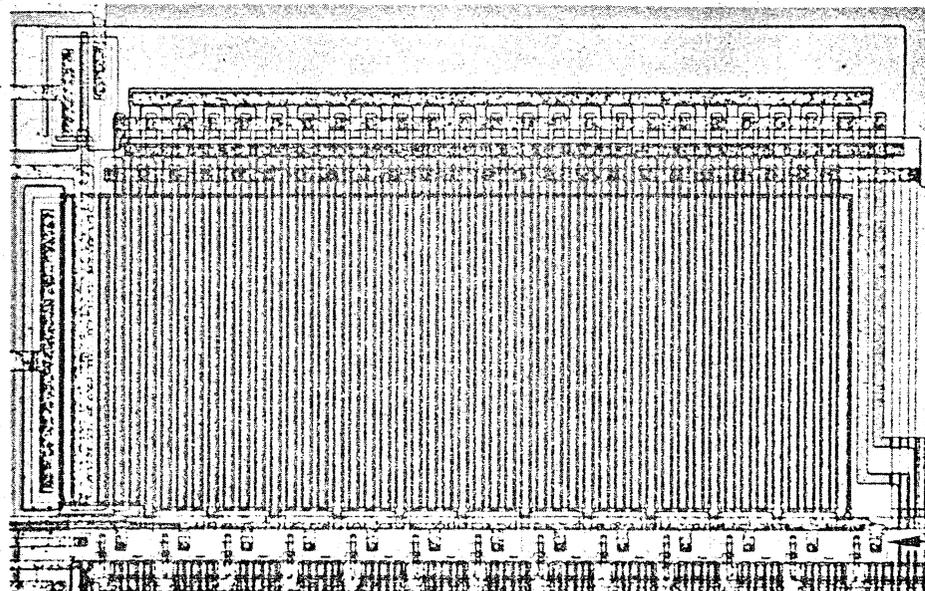


190 x 244
ELEMENT
ARRAY

Fig. 5 (bottom)

Enlarged view of the Distributed Floating Gate Amplifier (DFGA)

OUTPUT
AMPLIFIER



ENLARGED
VIEW OF
DFGA

INPUT
AMPLIFIERS

SIGNAL
INPUT

I_D (Amperes)

on
4



Fig. 5

Image obtained with 190 x 244
sensor