BURIED CHANNEL CCD'S WITH SUB-MICRON ELECTRODE SPACINGS

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ABSTRACT

The requirement for close spacing of the electrodes in CCD devices is well established, and has been emphasised by the advent of bulk transfer structures. Techniques for producing effective close spacing of adjacent electrodes are many and varied, and always involve considerable process complexity.

A technique will be described which enables a single layer metal pattern to be printed with electrode spacings as small as 0.2 micron, and with an intrinsically high yield capability. The degree of process complexity is less than that associated with many of the techniques presently in use for producing CCD electrode patterns. The process has been called the shadow etch technique and is applicable to two-dimensional structures. This technique has been developed from an idea originated by B.D. Williams of these laboratories.

The application of the above technique to buried channel charge transfer devices will be discussed, and the performance of short (32 bit) shift registers fabricated in this manner will be described.

1. INTRODUCTION

Shadow Etch Technology (S.E.T.) enables the restrictions imposed upon minimum rail separations by photolithographic tolerances to be reduced from a few microns to a small fraction of a micron. The ability to relax this spacing clearly has implications in many fields of activity, including the fabrication of small geometry bipolar transistors, dual gate MOST's and bulk CCD's.

Several techniques have been proposed to produce close spacing between adjacent electrodes in charge coupled devices (Refs.1,2,3,4,5). Both polysilicon and double level metallisation have been used successfully and are acceptable for certain applications. In particular, polysilicon electrode systems are useful for imaging applications where the transparency of the electrodes is a useful property, and where the maximum required data rate is well defined. However, limitations in speed are implied by the relatively high sheet resistance of polysilicon layers, and the high inter-electrode capacitance of such systems. Double layer metallisation produces a very small electrode spacing, but realises a definite packing density restriction. A shadowing technique has been described (Ref.6) which produces narrow gaps between single level metal electrodes, but this technique cannot readily be extended to two dimensional arrays.

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The Shadow Etch Technique to be described enables single level aluminium electrode systems to be defined with narrow gap (0.2 microns to 1 micron). The process realises an extremely high yield since both edges of the gap to be formed are defined by a single mask edge. This provides immunity to many mask and photoengraving defects. The technique was conceived for application to Buried Channel CCD structures and will be described in this context. Although the structures fabricated to date have been 3 phase, the process is simplified for 2 or 4 phase systems as will be seen.

2. THE SHADOW ETCH TECHNIQUE

The two commonly used methods of defining aluminium based interconnections on integrated circuits are chemical etching and "float off". Chemical etching is not well suited to closely spaced rails because of lateral etching, the degree of undercutting of the edges which increases the final spacing between the rails. "Float off" does enable the lateral dimensions of the photoresist print to be retained, but there is a definite limit on the width of photoresist fingers which may be printed.

A combination of chemical etching and float off can be employed to generate sub-micron spacings between adjacent electrodes. A first metal layer is etched until it clears, and a well defined overhang of photoresist is formed. The extent of the overhang determines the eventual gap width, and is adjustable by controlled over-etching of the initial metal. Vertical deposition of a second metal layer produces small gaps where the surface is "shadowed" by the resist overhang. In many applications, such as where three phase electrode assemblies are required, it is necessary to re-connect first and second metal layers. This is readily achieved by means of a 'latent image' linking mask which defines the areas to be linked prior to the first metal etch. This print is exposed, but not developed until after the first metal etch, and hence the name 'latent image'. Two and four phase CCD structures do not require this link stage. The process so far has defined all the required narrow gaps, and has left metal everywhere else. A final print and etch stage defines the interconnections and bonding pads. The Shadow Etch principle is illustrated in Fig.1. Fig.2 is a photograph of a CCD shift register fabricated in this manner using aluminium electrodes. Fig.3 shows a Scanning Electron Microscope photograph of a 5000Å gap. The gap width is a function of evaporation conditions when aluminium is employed, and it is thought that gold may be more suitable in this respect. The high yield capability of S.E.T. is emphasised in Fig.4 where the ability to etch around photoengraving defects is shown. All the CCD structures fabricated to date have employed electrode spacings of 0.5 micron. Field breakdown of such a gap occurs in the range 100 to 200 volts and is not a problem.

Metallisation yield on 32 bit linear shift registers and 256 bit SPS arrays has been consistently greater than 90%, with failures in most cases attributable to obvious mechanical scratches.

3. PERFORMANCE OF SHADOW ETCH CCD'S

Although the operation of bulk CCD's has been reported for electrode spacings up to 6 microns, it is generally accepted that narrow gaps are

desirable if spurious potential wells and consequent transfer inefficiency are to be avoided. Our conclusions from two-dimensional potential calculations are that spurious wells are evident for electrode separations greater than 2 microns.

The 32 bit shift registers described below have been fabricated on both ion implanted and epitaxial layers. Ion implanted structures are preferable from yield and layer uniformity aspects, as well as possessing intrinsically greater charge handling capability by virtue of the profiled layer. The test device to be described was constructed and operated as follows:

Type	- n-channel (silicon)
Electrode Width	- 16 microns
Gap Width	- 0.5 micron
Channel Depth	- 1.6 microns
Layer Thickness	- 2.0 microns (ion implanted)
Measured Transfer Inefficiency	- $(\epsilon) \ll 10^{-3}$
Overlap Period of 3-phase clocks	- 50 nS
On-Chip Amplification	- None
Fat-Zero	- None

The passage of a single full well of charge through the register is illustrated in Fig.5, and the integrated charge loss $n\epsilon$ after more than 90 discrete transfers is not discernible. The worst case has been chosen here with the interval between successive full wells being 10 mS, and no fat zero being employed. Since the low capacitance output diffusion is not buffered on-chip, spurious feed through from clock lines has proved a problem. This is principally positive going and has been blanked off the screen in the oscillograph of Fig.5. Using a clock amplitude of 10 volts the system handles an input voltage range of 4 volts representing a modulation efficiency of 80% (approximately).

The feasibility of signal tapping CCD shift registers has been demonstrated by operating the above device in pseudo 2-phase mode. The third phase is held at a DC potential as well as being employed to sense the idsplacement current associated with the arrival of signal charge (ref 8). To avoid signal degradation a virtual earth amplifier is used to sense the displacement current. Fig.6 illustrates the comulative tapped output of the above shift register. The sensing diffusion at the end of the register confirms the arrival of signal with negligible smearing.

Thermal leakage currents of typically 20 to 500 nA/sq.cm. (mean) have been seen for the above devices. Generation appears to be bulk dominated, with the surface apparently well behaved. Surface recombination velocities of 1 cm/sec. are typical, and this figure is attributed to the use of an HCl stabilised gate oxide. Bulk lifetimes of greater than 100μ S will be necessary to bring the bulk generation rate into line with that of the surface.

4. CONCLUSIONS

The feasibility of using single level shadow etch metallisation to fabricate CCD's has been demonstrated. Amidst a host of techniques for producing CCD electrode systems, it is felt that S.E.T. should prove useful in the following specific areas.

(a) The construction of high speed bulk CCD shift registers to operate at data rates > 100 MHz. In this case a four phase clocking system would be employed, thereby involving only two photoengraving steps in the metallisation process.

(b) By reducing aluminium rail spacings to less than a micron, the minimum pitching distance of two or four phase double level (polysilicon/aluminium) systems may be reduced to 16 microns.

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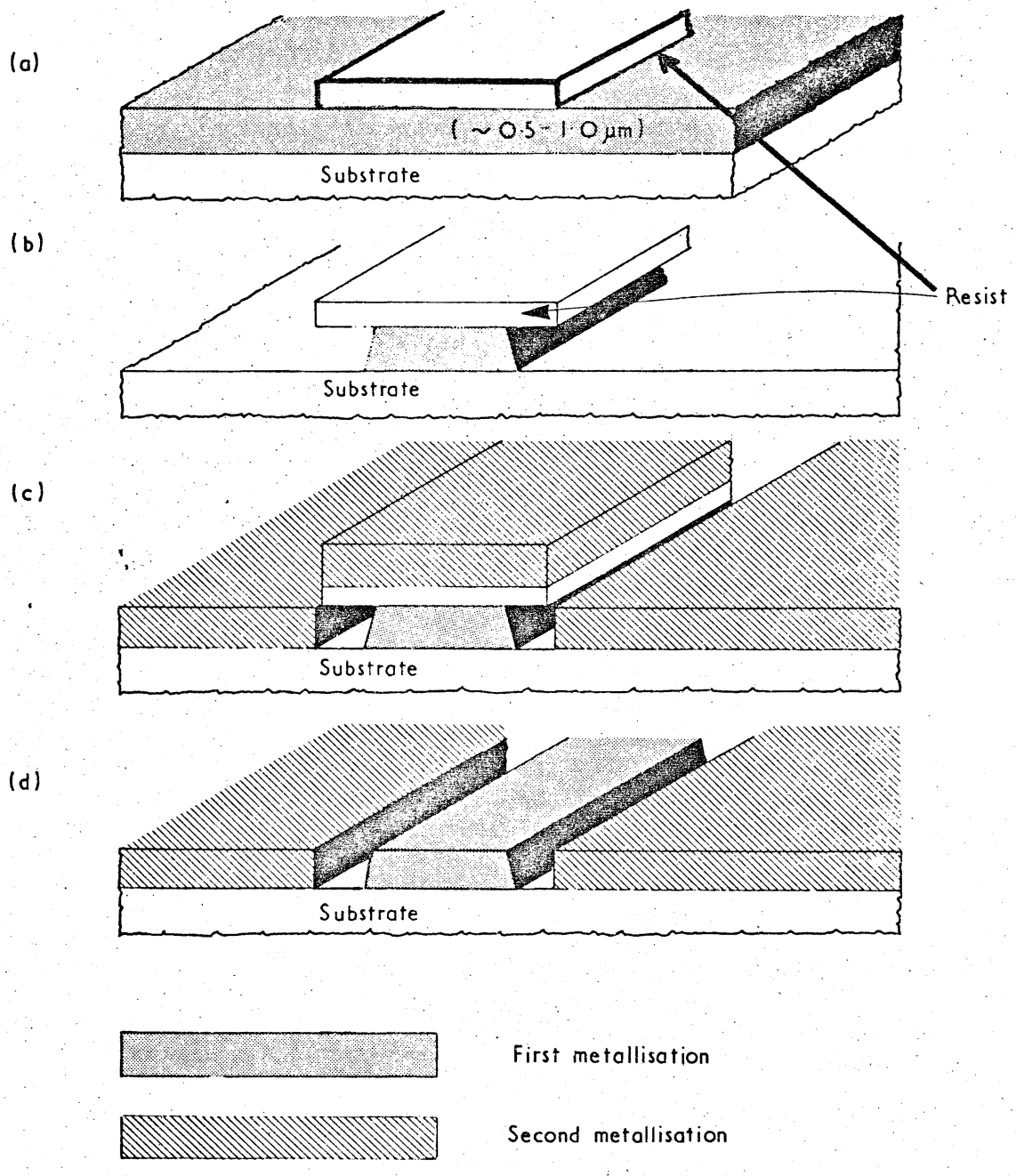
FIG. 1

SHADOW ETCH METALLISATION



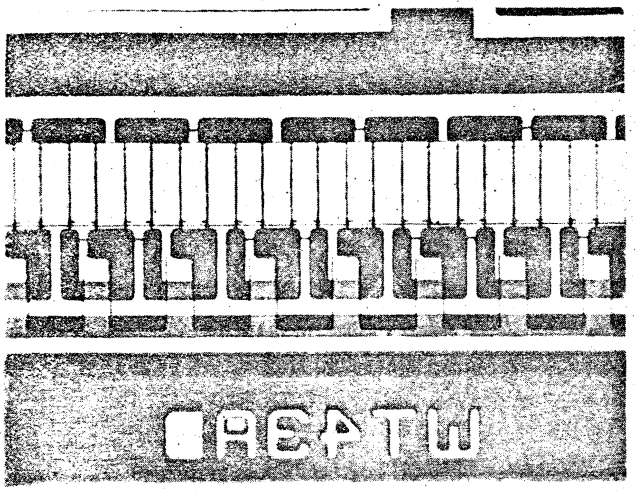


Fig.2

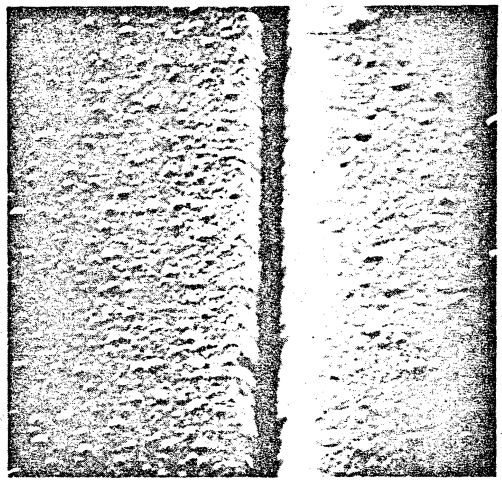


Fig.3

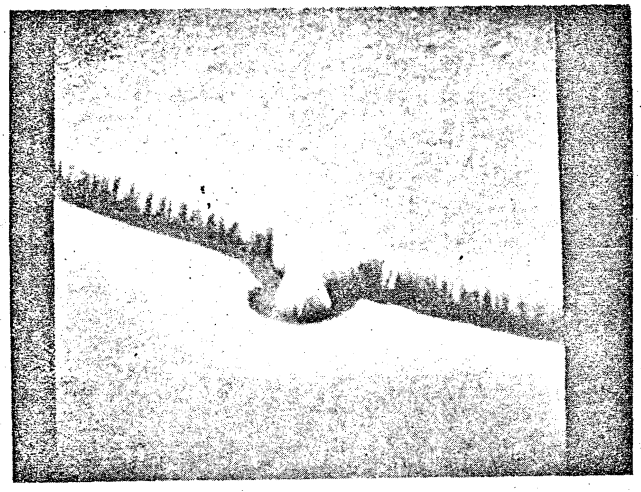


Fig.4

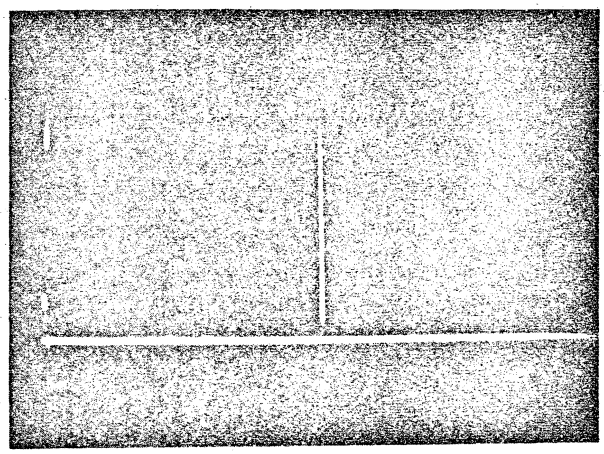


Fig.5

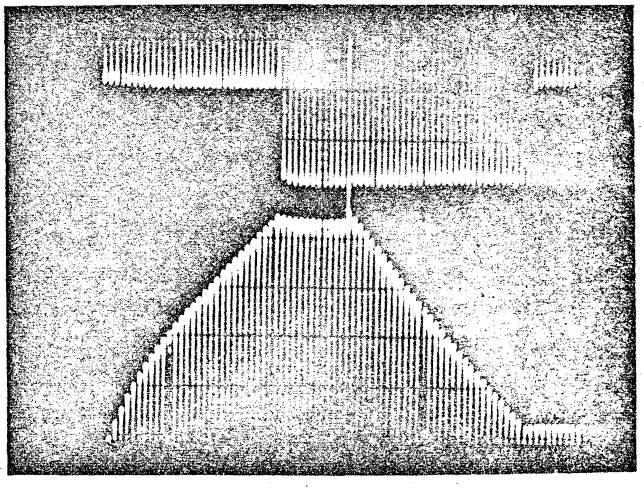


Fig.6