# PERFORMANCE LIMITATIONS OF CHARGE COUPLED DEVICES

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## ABSTRACT

The major performance limitations of Charge Coupled Devices which arise from the effects of charge transfer inefficiency and dark current are described and illustrated with results obtained from a three-phase surface channel device. Further results are then presented for two-phase devices with both surface channel and buried channel operation, and a serial-parallel-serial array, to illustrate means by which some of these limits can be extended. Fabrication complexity and clocking requirements are also considered. Lastly, to summarise the limits of present device performance, a practical operating range for CCDs is defined.

## INTRODUCTION

Many of the applications of charge coupled devices are analogue in nature, including for example the read-out of optically generated signal charges. As analogue devices, however, charge coupled devices have certain performance limitations. Nevertheless, as subsequent sections will show, a wide operating range in terms of frequency and delay is now available with practical devices.

## 1 DEVICE LIMITATIONS

Charge coupled devices are basically analogue, sampled data delay lines. Analogue samples are transferred through the device at the drive frequency $f_o$. From sampling theory, the maximum bandwidth of the data is thus $f_o/2$. Now as each signal sample (i.e. charge packet) moves from element to element in time $1/f_o$, the total signal delay is $N/f_o$ where N is the number of elements in the CCD. The delay-bandwidth product is therefore N/2.

The following sections describe limitations in N and $f_o$ which arise from the effects of transfer inefficiency and dark current. These effects are illustrated with results obtained from a simple 100 element linear CCD. A chip micrograph is shown in Figure 1. This device is fabricated with n-channel aluminium gate MOS technology and operates in the surface channel mode.

### 1.1 TRANSFER INEFFICIENCY

Probably the single most important parameter of a charge coupled device, and which ultimately determines the usefulness of the device, is the charge transfer inefficiency. The cumulative effect of charge being "left behind" during transfer of a charge packet through a number of CCD elements is illustrated in Figure 2. By assuming that the charge is lost as a constant fraction per transfer, the transfer inefficiency may be calculated from the relative magnitude of the residual "trailing" charge $\Delta Q$ to the full charge packet Q:

$$\Delta Q/Q \simeq n\varepsilon$$

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where n is the number of transfers. For surface channel devices $\varepsilon$ is typically in the range $5.10^{-3}$ to $10^{-4}$ (for medium frequency operation).

It can be shown that values for the $n\varepsilon$ product should not exceed 0.1 if the maximum bandwidth capabilities of the device are to be realised in an analogue application. This implies a limit of the order of 100 in the number of elements which can be usefully employed in a surface channel device.

Figure 3 illustrates the variation of transfer inefficiency with clocking frequency. At low frequencies the inefficiency is primarily that due to the effect of surface state trapping. At higher frequencies the rapid increase in transfer inefficiency is largely due to the finite time taken by the charge carriers to diffuse across the width of an element, 30 μm in this case. It is this increase in transfer inefficiency which ultimately sets the limit for high frequency operation; typically 1 - 10 MHz for surface channel devices. Some improvement is to be expected, however, from the use of smaller element spacings.

### 1.2 DARK CURRENT

The CCD is inherently a "dynamic memory" since the stored information disappears with increasing time. The mechanism for this is the accumulation of additional carriers, or dark current as it is called, by generation-recombination centres in the bulk and at the silicon-silicon dioxide interface. Figure 4 illustrates the effect of dark current on device performance; logic signals on the left of the output trace have been stored for 25 msec and show an increased d.c. zero level due to accumulated dark current.

Dark current in silicon CCDs is found to be typically 10 - 100 $nA/cm^2$ at room temperature. These current levels are equivalent to charge generation and collection at rates of between about 5 and 50% of the full charge storage capacity per element per second. A reasonable limit to the total time delay which can be achieved with CCDs is thus about 100 msec.

A more serious problem is that of dark current non-uniformities over an array as ultimately these will become the factor which limits small-signal performance. Improved processing is required to eliminate dark current "spikes", and this appears to be a realistic goal based upon experience with large area silicon vidicon devices.

## 2 IMPROVED DEVICES

The following sections describe improvements which may be used to extend the performance limitations of the simple device.

### 2.1 BURIED CHANNEL DEVICES

Using ion-implantation, the incorporation of a buried channel into any CCD structure is a relatively straightforward exercise, provided that the electrodes are very closely spaced. Close electrode spacings are necessary because the extent of the depletion region in the channel due to the gate potential is very small. Buried and surface channel devices are operated similarly, the only difference being the values of bias and clock voltages employed. With buried channel operation, however, higher transfer efficiency results because contact between the signal carriers and the

interface states is avoided. The speed of charge transfer is also enhanced because the carriers are kept further from the electrodes and are therefore subject to more fringing field effects.

Results have been obtained for operating both surface channel and buried channel devices each fabricated with the same 40 element two-phase electrode structure. An overlapping two-level aluminium-polysilicon electrode technology was employed to minimise electrode separation. Operation of the buried channel device at 8 MHz is shown in Figure 5. The surface channel devices have transfer inefficiencies of typically $5 \times 10^{-4}$ up to 1 - 2 MHz, whereas the buried channel devices have transfer inefficiencies less than $10^{-4}$ (the array being too short for a more precise measurement) at frequencies up to at least 20 MHz.

The buried channel mode of operation is thus capable of an order of magnitude improvement in transfer efficiency and frequency performance over surface channel operation. It is thus anticipated that buried channel devices will be employed for most practical applications of CCD. However, surface channel devices may be preferred for applications where it is necessary to non-destructively tap a signal from an array as the fact that the charge is kept further from the electrodes in a buried channel device makes signal sampling with electrode capacitance techniques considerably more difficult.

## 2.2 SERIAL-PARALLEL-SERIAL ARRAY

Although transfer efficiency limits the maximum number of elements through which charge can be transferred, on-chip multiplexing can extend this limit to realise a high capacity analogue or digital serial memory. Figure 6 shows a micrograph of such a structure currently under development. The device contains 1024 elements. Charge transfer in the 32 x 32 array of elements is organised on a 'Serial-Parallel-Serial' basis. Charge packets are shifted into the upper input serial register at clock rate $f_o$, then shifted in parallel one row at a time down an array of vertical channels to a lower output serial register for sequential readout. As the array is of 32 x 32 elements, the clock rate for the parallel transfers is $f_o/32$. The transfer electrodes on the parallel array are common to all the parallel channels and the channels are defined by diffusions in the silicon. Figure 7 shows operation of the array with digital inputs at $f_o$ = 1 MHz.

The main advantage of the serial-parallel-serial array is that the number of transfers made by any charge packet increases as the sum of the number of horizontal and vertical elements, whereas the total number of elements (i.e. the effective storage capacity) is the product of these two numbers. Thus, with the example shown, a memory of 1024 elements has been achieved with charge transfer through only 64 elements. The other basic parameters of the CCD remain as before. There is a need, however, to generate rather complex drive waveforms.

It should be noted that the advantage of the serial-parallel-serial organisation increases with increasing size. Hence chip size and yield, rather than transfer efficiency, will ultimately determine the maximum number of elements for this type of array. Certainly 16k elements would appear to be feasible with present technology.

## 3 SUMMARY

Limitations of device performance which have been described are summarised graphically in Figure 8. It can be seen that practical CCDs can operate over a wide range of frequency and delay. Also included are results for acoustic wave devices to illustrate the complementary operating range of this other technology.

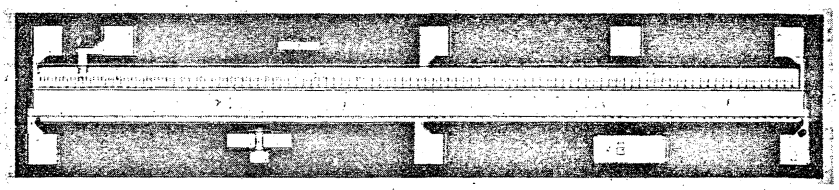


Figure 1 100 ELEMENT THREE-PHASE LINEAR CCD

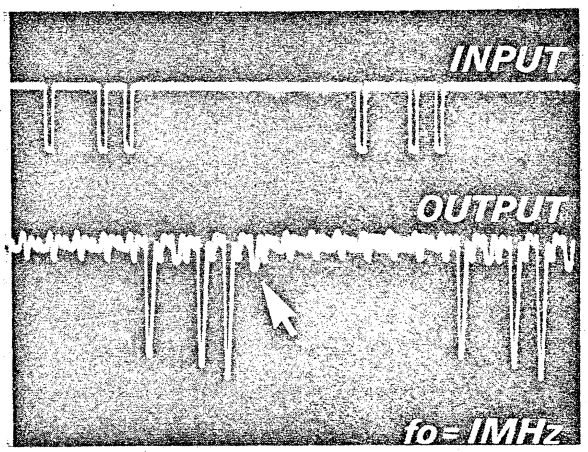



Figure 2 DIGITAL OPERATION SHOWING CHARGE RESIDUAL (arrowed) DUE TO TRANSFER INEFFICIENCY

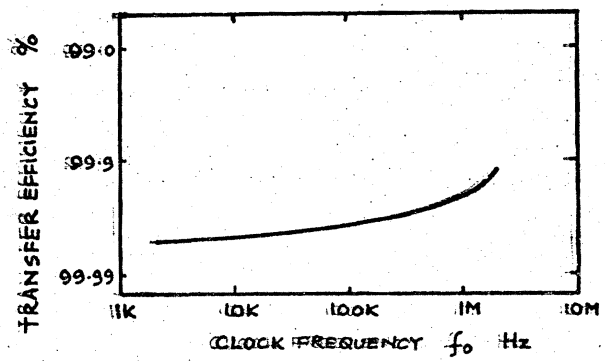



Figure 3 VARIATION OF TRANSFER EFFICIENCY WITH CLOCK FREQUENCY

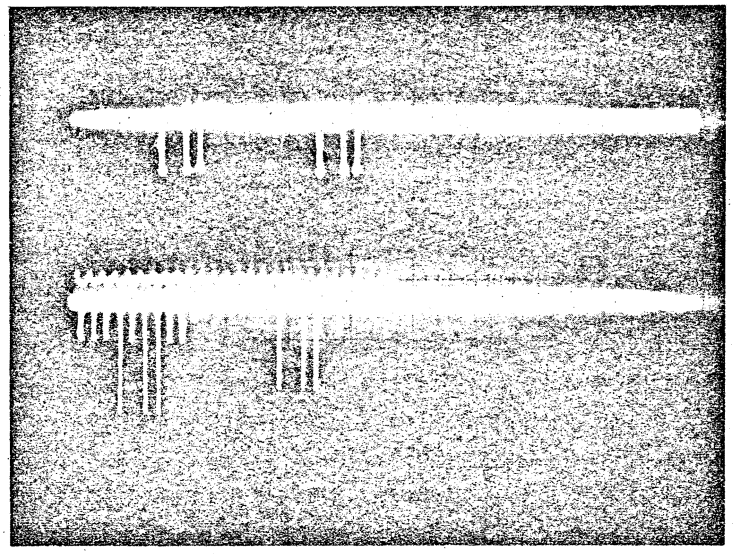



Figure 4 EFFECT OF DARK CURRENT

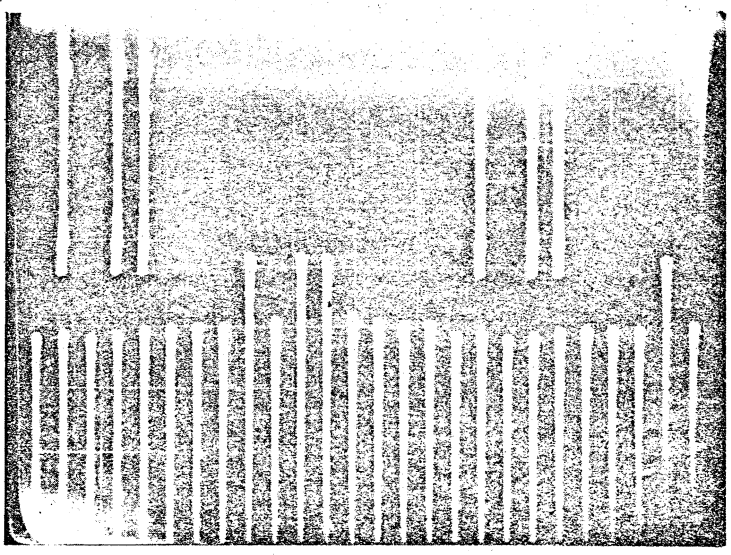



Figure 5 OPERATION OF A BURIED CHANNEL CCD, $f_o$ = 8MHz

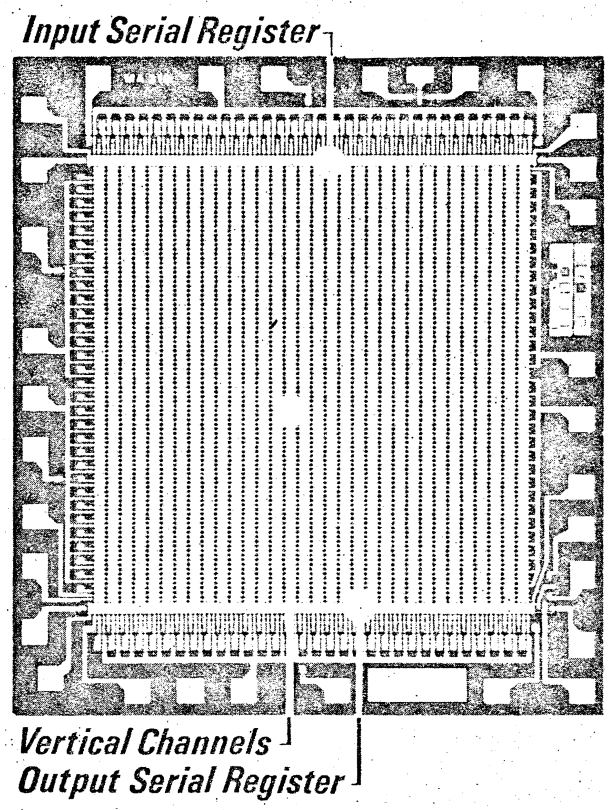
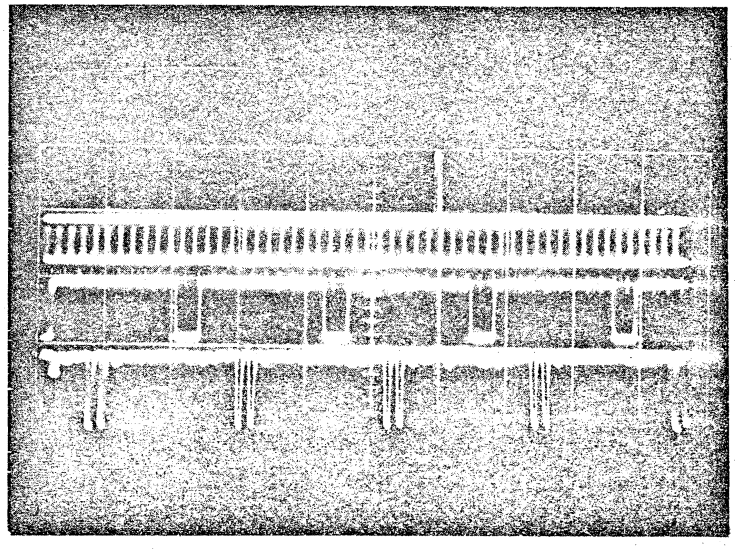



Figure 6 1024 ELEMENT SERIAL-PARALLEL-SERIAL ARRAY



Some of the drive waveforms

Input

Output

Figure 7 OPERATION OF 1024 ELEMENT ARRAY WITH DIGITAL INPUTS, $f_o$ = 1 MHz

Figure 8 PRESENT LIMITS OF CCD OPERATING RANGE