CCD TECHNOLOGY

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ABSTRACT

Since CCDs are MOS devices, the available integrated circuit processing technologies have shaped, and will continue to shape, the designs and performance of CCDs. Particularly in industrial facilities the adoption of current methods of fabrication shortens development times and eliminates the risk and cost of developing new technologies. If designs that use large minimum dimensions are also adopted then large high capacity memories and image sensors can be readily realized. The technology of CCDs then extends to ways of organizing the basic shift registers to perform necessary functions such as imaging, memory and signal processing, and the design of on-chip input and output circuits to give linearity and low noise. The state-of-the-art in all these areas is described. The performance of both surface and bulk channel CCDs is already at a high level and results obtained with devices are presented.

The most significant developments now taking place lie in several directions. In the processing technology, improvements in photolithography will make it easier to fabricate arrays with more elements. Careful control of the fabrication processes will reduce dark current to very low values. In signal processing we can expect to see implementation of analog and digital functions with LSI custom CCDs.

I. HISTORICAL ELECTRODE STRUCTURES

The original concept of a CCD was simplicity and elegance itself (ref 1). All that had to be done was to oxidize a silicon wafer and then etch one level of metal into little capacitors. Charge could then be transferred from one capacitor to the next. The charge could be generated either with light or by applying a large voltage spike to one capacitor and generating carriers by avalanche. The charge was detected by turning off the electrode and dumping it into the substrate from which a signal current was obtained. These techniques were applied to 2 (ref 2), 8 and 27 electrode devices and successfully demonstrated CCD action. In the latter cases the 3-phase interconnections were made to off-chip buses by stitch bonding and the elements were surrounded by a metal edge guard which could be biased into accumulation to prevent unwanted carriers from entering the potential wells. This simple technology then began a decline into increasing complexity, which is still continuing. A diffusion was introduced to make input and output diodes and diffused crossunders for the clock phases. Thick field oxide was used to prevent unwanted channels. The first CCD made in this way was p-channel, had eight elements and demonstrated delay and rudimentary image sensing capabilities (ref 3). It also demonstrated poor charge transfer efficiency on dry days unless one breathed on the device so as to provide a conducting film in the gaps. However, on n-channel devices the fixed charge in the oxide keeps the channel turned on and more stable devices with transfer inefficiencies as low as 2×10^{-4} were obtained in a 96-element device (ref 4). Also made were 13,000-element area image sensors using this electrode structure (ref 5). However, the 1 meter length of 2-3 μm gaps necessary for good performance and which had to be free of shorts were

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impossible to fabricate consistently, although excellent demonstration models were obtained. A 120,000-element device made in a similar way has also been announced (ref 6).

II. CURRENT ELECTRODE STRUCTURES

Tricks can be used to form conducting layers above (ref 7) or below (ref 8) the gaps, but mostly overlapping electrode structures (refs 9-11) of either the 4-, 3-, or 2-phase type are preferred. Schematic cross sections of these structures are illustrated in Fig. 1. These structures can all be

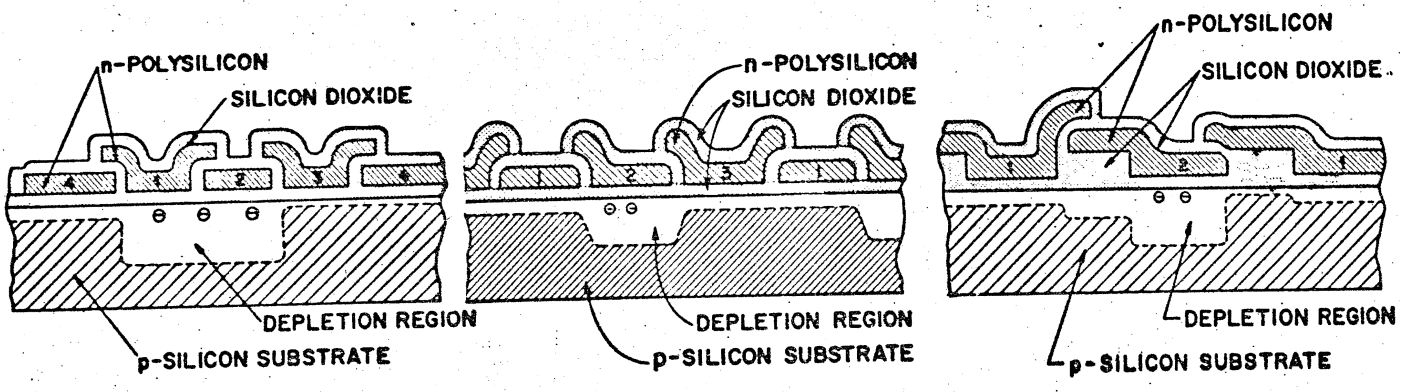

Fig. 1 Schematic cross sections of overlapping electrode 4-, 3-, and 2-phase electrode structures.

made using at least one level of polysilicon, which is defined and oxidized prior to subsequent levels of polysilicon or metal. This type of processing is similar to that used in self-aligned gate MOS technologies and hence is compatible with many existing MOS production facilities. It also permits the fabrication of high performance peripheral circuits on the same chip, which becomes increasingly important as devices become more applications oriented.

Before discussing the details of the above structures, it is appropriate to say a few words about the devices of which these structures may form a part. There are many applications, where large numbers of elements on one chip are necessary, such as area image sensors, memory devices and other applications in signal processing where several channels are processed in parallel or multiplexed. Thus to be able to take full advantage of the charge-coupled principle, it is necessary to be able to fabricate with high yield devices with very many elements. There are also other considerations of speed, transfer efficiency and cost, which force small electrode dimensions on the designer. The width of the transfer channels will be chosen according to the application. In recirculating memories this is defined by the size and sensitivity of the regenerators, in area-image sensors by the spatial resolution required, and in analog signal processing devices by the required signal-to-noise ratio in the output signal.

We will first consider the problems associated with the present MOS technology using conventional photolithography. The exposure and photoresist combination itself has a resolution limit that is on the order of 2 μm, but the existence of many defects of these dimensions both in the photoresist and on the mask make this an impossible design rule for large-area devices. In addition, as the mask is used additional defects are introduced. This is illustrated (ref 12) in Fig. 2 which shows the increase in defect density as a function of the number of wafers exposed and the distribution of defect size in a used mask. Many of the defects in a used mask are in excess of 5 μm in diameter.

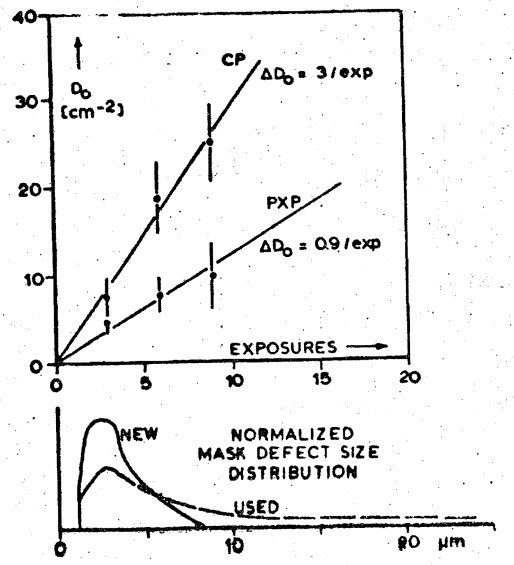

Fig. 2 Summary of defects on clear emulsion masks generated by contact (CP) and proximity (PXP) printing.

If we now return to the electrode structures illustrated in Fig. 1 and define a minimum dimension L of either a gap or an electrode and a maximum registration error of R ($< L/2$) then the minimum cell sizes for the 4-phase structures, the 3-phase, and the 2-phase structure are 4(L+R), 3L and 2L, respectively. In addition, in the latter two structures shorts between electrodes on a given level (intralevel) that might be caused by photolithographic defects are not fatal to the whole device since they are always at the same potential. In addition to the small cell size of the latter two structures, no contact windows, another yield determining feature, are required for each electrode. Only gross windows for the metal buses and any peripheral circuitry are required.

The above structures all place reliance on forming a near perfect insulator on the metal electrodes. Using polysilicon for the electrodes, this is readily attainable by using thermal oxidation. The disadvantages of depositing and oxidizing several layers of polysilicon are the extra processing steps, which require extra processing time and can increase the dark current. However, the use of polysilicon is an established and reliable MOS technology, which gives controllable flatband voltages and self-aligned MOSFETs for peripheral circuits. If phosphorus doped polysilicon is used, resistivities of 10-20 ohm per square can be obtained, which is adequate for even television image sensors, without the need for buttressing the electrodes with a real metal. Anodized aluminum (ref 13) is another contender to replace the polysilicon. Stability and radiation hardness are aspects of the choice of the fabrication technology that are also relevant. However, in contrast to normal MOS devices, changes in interface state density and dark current are now important, whereas some CCDs can be quite tolerant to changes in flatband voltage.

III. A 3-PHASE, 3-LEVEL POLYSILICON TECHNOLOGY

In fabricating our own devices we are using (100) p-type silicon to give us low interface state densities, growing 1500 Å of gate oxide and depositing undoped polysilicon. This is doped with phosphorus, defined and oxidized with a dry oxide. The process is then repeated twice for the 3-phase devices. Contact windows are opened and a Ti-Pd-Au metallization is used for rails and bonding pads. Careful control of the material, the cleaning processes and the furnaces, the use of gettering and a correct processing sequence are all required to obtain low dark current.

A technology is only as good as the product so I would like to present one or two experimental results. An n-channel analog delay line with 256 (30 µm) elements with 3 levels of polysilicon and a channel width of 200 µm is one device that has been well characterized (ref 10). Figure 3 shows the charge handling capability and the transfer inefficiency ε as a function of the pulse amplitude. The limiting value for ε of 5×10^{-5} is attained at

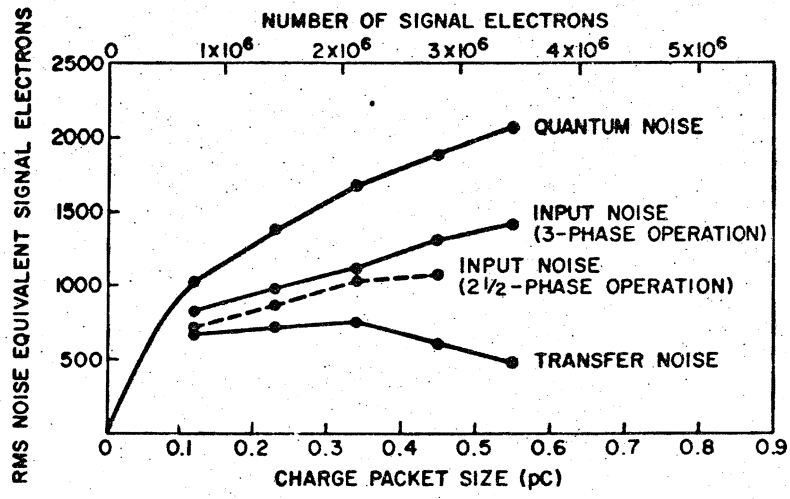

Fig. 6 Transfer noise spectrum in a SCCD as a function of frequency.

These results show the merits of an overlapping electrode structure and the low density of interface and bulk states in the SCCD and the BCCD, respectively. Using measurements of both transfer loss and noise in the SCCD, we determine (refs 15,16) a uniform surface state density of 1×10^{9} cm^{-2} eV^{-1}. Our measured bulk state densities are given in the previous paper (ref 14). The limits that these values place on the performance of an analog delay device and an area image sensor are seen in Table I and Table II.

TABLE I
NOISE EQUIVALENT SIGNALS IN 500-LINE CCAIS AT LOW LIGHT LEVELS
(Active Element Area 20×30 μm^2)

Noise Source	SCCD	BCCD
Input Noise of Background Charge	200(70[a])	not required
Transfer Noise	450	20-80
On-Chip Amplifier Noise C_o=0.2 pF	180	180(few electrons[b])
Dark Current Noise (10 nA/cm^2)	100	100(10[c])
Total Noise Equivalent	540(≈500[a])	≈220(≈20[b,c])

TABLE II
NOISE EQUIVALENT SIGNAL IN 256 ELEMENTS DELAY LINE
(Active Element Area 200×30 μm^2)

Noise Source	SCCD	BCCD
Input Noise of Background Charge	600-900(220[a])	not required
Input Noise of the Signal	600-900(220[a])	600-900(220[a])
Transfer Noise Assuming	720	70-370
On-Chip Amplifier Noise C_o=0.2 pF	180	180(few electrons[b])
Dark Current Noise (1 msec delay, 10 nA cm^{-2})	60	60
Total Noise	960(770[a])	720(230[a,b])
Maximum Signal for V_p=14 V	40×10^6	20×10^6
Dynamic Range	94 dB[a])	99 dB[a,b])

(a) Theoretical limit given by $\sqrt{\frac{2}{3}\frac{kTC}{q}}$.

(b) Use of ideal amplifier.

(c) Cooling by 60°C.

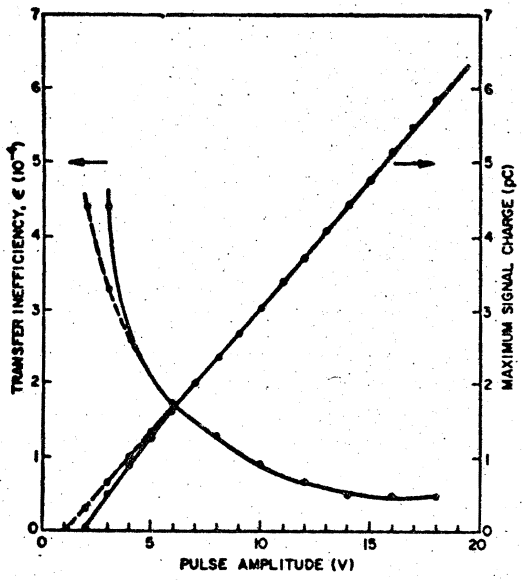

Fig. 3 Charge handling and transfer inefficiency in a 3-phase 3-level polysilicon overlapping electrode CCD as a function of operating voltage.

15 V but useful values of 2×10^{-4} are obtained at only 5 V. The limiting value of ε is maintained for drive frequencies of 10^3 Hz up to 8×10^6 Hz. Figure 4 shows the output from the surface channel device both without and with a background charge when two groups of ONEs are passed along the device separated by 18 and 2000 (not shown) ZEROs. The quantitative effects of the percentage of background charge on the leading ONE and the first ZERO behind the group of ONEs is shown in Fig. 5 for both a surface (SCCD) and a bulk channel (BCCD) device (ref 14). As can be seen the BCCD is significantly better without a background charge. A measurement of transfer noise (ref 15) is shown for the SCCD in Fig. 6. This figure also shows measured input noise and quantum noise.

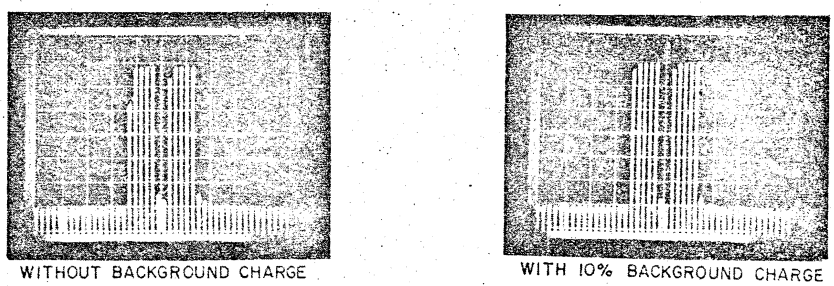

Fig. 4 Response of SCCD to a pulse sequence.

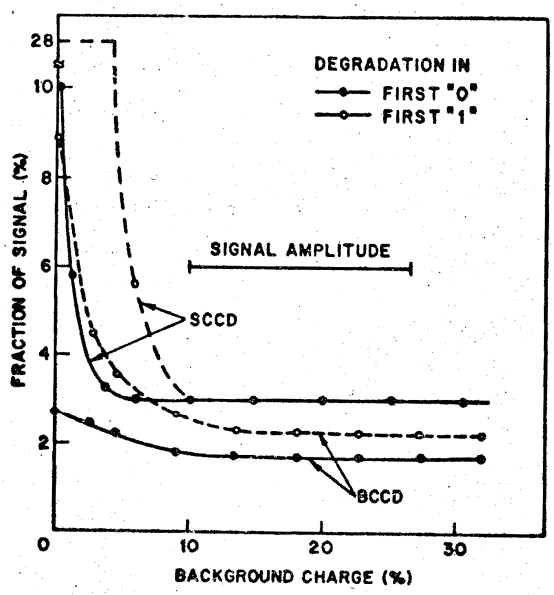

Fig. 5 Quantitative summary of pulse response as shown in Fig. 4 for SCCD and BCCD as a function of background charge.

IV. DESIGN OF CCDs

The organization and design of a CCD to carry out a specific function is a technology all of its own, that must be tailored to one of many particular applications. In designing a full resolution television image sensor where ultimately there may be one-quarter million elements it is important first and foremost to choose an organization that permits the simplest and highest yielding electrode structure to be used. This can be accomplished with the frame transfer organization (ref 4), which by using interlace (ref 17) gives a TV compatible signal. The requirements on transfer efficiency, could be realized using either 2-, 3- or 4-phase overlapping electrode structures. The cell size is determined by the diffusion of the carriers in the bulk and in our devices was made 48 μm along the channel with a 30 μm pitch between channels. A photograph of a camera and a 256×220-element device (ref 18) is shown in Fig. 7. The result obtained with this camera (ref 18) is shown in Fig. 8. There are several possible characteristic defects (ref 5) that can mar the performance and yield of these devices. These defects arise either from defects in the photolithography or etching or from excess recombination generation in the silicon. All of these are a function of the processing technology.

The ability to make a small element size (16 μm = 3×5.3 μm) using the 3-phase overlapping electrode structure has permitted us to make a high resolution, 1600-element linear image sensor (ref 19) with a lateral transfer into one register. The low transfer inefficiency of 3×10^{-5} obtained with this device permits high resolution linear image sensing with 800 line pairs limiting resolution to be performed.

At least two organizations of memory devices are being developed by several organizations. These consist of the serpentine arrangement with regeneration and multiple taps for applications requiring short read/write latency (μsecs) and a serial-parallel-serial arrangement for a more compact arrangement with longer latency (msec). The former arrangement requires considerable design technology in the peripheral circuits such as regenerators, taps, tap decoding, etc., but will function with a low performance transfer structure. The number of elements between regenerators and the idling power are primarily controlled by the dark current in the transfer channel. In the serial-parallel-serial memory, the exciting possibility of multilevel storage exists, but the number of possible levels and hence the capacity of the memory will be primarily controlled by the transfer inefficiency and the dark current.

In analog signal processing devices different considerations are important in different applications. In analog delay and some filtering applications, there is normally a need for flat frequency response, low noise and low harmonic distortion. The frequency response (ref 20) is controlled by the value of $n\varepsilon$, which can be <0.1 for many hundreds of transfers. Low noise is controlled by the correct design and operation of input and output circuits and by choosing a technology to give low surface or bulk state densities. In particular one major source of noise is that in the pickup from the clock pulses (refs 15,21). This problem can be avoided by using a differential amplifier, which if used with two parallel registers in the differential mode (ref 22) of operation has certain other advantages. Estimated noise values for a 256-element analog delay device have already been presented in Table II. The reduction of harmonic distortion requires special techniques at the input that eliminate the effects of dynamic conductance of the input gate and the varying depletion capacitance. The surface potential equilibration method (refs 20,23) where the diode is pulsed to a low value to fill the well under the input gate and then reverse biased to

equilibrate the charge trapped in this well is the most linear. A modified version (ref 24) of this technique can give harmonic distortion figures as low as 60 dB. Matched filters, particularly for detection operations have lower performance specifications, whereas transmission transversal filters are especially tough to design. In the latter case non-destructive linear taps probably with variable weighting are required. Design techniques for this important application are presently being investigated.

Another aspect of design technology concerning these functional signal processing devices is the minimization of necessary power supplies, leads to the chip and ancillary chips. This may require the design of simple logic configurations and drivers on the charge-coupled chip itself.

V. DEVELOPMENT ACTIVITY

The most significant developments of CCDs will lie in several directions. In particular we can expect to see improvements in photolithography, both in the ability to make smaller features but more importantly in the ability to make larger devices with greater perfection. Direct electron beam exposure of wafers is certainly possible but a more likely combination would be electron beam systems to form masks followed by X-ray or improved non-contact printing of these masks.

The careful design and control of the fabrication processes to reduce dark current is a problem that will be with us for some time. Low currents < 20 nA/cm^2 on finished devices can be obtained but consistent routine uniform values < 5 nA/cm over 2 cm^2, as required for uncooled image sensors, are difficult to obtain. Our results indicate that the starting material, the cleaning process, cleanliness of the processing facilities and the process sequences each have a profound effect on the dark current. Even the best storage times of simple capacitors pulsed to 10 V can vary from <0.1 sec to >1000 sec on differently processed wafers. I believe that attention to the above aspects with all the careful experiments and monitoring required will lead to an understanding of the mechanisms involved and to devices with very low leakage currents (< 5 nA/cm^2).

The two developments outlined above will make television image sensors with 525 and 625 lines a viable product. I also believe that backside thindown will become a viable process.

We now see the technology being pushed using television image sensors as very visible vehicles because of their uncompromising requirements, but we will see many other products riding along with them and maybe ahead. The cost of a memory using serial-parallel-serial organized devices and hence the extent of their application will be directly proportional to the yield of these multielement devices and inversely to the dark current, which determines the number of levels that can be stored or the idle power. The use of analog CCDs in many signal processing applications promises considerable cost savings, but low dark current again is often necessary to ensure low noise and uniformity. Careful attention to the input and output configurations is required to ensure low noise and linearity. Thus further development of present MOS technologies and careful device design will be essential to the application of CCDs. There are also potential advantages in combining charge-coupled registers with bipolar, CMOS or MNOS elements and this is an area for development. There are also exploratory efforts to make CCDs on other materials than silicon for infrared image sensors.

At this point in time with a good physical understanding of CCDs we can see considerable efforts to firm up on a few CCD technologies, to reduce dark current and to characterize and improve the performance and the peripheral aspects of the devices. However, there is still a real challenge in the

design area where CCD designers and systems engineers must work together to innovate and design completely new analog and digital custom charge-coupled LSI devices for both old and new systems. It is the success or otherwise of these efforts that will define the broad future of CCDs and the pace of development of CCD technologies.

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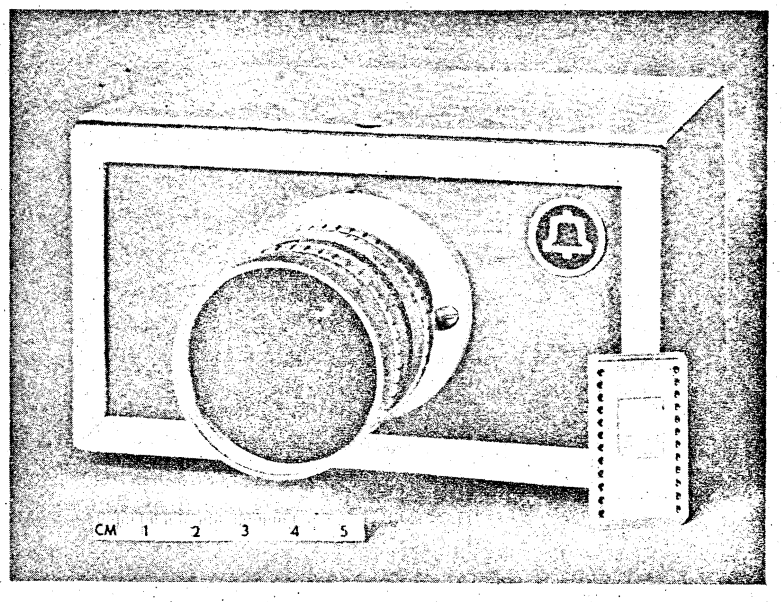

Fig. 7 Photograph of battery operated television camera and 256×220 element CCAIS.

Fig. 8 Photograph of picture reproduced with camera shown in Fig. 7. NTSC scan rates were used.