INFLUENCE OF CLOCKING WAVEFORM ON CHARGE TRANSFER IN THREE-PHASE C.C.D.'s

M.P. Singh*, S.D. Brotherton[ø], P.C.T. Roberts* and D.R. Lamb*

ABSTRACT

An analysis of charge transfer in three-phase C.C.D.'s is presented for the case when they are driven by two-level 'linear' clock pulses. The analysis indicates that the backwards flow loss is an important loss mechanism in 3-phase C.C.D.'s and that the turn-off time of these clock pulses has a very significant role in determining the exact value of the transfer inefficiency. It is shown that in general, longer turn-off times give lower inefficiency and also that efficiency improves with the use of smaller charge packets. Experimental results which confirm the above mentioned trends are also given.

1. INTRODUCTION

Although a three-level stepped clocking scheme was first suggested for operating three-phase C.C.D.'s, the simpler two-level clocking scheme is commonly used for practical device operation. Real voltage pulses have finite turn-on and turn-off times and normally a certain amount of overlap is given between the phase waveforms to ensure proper coupling between adjacent electrodes. Many of the earlier theoretical treatments (for example, ref 1) when analysing the charge transfer process, treat the end of the emptying well as an infinite sink and also assume the voltage on the emptying electrode to be constant during the transfer period. These assumptions are valid only for the three-level stepped pulse operation. For the two-level clocking scheme, charge transfer from the emptying well depends on the potentials and charge densities both in the collecting well and under the other adjacent electrode. Furthermore, the changes of voltage on the 'emptying' electrode must be taken into account. A more exact analysis would include the neighbouring electrodes and solve the differential equations for this entire region taking into consideration the temporal changes of the voltages on all the electrodes. This present study uses such an extended analysis for the transfer process in a 3-phase surface channel C.C.D. driven with a two-level clocking scheme.

Firstly, the charge transfer for various turn-off times of the voltage on the emptying electrode is considered. Tompsett et al. (ref 2) have found experimentally that longer turn-off times improve the transfer efficiency and they reported that the best performance for their device was obtained when a sawtooth waveform was used for the clocking pulses. The present analysis similarly shows that longer turn-off times are preferable since they incur less backwards flow loss, but also that at any given frequency, there is an optimum turn-off time which gives a minimal transfer inefficiency.

*Department of Electronics, The University, Southampton, U.K.

[ø]Mullard Research Laboratories, Redhill, Surrey, U.K.

Secondly, the influence on transfer of the size of the charge packet for a given voltage swing of the clocking pulses, is studied. Boyle and Smith (ref 3) have reported an experiment in which transfer efficiency changed with the voltage swing. This present analysis shows that the use of smaller charge packets (at a given voltage swing) can give higher efficiency and that this change depends on the turn-off time. Attempts have been made to verify these theoretical predictions experimentally and some of these results are presented in this paper.

2. METHOD OF ANALYSIS

The equations describing the charge transfer in a p-channel device (when there is no recombination loss and no increase in carrier density by generation) are: (1) the expression for hole current density,

$$J_p(x,t) = -q\, p(x,t)\mu_p \frac{\partial \psi}{\partial x}(x,t) - q\, D_p \frac{\partial}{\partial x} p(x,t) + q\, p(x,t)\mu_p \mathcal{E}_f(x,t) \tag{1}$$

and (2) the hole continuity relation,

$$\frac{\partial}{\partial t} p(x,t) = -\frac{1}{q} \frac{\partial}{\partial x} J_p(x,t) \tag{2}$$

where p is the hole concentration, q the electronic charge, μ_p the hole mobility and D_p the hole diffusion coefficient. ψ is the surface potential calculated from Poisson's equation reduced to one dimension, and $\mathcal{E}_f$ is a fringing field, separately introduced to take care of the gradient in the surface potential under any one electrode caused by the differing voltages on adjacent electrodes.

These Partial Differential equations are solved in this analysis by the method of Finite Differences, using the Explicit Scheme (ref 4). The surface potential at each time step in the programme is calculated from the following equation (ref 5),

$$\psi(x,t) = -\left[V_o + V(x,t) - (V_o^2 + 2V(x,t)V_o)^{\frac{1}{2}} \right] \tag{3}$$

where $V_o = \varepsilon_s q N_D / C_o^2$ (4)

and $V(x,t) = V_G(t) - V_{FB} - q\, p(x,t)/C_o$ (5)

ε_s is the dielectric constant for silicon, N_D is the net doping density, C_o is the oxide capacitance per unit area. V_G is the magnitude of the applied voltage on the electrode relative to the neutral substrate and V_{FB} is the magnitude of the flat-band voltage. Carnes, Kosonocky and Ramberg (ref 6) have given an empirical formula to be used for computing an 'average' fringing field, assumed constant during the transfer process:

$$\mathcal{E}_f = 13.0 \cdot \frac{t_o}{L} \cdot \frac{V_s}{2L} \cdot \left[\frac{5x_d/L}{(5x_d/L) + 1} \right]^4 \tag{6}$$

Here, t_o is the oxide thickness, L is the electrode length, V_s is the voltage swing and x_d is the depletion thickness when the voltage on the electrode is $V_R + (V_s/2)$. V_R denotes the 'resting' (or OFF) potential.

In the following calculations, the fringing field given by (6) is used during and after the turn-off time of the voltage on the emptying electrode. During the turn-on time of the voltage on the collecting electrode, and during the overlap time, the fringing field is neglected since its contribution will be small by comparison with the self-induced drift field which dominates the early transfer process. The fringing field under the electrode preceding the emptying electrode is given the same magnitude but the opposite sign to that of the field under the emptying electrode. The effect of the fringing field is neglected in the collecting well.

The gap between the electrodes is assumed to be negligibly small since practical devices with sub-micron gaps are available (ref 7). Since linear edges are easier than, say, exponential edges to control experimentally with reasonably high precision, this study is restricted to linear edges. Practical waveforms for real device operation will have some rounding-off at the corners as compared with the linear assumption used for this analysis. Trapping of carriers by surface states is ignored throughout the analysis. We only consider here the cases when there is no 'fat-zero'.

2. COMPUTATIONAL RESULTS

Numerical solutions are obtained which are applicable to one of our experimental devices. The device comprises a 10 Ω.cm, (100), n-type substrate with a 0.17 μm thick gate-oxide and 20 μm long electrodes with about 0.5 μm gap width. Mobility is assumed to be constant at 100 $cm^2.V^{-1}.sec^{-1}$. A measured value of conductivity mobility along the C.C.D. when operated as a M.O.S.T. with about 200 $V.cm^{-1}$ along the channel is 120 $cm^2.V^{-1}.sec^{-1}$. The resting potential is taken to be 6 volts above the threshold voltage of the device and the voltage swing is 10 volts.

When the voltage on the collecting electrode starts its turn-on, carriers from the emptying well will begin to flow into the collecting well. If the overlap period is sufficient, the charge packet will divide almost equally between these two wells. As the voltage on the emptying electrode turns off, a further charge transfer will occur. At the end of the turn-off time, when the voltage has reached its resting value, there is still some charge remaining. The value of the turn-off time used will determine the amount of this charge remaining at this time. Depending on the voltage V_R, recombination may occur or be totally absent. In this study since V_R is sufficiently large, it will be assumed that the recombination loss never occurs.

This charge remaining under the 'emptying' electrode, in addition to continuing to flow forwards can also flow backwards since there is no potential barrier. Thus a certain fraction of the remaining charge will join the following packet. Smaller turn-off times, though enabling a faster transfer rate at the beginning, will now cause a greater amount of charge to be lost by backwards flow. However, for turn-off times approaching the total time available for transfer at a given clock repetition frequency (one-third of the clocking period less turn-on and overlap times) the charge still remaining in the emptying well has no time to flow forwards. Thus for a given operating frequency there will be an optimum turn-off time and Fig. 1 (Curve A) gives the predicted result for 1 MHz clock frequency when the signal size is such as to fill the potential well.

Since the backwards flow loss is solely determined by the turn-off time used, changing the frequency of operation with a fixed turn-off time and packet size should not affect the value of inefficiency except at high frequencies. Fig. 2 shows the predicted inefficiency as a function of frequency for two different turn-off times (A - 40 ns and B - 160 ns).

If the signal size is such as only to half fill the well, inefficiency vs. turn-off time follows the Curve B of Fig. 1. This improvement in transfer efficiency can be explained as follows. During the initial stages of the turn-off, for the same reduction in the electrode voltage, a greater fraction of the smaller packet will be transferred since the net current densities are almost the same. At a later stage in the turn-off there will be greater potential gradients developed for partially filled wells. Consequently after the turn-off time, there will be a smaller percentage of the starting charge to be lost by backwards flow. This decrease of inefficiency values for smaller packets will not, however, be monotonic. When the packet is very small, the rate of transfer will rapidly cease to depend on the clock voltage change and will instead be limited by the 'inherent' transfer rate. Therefore very small packets will have a greater inefficiency. Of course, the detailed nature of this effect will depend on the exact rate of turn-off and the fringing field present during the turn-off. Curves A and B in Fig. 3 show the change of inefficiency with fractional filling for two different turn-off times (60 ns and 120 ns) at 1 MHz.

4. EXPERIMENTAL RESULTS

Aluminium gate 3-phase C.C.D.'s using a shadow-aluminisation technique to obtain sub-micron gaps (ref 7) between electrodes of length 20 μm (8-bits) and 11 μm (14-bits) are being made at present. It is planned to fabricate 6 μm-gate devices in the near future. The clock voltages used to drive the devices are derived from high-current capacitively-loaded output circuits. The internal capacitance loading the output is 270 pF (±1%), which permits probing by a Tektronix 10x voltage probe (~ 7 pF, 10 MΩ) without changing the total capacitance by more than 3%. The three phase-locked clock voltages must be closely matched. Overlap time, turn-off time and turn-on time for each of the three phases can be adjusted in synchronism in the pulsing circuit developed by us. These time periods together with the common voltage levels can be set to an accuracy approaching 5% at worst for clock frequencies up to about 5 MHz. The output of the C.C.D. incorporates a simple M.O.S. unity-gain amplifier calibrated as a charge amplifier, and also a reset high-gain M.O.S.T. A small internal 'pad' is provided which permits direct probing of the sense diode/input transistor gate node. The capacitance of this node can therefore be measured directly as a function of the node voltage. The voltage gain from this node to the output of the amplifier can similarly be measured as a function of the node voltage. This on-chip output amplifier is found to be linear to within 5% over a range of at least 6 volts. The response of the output circuit is found to be better than 40 ns rise-time when loaded by a 10x probe and driven from a 50Ω, 10 ns rise-time square wave. The reset M.O.S.T. was designed and is measured to recharge the output node in about 20 ns.

Theoretical analysis indicates that for a given turn-off time, the transfer inefficiency (ε) is expected to change with packet size (Fig. 3). If the transfer inefficiency is very high, then as the packet proceeds along the C.C.D., the reduction in packet size may be sufficient to change significantly the value of the inefficiency for further transfers. However,

for an 8-bit 3-phase device, with an 'initial' inefficiency of 2×10^{-2}, the packet reduces after 12 transfers by only about 12%. This reduction in packet size is expected to cause the value of the inefficiency to change by only a factor of 2. A similar change of inefficiency should result for longer turn-off times since the value of ε will be much lower. Hence the assumption that the packet travels with the same transfer inefficiency all along the C.C.D. is reasonable for efficiency values of the order 2×10^{-2} or below in an 8-bit device. When a ONE is introduced in a stream of ZEROs along the C.C.D., and if the following assumptions are valid:

(1) There is no loss of charge due to recombination,

(2) there is no gain of charge due to generation, and

(3) the inefficiency value remains the same for all the transfers along the C.C.D.,

then the first output charge pulse will be $\alpha^n Q_{IN}$. Here, $\alpha = 1-\varepsilon$, n is the total number of transfers and Q_{IN} is the input charge. Also, the sum of all the output charge pulses will equal the input charge. Therefore, by measuring the first output pulse as a fraction of the sum of all the output pulses, the value of ε can be calculated. In these experiments, the differences between the output voltage pulses are measured to a precision of about 0.5 mV using a Tektronix 547 oscilloscope with 1A5 plug-in differential amplifier and 10x probe. The plug-in has a D.C. comparison voltage facility with fine control; the value of the D.C. voltage necessary to give a 'null' as viewed on the screen is measured by a DVM with respect to a second fixed voltage ($\pm$10 μV).

The input end of the C.C.D. consists of an input diode, whose potential is held appropriately to the bit information, and an input gate which strobes this level in phase with $\emptyset_1$. The fractional filling of the well is measured in these experiments in the following manner. If the first well is 'overfilled', then an output pulse will appear after only 7 bits delay (in an 8-bit device). The output pulse after 7 bits is monitored at maximum sensitivity and the input diode voltage is adjusted to ensure that the first well is only just filled. For any other fractional filling of the first well, the input diode voltage is appropriately adjusted and the sum of the output pulses measured. The fractional filling is the ratio of this sum to the total output of a full well.

The experimental results are shown together with the theoretical predictions in Figures 1, 2 and 3.

ACKNOWLEDGEMENTS

This work has been supported by the Procurement Executive, Ministry of Defence and also by the Science Research Council.

REFERENCES

1. R.J. Strain, N.L. Schryer, Bell Sys. Tech. J. 50, 1721 (1971).

2. M.F. Tompsett, G.F. Amelio, G.E. Smith, App. Phys. Lett. 17, 111 (1970).

3. W.S. Boyle, G.E. Smith, I.E.E.E. Spectrum 8, 18 (1971).

4. G.D. Smith, Numerical Solution of Partial Differential Equations (Oxford University Press, London, 1971), p. 10.

5. H. Hara, Elect. and Comm. in Japan, 54-C, 133 (1971).

6. J.E. Carnes, W.F. Kosonocky, E.G. Ramberg, I.E.E.E. J. of Sol. State Circ. SC-6, 322 (1971).

7. I.M. Baker, J.D.E. Beynon, M.A. Copeland, Elect. Lett. 9, 48 (1973).

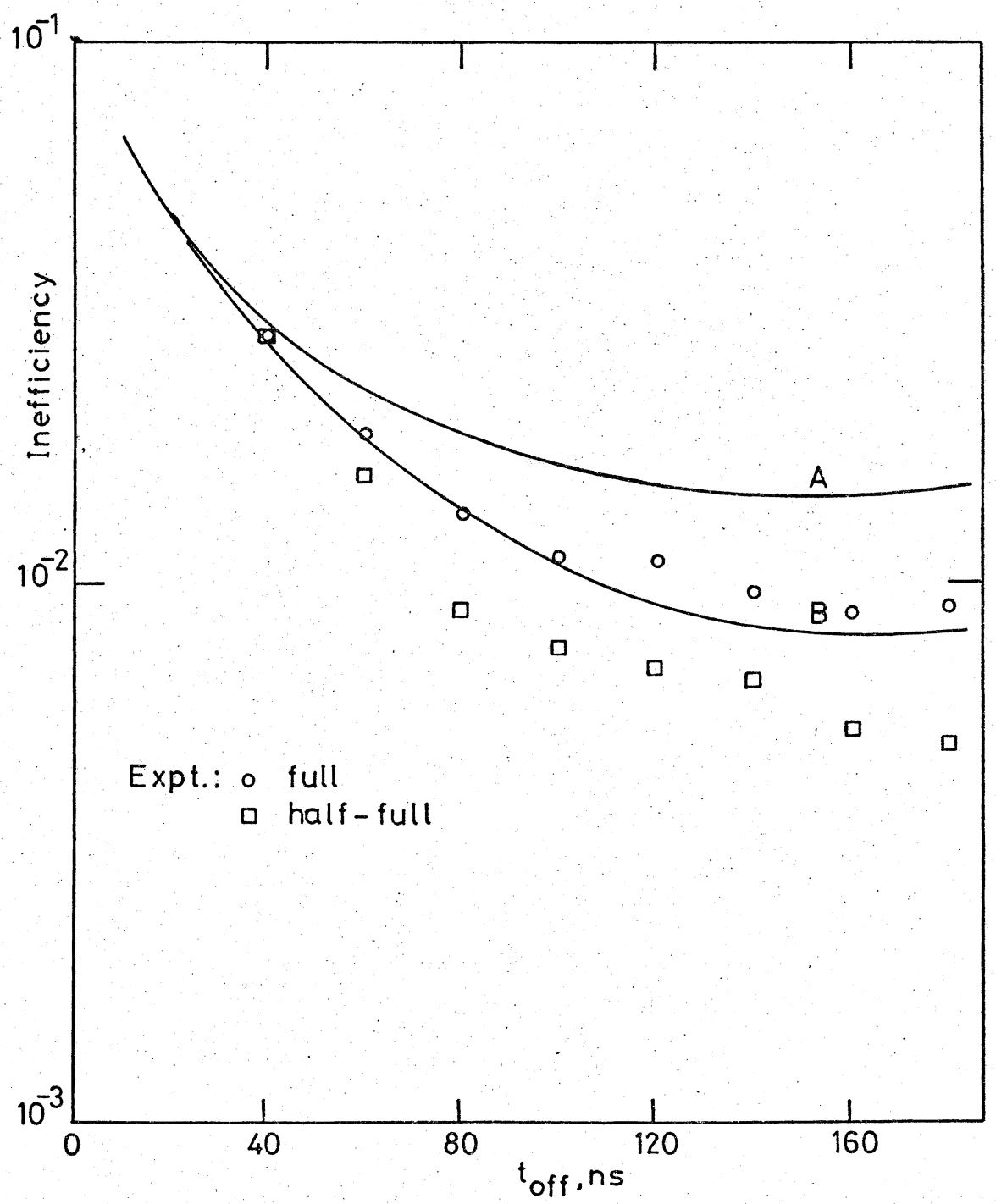

Fig. 1. Inefficiency vs. turn-off time, t_{off}, at 1 MHz (A - full, B - half full).

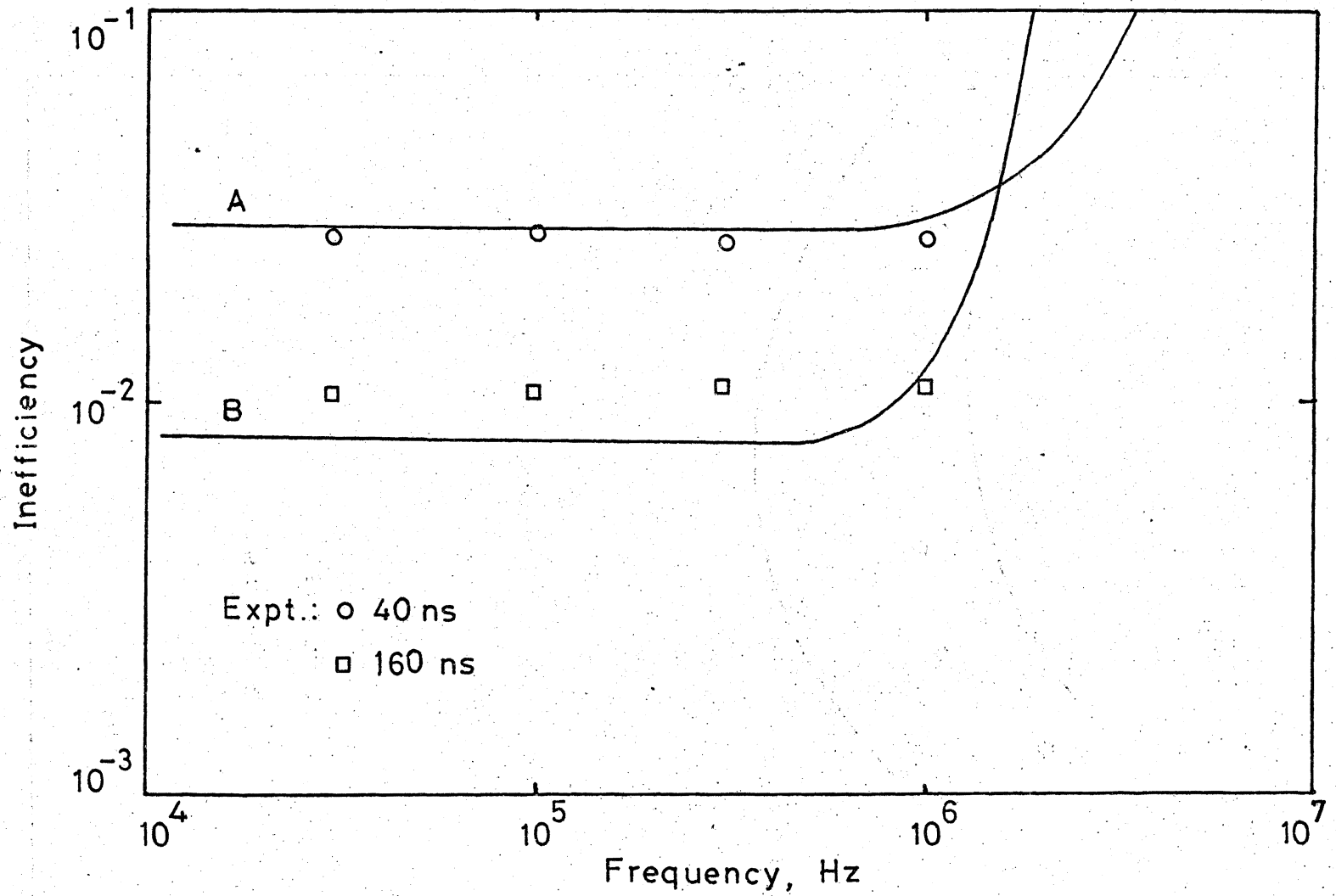

Fig. 2. Inefficiency vs. clock frequency for a full packet (A - 40 ns, B - 160 ns).

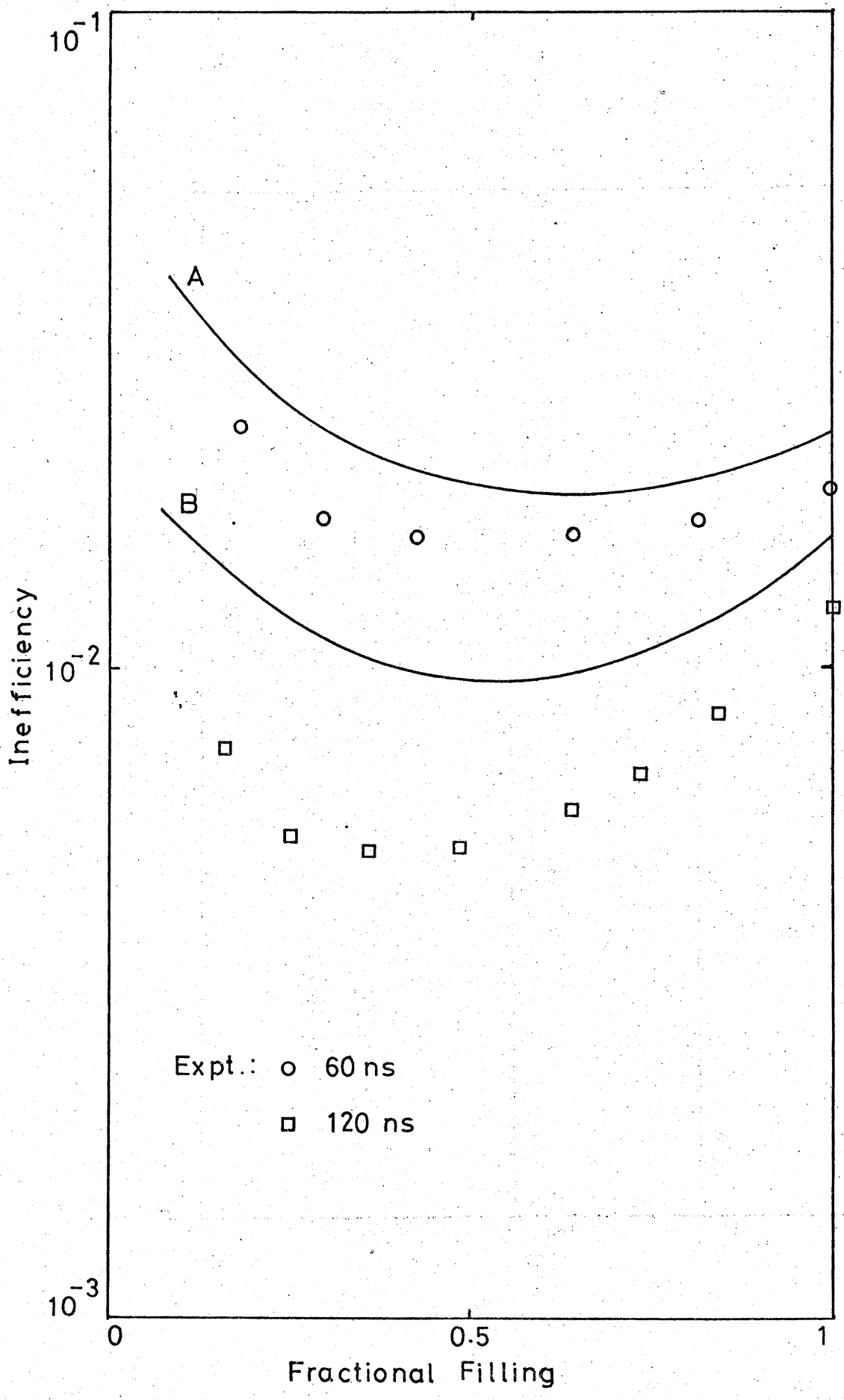

Fig. 3. Inefficiency vs. fractional filling at 1 MHz (A - 60 ns, B - 120 ns).