The Use of CCD Correlators in a Spread Spectrum Communications Example

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ABSTRACT

The general design of a digital programmable CCD correlator is discussed. The concept is treated in broad terms allowing application to a number of problems. The design is then applied to a specific situation: the realization of a multilevel digital correlation detector useful in spread spectrum IFF communication systems. This multilevel detector takes an input analog signal and separates it into in-phase (I) and quadrature phase (Q) components; both I and Q channels are then digitized and each level of each channel is then separately correlated with the corresponding level of the digitized reference code.

By proper demultiplexing of the input to the correlators, the system can handle bit rates that are higher than the basic individual correlator shifting rate. Analog outputs provide an indication of the degree of correlation. Threshold detectors provide a final output signal that indicates when the proper correlation has been obtained.

Finally the design of this system is compared to an existing design using triple diffused emitter follower logic LSI. A substantial savings is realized in both the number of chips and total power consumed.

PROGRAMMABLE CORRELATOR DESIGN

Approaches for implementing CCD correlators have appeared in the literature several times (for a recent reference see (1)). The basic concept used for a digital implementation is to fill a shift register with a received code, determine which shift register positions contain charge and which do not contain charge, and then to "correlate" this information with the knowledge of the desired code. One way to monitor the presence of a signal charge packet is to measure the charge that flows to a CCD storage well gate as the signal charge is introduced under that gate. This idea leads to an implementation (2) such as outlined in Figure 1.

The operation is as follows. All storage gates that should have a full well under them (when the shift register is filled with the correct sequence) are connected together. All the remaining gates, which of course should be empty when the correct sequence is received, are also connected together. The gates are precharged and allowed to float. Now each gate that has charge transferred under it will require a corresponding amount of charge to flow to that gate from the capacitor to which it is connected. Thus each gate that receives a "1" bit will decrease the voltage across its corresponding capacitor by a specific amount. The "1"s capacitor in Figure 1 will decrease by ΔV for each correctly received "1" bit, and the "0"s capacitor will decrease by ΔV for each incorrectly received "0" bit. The differential voltage across the two capacitors yields a direct measure of the degree of correlation of the desired sequence and the received sequence. This is treated quantitatively in Table 1.

The implementation shown in Figure 1 can be

expanded to a sequence of any desired length. Figure 2 shows the nonlinear relationship between the voltage charge across the clock line capacitor and the amount of charge transferred per gate. There are several significant features to be noted in this figure. First, the assumed conditions yield a reasonable value of voltage change. Secondly, the relationship is nonlinear; thus for approximately linear analog operation, a restricted dynamic range is necessary. Thirdly, the use of a fat "0" will not interfere with digital operation; even a large fat "0" of 30% uses only about 10% of the total range involved.

A correlator that has the correlation function built into the metallization pattern can be made using the concept as developed to this point. To expand this, it is necessary to devise a suitable scheme for externally altering the correlation function. Figure 3 shows a method for externally controlling the correlation of a single bit. Control pulses are used to connect each storage gate to the appropriate buss line, depending upon whether a "1" or "0" correlation is desired in that bit location. Note that the "1" and "0" control signals are simply the inverse of each other; the "1" control is a bit sequence

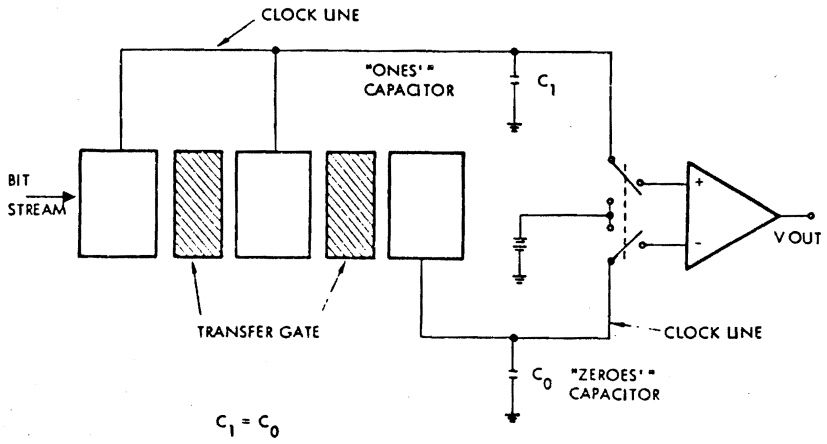

Figure 1. Correlator Matched to Sequence 110

Table 1. Voltage Output for a Given Received Sequence

Received Sequence	Number of Disagreements With Desired Sequence	Vout* (ΔV)
110	0	+2
111	1	+1
100	1	+1
010	1	+1
000	2	0
101	2	0
011	2	0
001	3	-1

*The units of this column are in terms of the voltage change produced by the charge that flows from the clock line to one gate when a full charge packet is transferred under that gate.

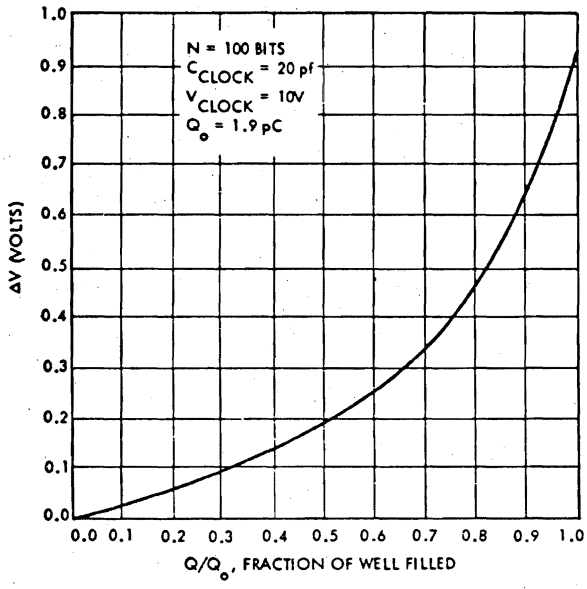

Figure 2. Voltage Change as a Function of Charge Transferred

representing all the locations where a "1" exits in the desired sequence and the "0" control is naturally the inverse of that sequence. Figure 4 indicates how the correlation of each bit in a register can be controlled by the bits in two auxiliary registers which contain the correlation function and its inverse. The bits in the auxiliary registers are nondestructively sensed and they in turn control the FET switches which connect the data bit stream gate to either the "1" buss or the "0" buss. In practice the two buss lines can be identical with the drains of the two FET's. A more detailed layout is given in Figure 5.

Figure 5 shows the complete layout for the correlation of two bits; previous figures had dealt with one bit only. Assuming 0.3 mil photolithography, the area required for the layout of Figure 5 is under 7.0 mil^2/bit.

SPREAD SPECTRUM CORRELATION DETECTOR EXAMPLE

In many data communication or pulsed radar systems, a pseudorandom sequence is used to code the binary data or the radar pulse. As an actual system application* consider a radar pulse coded with a 512-bit pseudo-random sequence which is used to biphase-modulate a 60 MHz IF carrier.

The general digital implementation of a correlation detector suited to this type of input signal is shown in Figure 6. The input analog signal at an IF frequency of 60 MHz is sampled at 2 samples per modulation bit time and separated into its I and Q components (in-phase and quadrature phase). The waveforms in both the I and Q channels are then converted to digital form by means of a 2 bit A/D converter, thus generating a 4 level coded signal. This signal is then correlated to a reference binary code of length 512 bits. The input code rate is 6 Mbps. Hence the pertinent parameters are:

I or Q correlation reference code length = 512 bits/code

Number of inputs = 2 (I and Q)

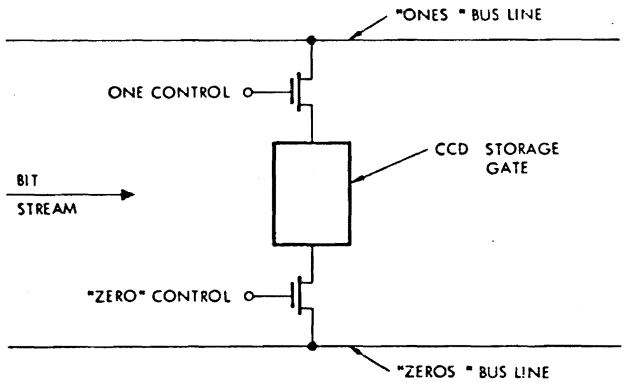

Figure 3. Programmable Control of Correlation of a Single Bit

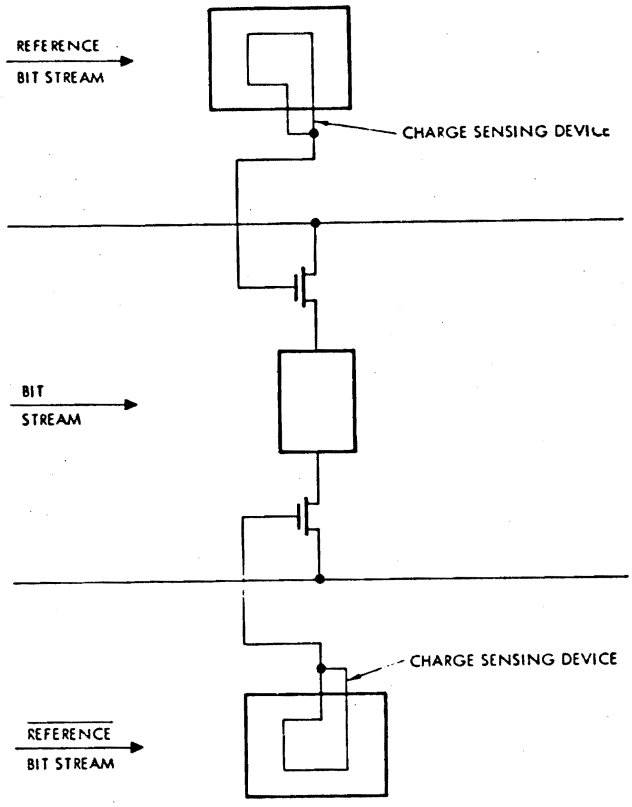

Figure 4. Programmable Correlation of a Single Bit the Use of Two Auxiliary Bit Locations

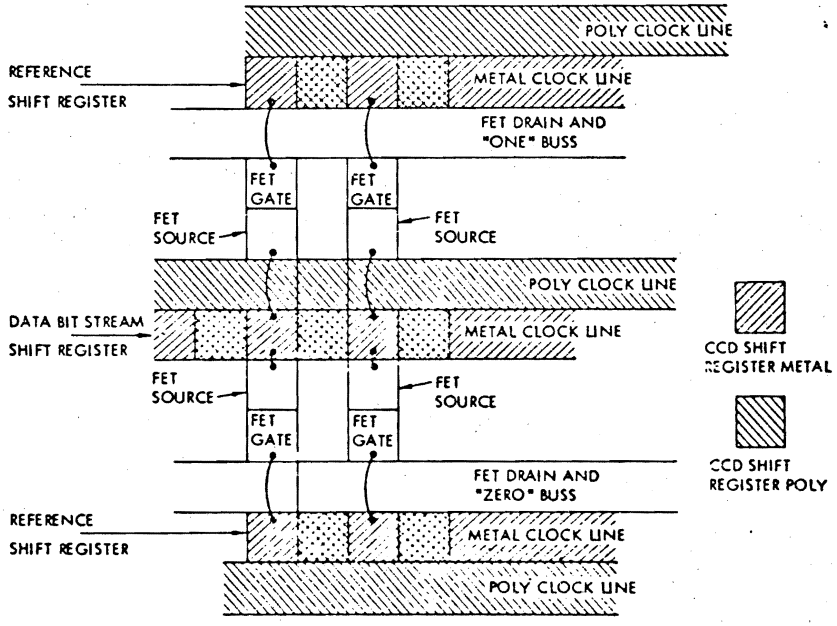

Figure 5. Plan View of Detailed Layout of Two Bits of Correlation

Number of levels/sample = 4

I or Q signal sample length =

512 bits/code x 2 samples/bit =

1024 samples/code

Therefore, a total of 2 x 4 = 8 correlator channels must be utilized at a bit rate of 12 Mbs. Each correlator channel consists of a 1024-bit parallel correlator at 12 Mbs; overall, 8192 bits are required.

The existing design of the correlation detector system (which has been reduced to practice) utilizes triple diffused emitter follower logic. Each 3D/EFL parallel correlator LSI chip performs 64 bits of correlation at a 12 MHz rate, and a total of 128 such chips are required for the complete function.

If this same system were implemented using CCD correlators, a primary concern would be the 12 MHz shifting frequency. Assuming that a shifting rate of 3-5 MHz is reasonable with today's technology, certain changes must be made in the overall system design. One obvious approach is to demultiplex the incoming data immediately after the A/D conversion process and then use several correlators in parallel at lower speeds. For instance, if 3 MHz is the basic shift rate then a 1:4 demultiplexer followed by 4 sets of correlators working in parallel could be used for each of the I and Q channels. Due to the presence of the 1:4 demultiplexer each of the 4 sets of correlators must itself contain 4 separate correlators; the reference code of each one is offset by one bit time to account for the arbitrary location of the first received bit. This means that the overall CCD implementation must have four times the shift register

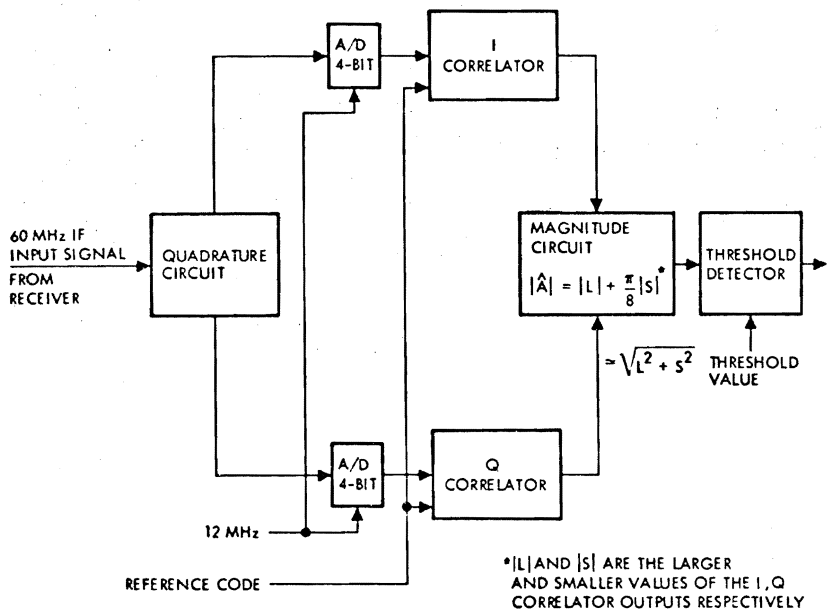

Figure 6. Digital Implementation of the Correlation Detector

*TRW Systems is presently under contract to develop a breadboard model of a "Multilevel Digital Correlation Detector" system using triple diffused emitter follower logic LSI, in the form of 64 bit correlators per chip. Contract N00014-73-C-0019. This correlation detector is applicable to a spread spectrum IFF communication system and provides 27 db of AJ processing gain.

capacity of the 3D/EFL approach. This penalty is balanced by the inherent high density and low power characteristics of the CCD design. Table 2 compares the CCD and 3D/EFL approaches. In preparing the table, a 7.5 micron photolithography has been assumed. The 4 watts of correlator power include clock driver losses, power supply losses, as well as the on chip dissipation, and the 1:4 demultiplexers.

Table 2. Comparison of Correlation Detector LSI Implementations

Parameter	Bipolar LSI	CCD LSI (Digital)
LSI technology	Triple diffused EFL	3 phase N type surface channel
Number of LSI correlator chips required	128	16
Total correlator power	200 watts	4 watts
Correlation bits/chip	64 bits/chip	2048 bits/chip
Total number of correlator bits	128 x 64 = 8192 bits	16 x 2048 = 32,768 bits
Individual correlator circuit clock rates	12 MHz	3 MHz
Size of correlator chip	200 x 200 $mils^2$	150 x 150 $mils^2$

1. D. D. Buss, D. R. Collins, W. H. Bailey, C. R. Reeves, "Transversal Filtering Using Charge-Transfer Devices," IEEE Journal of Solid-State Circuits, Vol. SC-8, No. 2, April 1973, p 138-146.

2. D. R. Collins, W. H. Bailey, W. M. Gosney, D. D. Buss, "Charge-Coupled-Device Analogue Matched Filters," Electronics Letters, Vol. 8, 29 June 1972, p 328-329.