Characterization of Surface Channel CCD Image Arrays at Low Light Levels*

Marvin H. White, Donald R. Lampe, Franklyn C. Blaha, Ingham A. Mack

Westinghouse Electric Corporation, Advanced Technology Laboratories, Baltimore, Maryland 21203

ABSTRACT

The characteristics of surface channel CCD line imagers with front-surface imaging, interline transfer, and 2-phase stepped oxide, aluminum and silicon-gate CCD registers, are presented in this paper. The analysis, design, and evaluation of 1 x 64 CCD line arrays are described in terms of their performance at low light levels. The signal-to-noise, S/N, is formulated in terms of charge at the collection diode. A dynamic range of 80 dB and a noise equivalent signal (NES), where S/N = 1, of 135 electrons is achieved with a picture element time of 20μsec and an integration time of 1.32 msec in the absence of a fat-zero. A unique CMOS readout circuit, which uses correlated double sampling within a picture element time window, removes the Nyquist noise of the reset switch, eliminates switching transients, and suppresses low-frequency noise to provide low-noise analog signal processing of the video signals. This paper describes the responsivity, resolution, spectral and noise measurements on silicon-gate CCD sensors and CCD interline shift-registers. The influence of transfer inefficiency and electrical fat-zero insertion on resolution and noise is described at low light levels.

*A condensation of a paper to appear in the Journal of Solid State Circuits.

I. CCD LINE ARRAYS AND SIGNAL PROCESSING

Figure 1 illustrates the line array functional block diagram. The interline transfer approach requires a transfer pulse, ϕ_T, at the start of a line time to transfer the stored photocharge from the individual sensor locations to a corresponding bit in the parallel-to-serial CCD shift register. In our case, a 2-phase clock system transfers the charge along the shift register to a CMOS readout circuit. The shift register is a 2-phase stepped-oxide geometry with a surface field and potential profile as shown in figure 2. Figure 3 is an enlargement of the CCD linear array after the definition of the shift-register with an aluminum interconnection. The sensors are constructed with transparent, conductive, polycrystalline silicon-gate electrodes with a N+ stopper diffusion (N-type, <100> substrates) on three sides. The sensors are defined by an aluminum light shield, which also serves to cover the CCD shift-register and CMOS readout circuits. The CCD line array is constructed of 128 CCD sensors with a 2P offset in the along track direction (P=15 μm, Δx = 22 μm, Δy = 18 μm). The dimension Δx is in the across track direction and Δy is in the along-track mechanical-scan direction.

Figure 4 illustrates the CMOS readout circuit, which consists of a multiplex gate (i.e., muxgate ϕ_M), a reverse-biased collection diode, n-channel MOS reset switch (i.e., reset gate ϕ_R), and p-channel MOS electrometer amplifier. The voltage waveform on the gate of the electrometer is also displayed in figure 4. The four timing intervals comprise a pixel (i.e., picture element) time and form the basis of a signal processing method called correlated double sampling[1, 2]. The node capacitance at the collecting diode is a 0.25 pF and is not influenced by the parasitic N^+/P^- diode of the reset switch, which is reverse-biased to

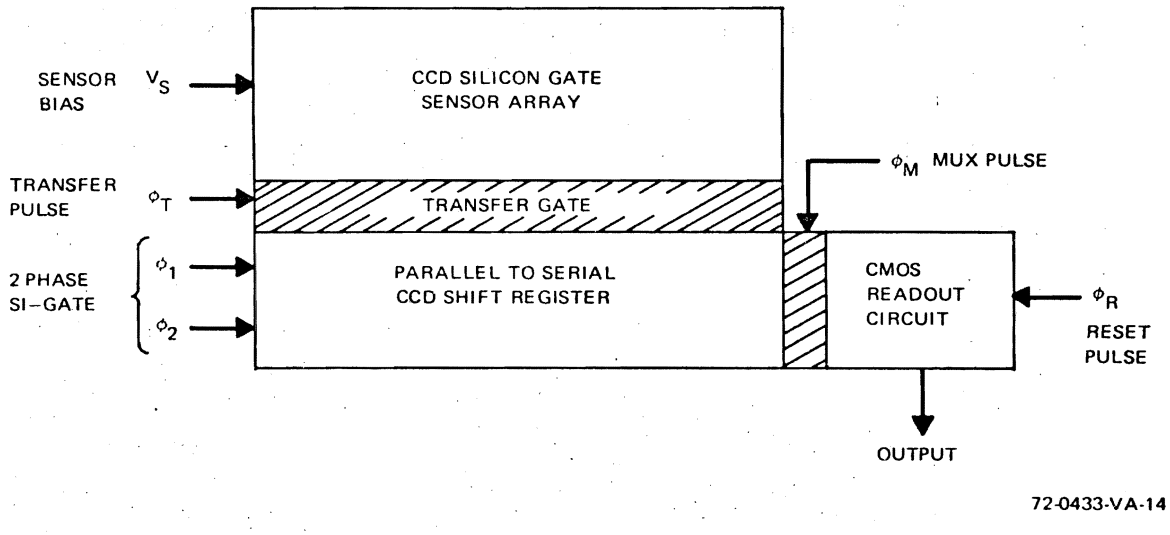

Figure 1. CCD Line Array Functional Block Diagram Illustrating Interline Transfers

prevent discharge of the collecting node by the reset feedthrough "pedestal" when the reset switch is turned off. The aluminum light shield provides about 0.03 pF of the node capacitance since it rests over 1.3 to 1.5 μm of deposited SiO_2 and forms a ground plane to shield the sensitive output collection circuit from pick-up. In the use of a CCD sensor array, the natural output is charge integration, and sampling techniques are advantageous to provide on-chip signal processing and reconstruction. With the advent of CCD imagers, the integrity of the signal charge is maintained until signal detection occurs at a common collection diode. The importance of this point cannot be emphasized too strongly, since the problem of signal and clock interaction is localized at a common readout circuit. All of the pixel information passes through a common collection diode, integrating capacitance, and electrometer amplifier. For a noise current i_n at the input to the preamplifier in figure 4, the equivalent noise charge at the collection diode is $C\, i_n/g_m$. Thus, the small C/g_m of the electrometer increases the signal-to-noise charge ratio at the collection diode for such noise currents as shot noise, preamplifier noise, surface-state noise and supply noise.

The video output voltage is the time difference between the previously clamped reset level and the same reset level plus signal increment introduced by the closure

Two-Phase Stepped Oxide Silicon Gate/CCD Shift Register

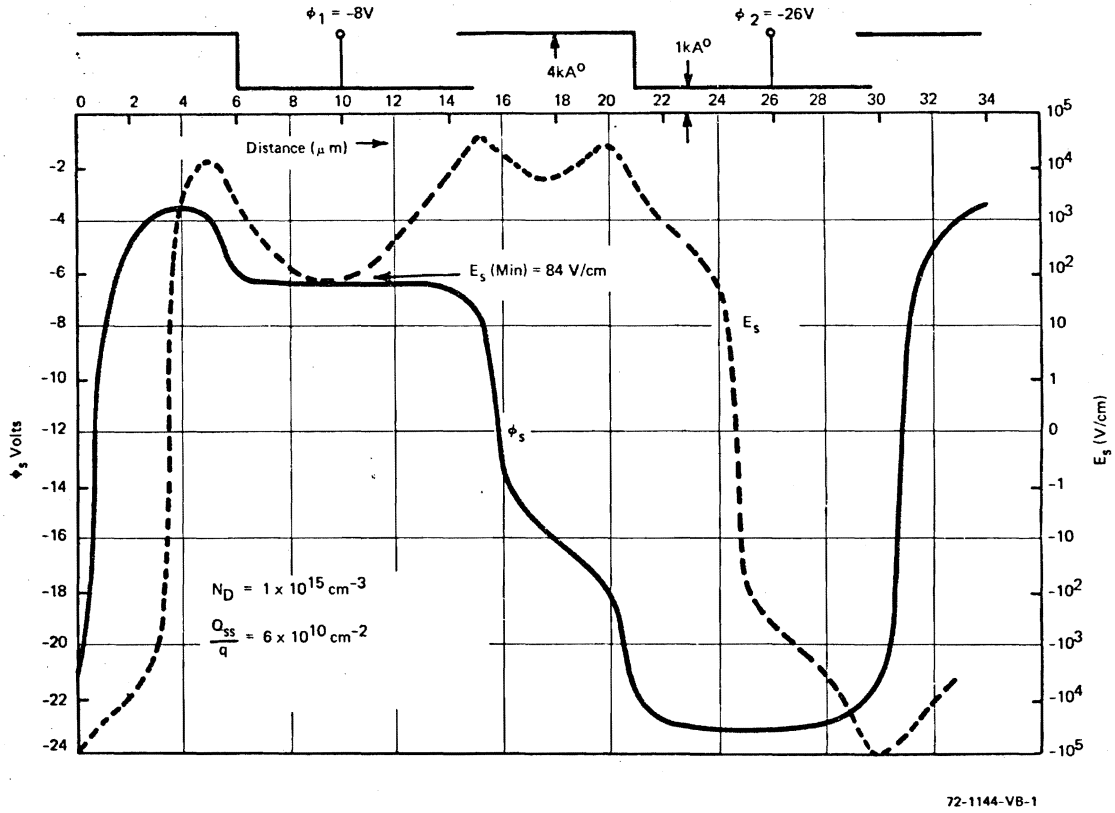

Figure 2. A Two-Phase Stepped Oxide CCD Unit Cell with Curves of Periodic Surface Potential and Longitudinal Electric Field Relative to Electrode Cross-Section at Top of Figure

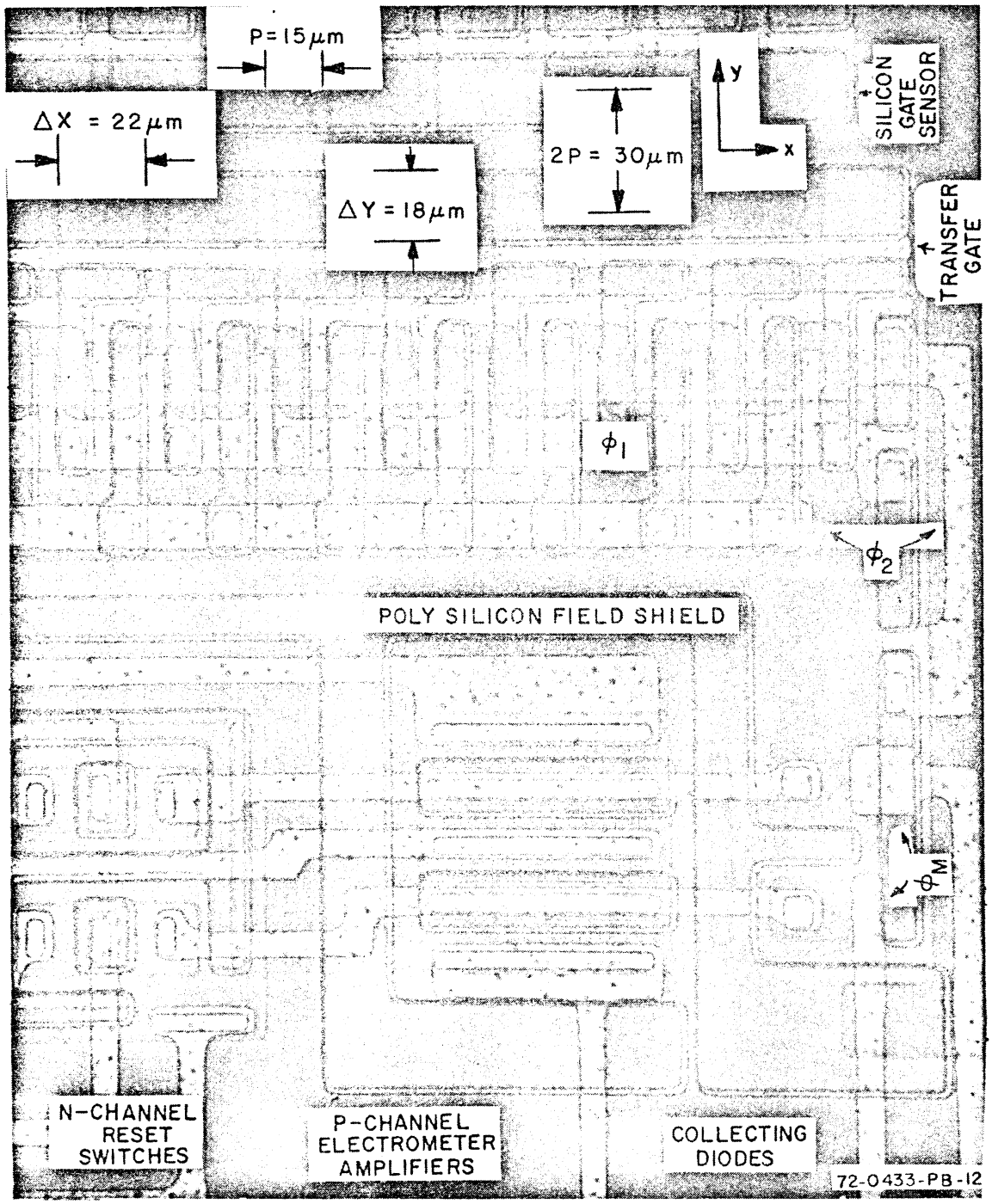

Figure 3. CCD "Interline-Transfer" Line-Array with CMOS Readout Circuit (prior to Aluminum Light Shield)

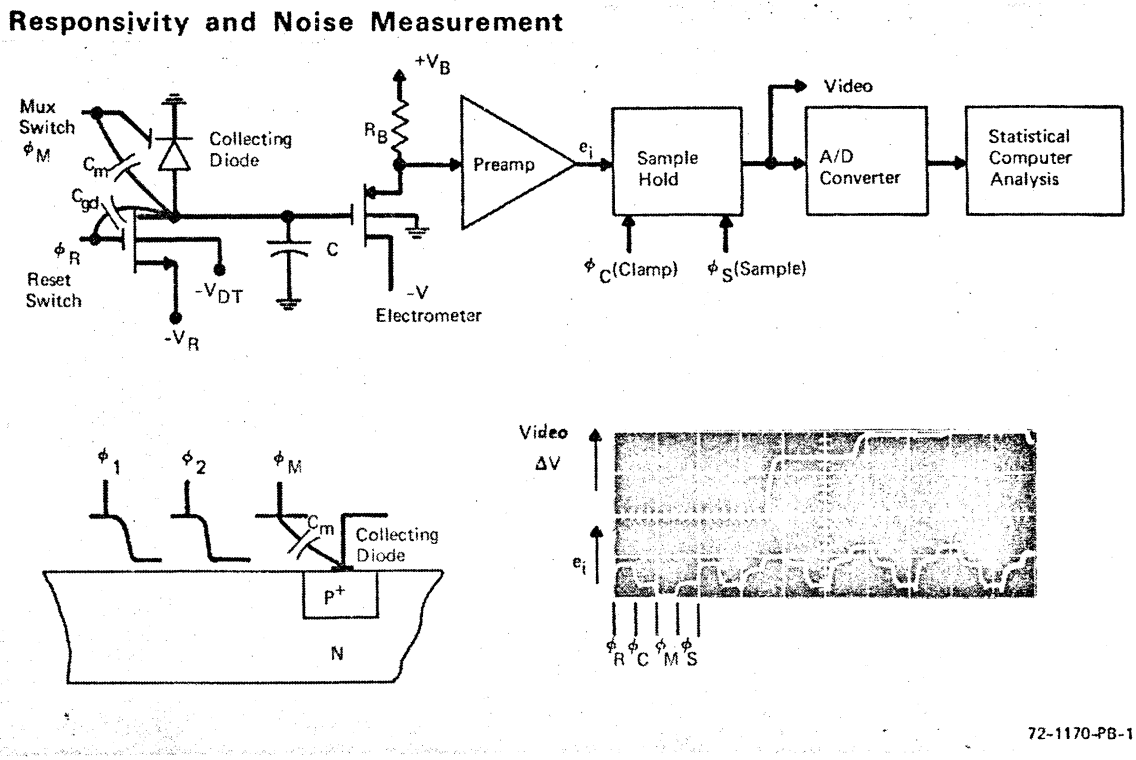

Figure 4. Test Apparatus for Measurement of Responsivity and Noise with Typical Output Waveforms, from the Correlated Double Sampling (CDS) Analog Signal Processor

of the MUX switch ϕ_M (i.e., there is negligible leakage of the reset level between read reset (clamp) and read signal (sample) intervals. Thus, the reset noise, which includes Nyquist noise and V_R power supply noise, is correlated within a pixel time window. The signal increment, which consists of sensor and shift-register leakage current added to photocharge, is amplified and passed to the output of the signal porcessor by the closure of the sample switch. The output video stream is a sequence of pixel element responses free from reset noise and proportional to the minority carrier signal increment introduced by closure of the MUX switch. The correlated double sampling (CDS) method removes switching transients and provides dark level subtraction similar to an earlier technique[3], which used a gated charge integrator in lieu of storing (clamping) the actual diode reset level, for subsequent subtraction from the reset level plus signal increment to give the signal increment without reset-noise. The Nyquist noise of the reset switch has been removed, since it is correlated within a pixel time, and this means a removal of a noise charge [4,5]

$$Q_n = \frac{(kTC)^{1/2}}{q} = 200\ e^- \qquad (1)$$

for a 0.25 pF capacitor.

II. RESPONSIVITY AND NOISE CONSIDERATIONS

ANALYTICAL FORMULATION

We can begin by an examination of what we mean by responsivity. We will define this quantity to be R in pA/mW/m^2 or current output per input irradiance,* which makes the responsivity a function of sensor area. Suppose we attempt to

formulate the responsivity by reference to an ideal blackbody source of temperature T_S [e.g., $T_S = 6000^{\circ}$ K]. Thus, we can write

$$R = \frac{\int_{\lambda_1}^{\lambda_2} R_\lambda H_s(\lambda)\, d\lambda}{\int_{\lambda_1}^{\lambda_2} H_s(\lambda)\, d\lambda} = \text{Individual Sensor Responsivity} \qquad (2)$$

and

$$R_\lambda = \text{spectral responsivity} = \frac{q\eta(\lambda)A}{hc/\lambda} \qquad (3)$$

where H_s is the specified source irradiance, λ_2 and λ_1 the reference spectral band [e.g., $\lambda_1 = 400$ nm, $\lambda_2 = 800$ nm], A the area of the sensor and $\eta(\lambda)$ the effective quantum efficiency. Integration of equation (3) for the specified temperature source and wavelength interval yields,

$$R = 0.186\eta \left[\frac{A}{18\,\mu m \times 22\,\mu m}\right] \frac{pA}{mW/m^2} \qquad (4)$$

where η has been assumed to be constant over the wavelength interval. The experimental responsivity may be referenced to the gate capacitance C of the electrometer in figure 4, and expressed as

$$R(1-\epsilon)^{2N} = \frac{C\Delta V}{g_m R_f G \Delta E} = \frac{\Delta Q}{\Delta E} = \text{Responsivity Measured at Collection Diode} \qquad (5)$$

where C is the node capacitance at the gate of the electrometer, g_m the electrometer transconductance, R_F the preamplifier feedback resistance, G the gain of the signal processor following the preamplifier, and ΔV the change in video output voltage for a change in input exposure density ΔE. The responsivity of each sensor is degraded by a factor $(1-\epsilon)^{2N}$, where 2N is the number of transfers the signal undergoes before it reaches the collection diode. In practice, the integral in the numerator of equation (2), which represents current output, is obtained with a test source whose spectral irradiance profile is known. The irradiance supplied by the test source, while effective over the entire spectral response of the sensor (i.e., 200 nm to 1200 nm for silicon), is converted to an effective irradiance from a 6000°K blackbody source in the 400 nm to 800 nm window.

The measurement procedure involves the use of a 10 bit A/D converter, which provides an accuracy of 1024 bits. In practice, the signal output from each sensor element in the array is sampled 1024 times at each irradiance level and recorded in terms of A/D bits. The mean and variance corresponds to the uncertainty or noise as determined over 1024 samples. With these quantities we can determine linearity, streaking, responsivity, noise, etc. The measurement circuit is illustrated in figure 4, which shows the timing sequence at the preamplifier output and video output signal. The noise is converted from rms A/D bits to an equivalent input exposure density, (microjoules/m^2) called the noise equivalent signal (NES), by multiplying the rms A/D bits by the reciprocal slope of the transfer curve at the particular irradiance level (exposure density). The transfer curve is essentially a plot of signal A/D bits versus input exposure density. The reciprocal slope of the transfer curve is called the quantizing interval and is given as,

$$Q_I = \frac{\Delta E}{\Delta(A/D\,bits)}\left(\frac{\mu J}{m^2 \cdot bit}\right) \qquad (6)$$

Thus, if we have B_{RMS} bits variance at a specified irradiance level, then the NES becomes

$$NES = Q_I B_{RMS}(\mu J/m^2) \qquad (7)$$

The NES, which is measured by the above procedure, consists of 4 principal terms:

a. System noise from analog signal processor, power supplies, pulse jitter, mechanical vibrations, etc.

b. Chip noise from the CCD sensor array. This noise is determined by geometrical design and fabrication processes

*R may easily be converted to electrons/microjoule/m^2.

for the chip

c. Radiation shot noise from the fluctuation in arriving signal photons and which represents a background limited performance

d. Quantization noise from the uncertainty associated with the finite size of the quantizing interval Q_I.

The measured or total NES is given as

$$NES_T^2(\text{total}) = NES_{syst}^2 + NES_{chip}^2 + \frac{qE}{R} + \frac{Q_I^2}{12} \quad (8)$$

where the radiation shot noise term involves the exposure density and the quantization noise assumes an error which varies linearly with time.[6]

We can formulate analytically the chip NES at the collection diode in figure 4. There are 3 sources of noise on the CCD chip:

a. Nyquist noise at the reset switch and output capacitance $Q_n^2 = kTC$

b. Thermal shot noise associated with the sensor and shift register $Q_n^2 = q\left[I_{LR} + I_{LS}(1-\epsilon)^{2N}\right]\tau$, where τ = line read-out time = integration or exposure time

c. Surface state noise associated with the transfer of charge to and from $Si\text{-}SiO_2$ interface states within the sensor, shift-register and electrometer amplifier

$$Q_n^2 = kTC_{st}$$

where C_{st} is an effective surface state capacitance, determined by the number of transfers, the clock frequency, the effective bandwidth of the signal processor, etc. We have mentioned that the correlated double sampling removes the Nyquist noise of the reset switch, however; we will include this term in the formulation of signal-to-noise, written as

$$\frac{S}{N} = \frac{\text{Signal Charge}}{\text{Noise Charge}} = \frac{R(1-\epsilon)^{2N}E}{\left(kT(c+C_{st}) + q[I_{LR}+I_{LS}(1-\epsilon)^{2N}]\tau\right)^{1/2}} \quad (9)$$

If we set the S/N = 1 in the equation (5-7), then the chip NES becomes,

$$NES_{chip} = \frac{\left(kT(C + C_{st}) + q[I_{LR} + I_{LS}(1-\epsilon)^{2N}]\tau\right)^{1/2}}{R(1-\epsilon)^{2N}} \quad (10)$$

MEASUREMENTS

Table 1 lists the experimental measurements of parameters associated with a 1 x 64 element CCD line array. The experimental responsivity calculated from these parameters [see equation (5)] is

$$R(\text{exp}) = \frac{0.065\ pA}{mW/m^2}\left(\frac{406e^-}{\mu J/m^2}\right) \quad (11)$$

and substitution of equation (11) into equation (4) yields

$$\eta(\text{effective}) = 0.35 \quad (12)$$

for the CCD sensor. The effective quantum efficiency calculated for this CCD sensor must be taken with caution since the relative spectral response profile displays interference fringes due to the 2kÅ polysilicon electrode over a 1kÅ gate oxidation. The relative spectral responses of the CCD sensor compared with a diffused P + / P⁻/N(x_j = 12μm) photodiode are shown in figure 5. The photodiode response illustrates a constant quantum efficiency η = 0.65 between 400 nm and 800 nm, and the responsivity for an equivalent area size is $0.124\frac{pA}{mW/m^2}$. Thus, it is clear that a photodiode sensor would have a definite advantage over its CCD sensor counterpart. Both sensors are overcoated with approximately 3μm of SiO_2.

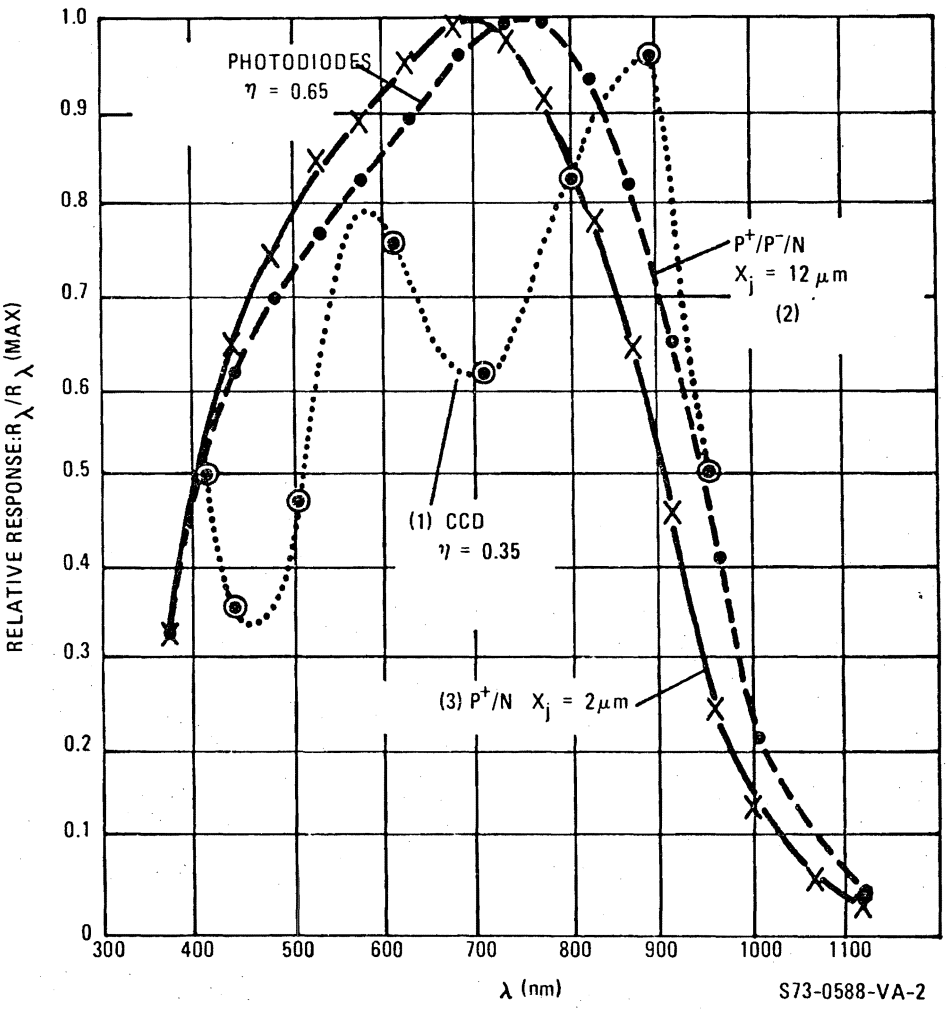

Figure 5. The Relative Spectral Responses of (1) a CCD Sensor with a 0.2 m Silicon Gate over a 0.1 m SiO_2 and of two Diffused Photodiodes: (2) a Pt/P-IN Diode 12 m Deep and (3) a Pt/N Diode 2 m Deep

TABLE 1

EXPERIMENTAL PARAMETERS OF CCD READOUT CIRCUIT AND ANALOG SIGNAL PROCESSOR

g_m = 250 μmho	G = 2.57
R_F = 75K ohm	E = 290 $\mu J/m^2$
A = 18μm x 22μm	τ = 1.32 msec
2N+3 = 5 to 133	V_R = -12V
ΔV = 3.56v	
C = 0.25 pF	
$\epsilon = 10^{-4}$	

The dynamic range of a CCD sensor line array (1x64 element) is shown in figure 6. This particular CCD array had a high quantizing interval $Q_I = 0.80\mu J/m^2 \cdot$ bit. Figure 6 illustrates the variance or noise measured for the correlated and uncorrelated noise, we reversed the clamp and sample sequence so that they were not performed in the same pixel time window. This is proof of the correlated double sampling technique in action. Measurements had been taken on another CCD line array with a lower leakage current (1.5 pA/well), and the total NES measured was $0.40\mu J/m^2$ ($160e^-$) for a quantizing interval of $0.03\mu J/m^2 \cdot$ bit. This total NES is less than the Nyquist noise contribution, which is

$$NES(Nyquist) = \frac{(2kTC)^{1/2}}{R} = \frac{0.70\ \mu J}{m^2}(284e^-) \quad (13)$$

where the factor of 2 is used to illustrate the uncorrelated case of 2 independent readings of clamp and sample. The NES values shown in figure 6 are for the basic sensor chip. The system NES = $0.15\frac{\mu J}{m^2}$ which is referred to the input of the electrometer amplifier. As figure 6 illustrates, the dynamic range is about 75 dB for this particular CCD array, with a chip NES=$260e^-$; measurements on lower leakage devices indicate a chip NES = $135e^-$ and a dynamic range of 80 dB. All of the measurements were performed under uniform irradiance (line time τ= 1.32 msec) with the limitation as the "shot" noise associated with the leakage current on the chip. For example,

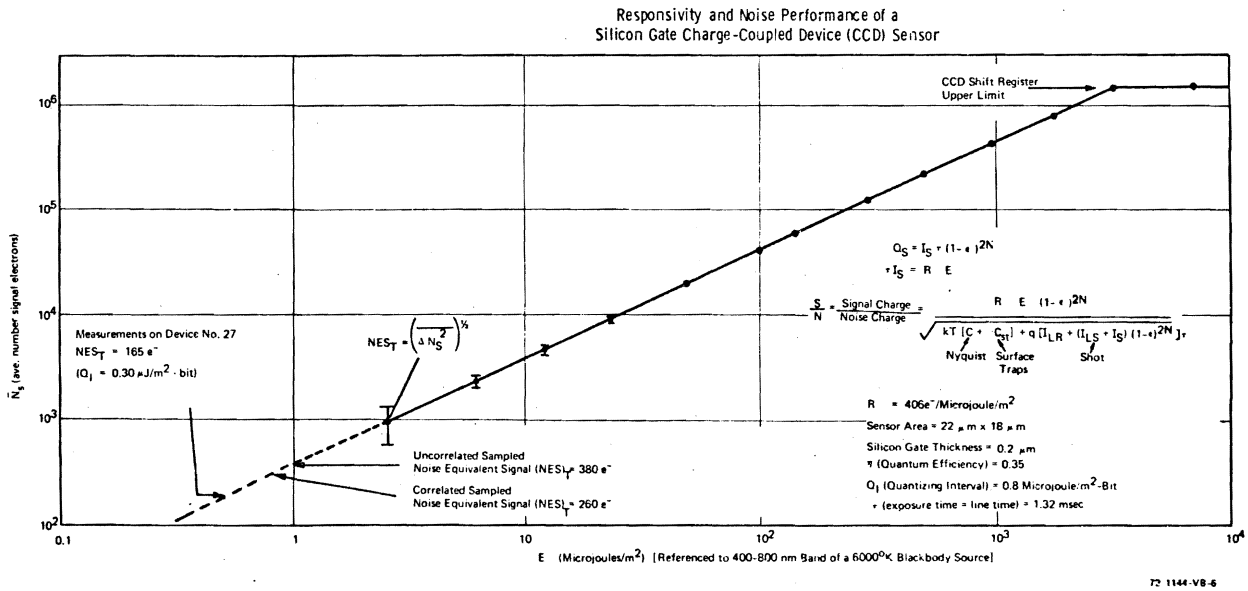

Figure 6. The Dynamic Range and Noise in a CCD Sensor Array (1 x 64 Elements) with Uniform Irradiance

the device measured in figure 6 had a leakage current I_{LR} = 7.0 pA in the register (the sensor leakage current I_{LS} was negligible compared with the register leakage current because of the low sensor bias voltage V_S = -8v.) and the shot noise NES contribution.

$$NES(shot) = \frac{(qI_{LR}\tau)^{1/2}}{R} = \quad (14)$$

$$0.591 \frac{\mu J}{m^2}(240e^-)$$

which accounts for most of the noise. In the low leakage devices the measured chip NES = $0.33\frac{\mu J}{m^2}(135e^-)$ can be attributed to the leakage current of 1.5 pA/well or a NES = $0.275\frac{\mu J}{m^2}(112e^-)$. The remaining noise is attributed to the surface-state noise[7] -- in the low leakage device this is a NES = $0.18\frac{\mu J}{m^2}(74e^-)$. Table 2 summarizes the noise performance and noise sources which influence the performance of the CCD array.

If we inject an electrical fat-zero (20 percent full CCD well) into the shift-register, the output is uniform because of improved transfer efficiency. An electri-fat-zero injected over the entire pixel time window produced a high, non-uniform noise at the output. The output noise for a 10 percent full CCD well under these conditions was approximately $4.0\frac{\mu J}{m^2}(1600e^-)$ and consisted of irregular "burst" noise. When the time window for electrical injections was narrowed to about 1 percent of the pixel window, the output noise for a 20 percent full CCD well was reduced to approximately $3.0\frac{\mu J}{m^2}(1200e^-)$ with no evidence of irregular noise. The method of electrical fat-zero injection requires further investigation before production of a truly low noise injection process.

TABLE 2
SUMMARY OF NOISE PERFORMANCE OF CCD IMAGING ARRAY
τ = 1.32 msec (NO ELECTRICAL FAT ZERO)

R = 406 e-/μJ/m^2	
Total NES (measured) at $166\frac{\mu J}{m^2}$ =	$0.74\frac{\mu J}{m^2}$
Calculated radiation shot noise $(\frac{qE}{R})^{1/2}$ =	$0.64\frac{\mu J}{m^2}$
Signal Processor Noise (measured system noise) =	$0.15\frac{\mu J}{m^2}$
Quantizing Noise $\frac{Q_I^2}{12})^{1/2}$ =	$0.087\frac{\mu J}{m^2}$
NES (chip) = $((0.74)^2 - (0.64)^2 - (0.15)^2 - (0.087)^2)^{1/2}$ = 0.33	$0.33\frac{\mu J}{m^2}$
= $(kTC_{st} + qI_{LR})^{1/2}$ (theoretical)	$0.34\frac{\mu J}{m^2}$
NES (shot) = $\frac{(qI_{LR}\tau)^{1/2}}{R}$ =	$0.275\frac{\mu J}{m^2}$
NES (surface) = $\frac{(kTC_{st})^{1/2}}{R}$ =	$0.20\frac{\mu J}{m^2}$

*A method for low-noise, electrical injection of a fat-zero (8) can give a NES less than the simple shot noise associated with the fat-zero.

III. LOW LIGHT LEVEL IMAGING

In order to evaluate the CCD line arrays, we employed a rotating drum to provide the along-track image motion while the line array was scanned electronically in the across-track direction. A transparency was mounted on the drum and irradiated by a calibrated source, with all irradiance levels referenced to a blackbody source at 6000°K in the 400 nm to 800 nm band. Figure 7 illustrates the low light level performance of the CCD 1 x 64 element line array with 3 msec exposure time (0.75 msec line readout time) and a highlight irradiance of 18.7 mW/m^2, which is about 120 pA of signal current. Our minimum detectable signal with a 20 percent fat-zero is 0.97 mW/m^2 or about 6 pA. The minimum detectable signal, if we could introduce the fat-zero with negligible noise,* is 0.08 mW/m^2 or about 0.4 pA. Notice the loss in resolution if we remove the electrical fat-zero. In the scene of the White House, the elements furthest from the collecting diode are at the top of the picture. It is apparent that the long number of empty CCD wells (as denoted by the black "tree" area), affects the resolution severely, since these wells do not have a background "radiation fat-zero" to provide low transfer inefficiencies.

Since a CCD imager uses an analog shift register, we must have low leakage register elements in addition to the requirements of low leakage sensor elements. With the interline transfer method we can separate the causes of leakage in an imager by simply turning on and off the transfer gate. In general, we encounter more leakage in the shift-register than the sensor elements. One advantage of the interline transfer approach is that the shift-register can be operated "free-running" to distribute the leakage throughout the register. If the register is "blanked" or held stationary for a period of time, then the local dark-current spots will begin to saturate the analog signal processor.

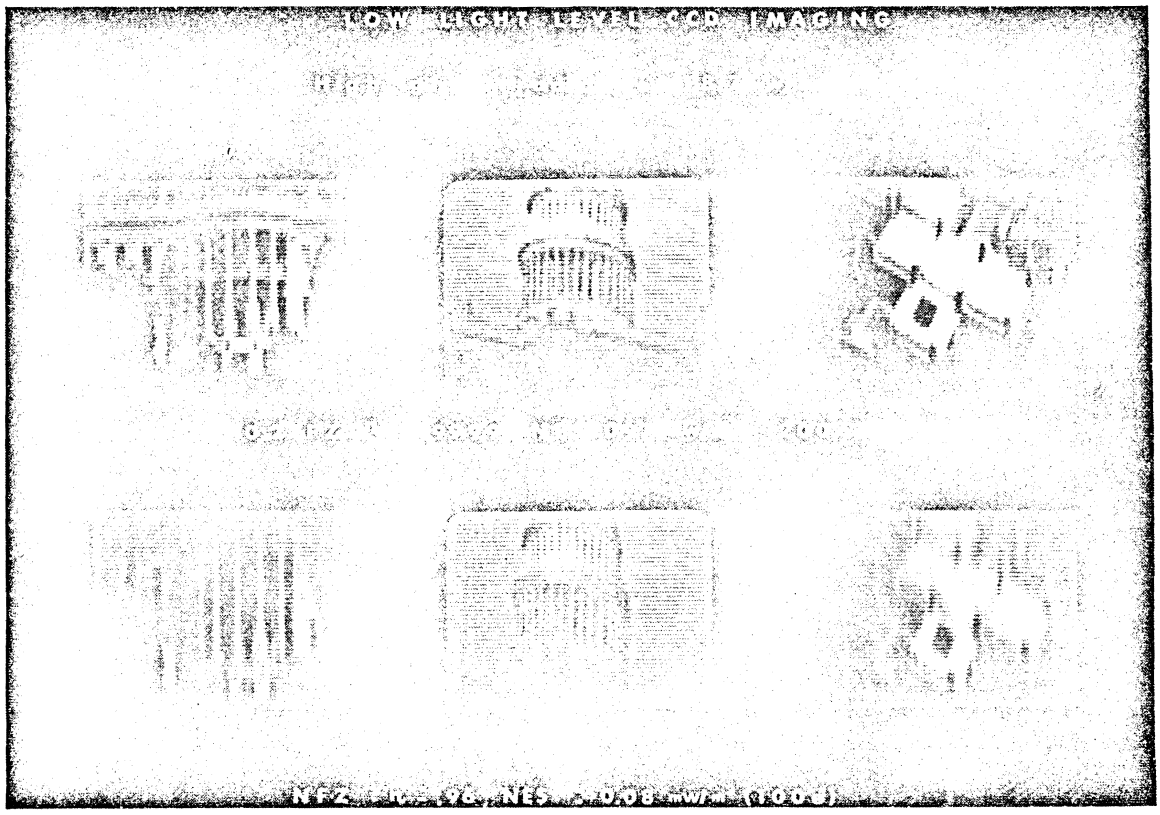

Figure 7. Low-Light Level Imaging With and Without an Electrical Fat Zero

IV. CONCLUSIONS

We have developed a method of signal processing called correlated double sampling, which removes the switching transients at the output collection diode, eliminates the Nyquist noise of the reset switch-output capacitance combination, provides dc restoration, increases dynamic range and suppresses surface state and 1/f noise contributions. The analog signal processor, which uses this technique, has been operated with clock frequencies from 800 Hz to over 3 mHz. We have measured the intrinsic noise-equivalent-signal (NES) or minimum detectable input exposure density of the CCD imager with this technique. The primary limitation to the NES is the shot noise associated with thermal leakage current generated in the sensor and shift-register. The surface channel CCD imager requires a 20 percent fat-zero for transfer inefficiency $\epsilon \leq 10^{-4}$ to obtain geometrical resolution. The excess noise associated with the electrical fat-zero limits the sensitivity of the surface channel CCD, and attention must be directed toward a method of low noise electrical injection. For an electrical fat-zero introduced by a gated diode, our measurements indicate a noise charge of 1000 to 1200 electrons; however, a redesign of the input electrical injection circuit[8] should enable surface channel CCD's to operate with an NES limited by thermal leakage shot noise and a dynamic range in excess of 80 dB. For our simple gated diode injection circuit with a 20 percent fat-zero, we have achieved greater than 60 dB dynamic range with less than $\pm$ 2 percent deviation from linearity over this range and less than $\pm$ 3 percent variation in responsivity and NES across a 1x64 element line array. The dark current variation was less than $\pm$ 3 percent across the array. We have made measurements without an electrical fat-zero and under uniform exposure, to indicate a noise charge of 135 electrons at an integration time of 1.32 msec. This noise was associated primarily with the thermal leakage current in the CCD shift-register. The thermal leakage current on the better arrays was about 50nA/cm^2.

Spectral response and responsivity measurements indicate a non-uniform spectral response, due to interference fringes caused by the silicon gate thickness and the underlying SiO_2. The effective quantum efficiency of the silicon gate CCD sensor in the range from 400 nm to 800 nm was $\eta = 0.35$, compared with a photodiode $\eta = 0.65$, which is constant. Consideration should be given to the design of the CCD imaging array with the use of a diffused photodiode for the sensor. The g_m/C ratio should be increased at the output collection diode to overcome system noise limitations, and the quantizing interval, Q_I, if digital signal processing is used, should be decreased in accordance with dynamic range and data rate limitations.

REFERENCES

1. M.H. White, D.R. Lampe, F.C. Blaha, I.A. Mack, "Charge Coupled Device (CCD) Imaging at Low Light Levels", IEEE Int'l Electron Device Meeting, Washington, D.C. (1972).

2. M.H. White, D.R. Lampe, I.A. Mack, F.C. Blaha, "Characterization of Charge Coupled Device Line and Area-Array Imaging at Low Light Levels" IEEE Int'l Solid State Circuits Conference, Philadelphia, Pa. (1973).

3. J.D. Plummer, J.D. Meindl, "MOS Electronics for a Portable Reading Aid for the Blind," IEEE Journal of Solid-State Circuits, SC-7, No. 2, pp. 111-20, April 1972.

4. J.E. Carnes and W.F. Kosonocky, "Noise Sources in Charge-Coupled Devices". RCA Review 33, 327 (1972).

5. D.F. Barbe, "Noise and Distortion Considerations in Charge-Coupled Devices", Electronics Letters, 8, 207 (1972).

6. J.A. Betts, Signal Processing, Modulation and Noise, American Elsevier Publ. Co., New York (1971).

7. K.K. Thornber and M.F. Tompsett, "Spectral Density of Noise Generated in Charge Transfer Devices", IEEE Trans. on Electon Devices ED-20 No. 4, p. 456, April 1973.

8. S.P. Emmons, D.D. Buss, "Techniques for Introducing a Low Noise Fat-Zero in CCD's," Device Research Conference (Boulder, Colorado), June 1973.

REVERSE SIDE BLANK