A Global Shutter, Backside Illumination CMOS Image Sensor for Satellite Navigation

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Abstract – A 1 mega pixel global shutter backside illumination CMOS image sensor has been developed for use in Medium Accuracy Star Tracking applications. The chip is fabricated in a commercial 0.18 μm CMOS process, and includes a 16-bit on-chip ADC, allowing either rolling or global shutter operation, and is radiation tolerant. This paper describes the basic architecture, processing, and assembly of the star tracker sensor and presents data on image sensor performance and radiation tolerance. We discuss how the design of the epitaxial Si layer and backside process impact important imaging features. This is the first report on radiation tolerance of a global shutter, backside illumination image sensor.

I. INTRODUCTION

Star trackers are the most accurate sensors for 3-axis satellite attitude estimation. Current star trackers typically use CMOS image sensors, because these sensors have low power, low cost, and can be integrated with additional functions such as digital signal processing [1]. Historically, CMOS image sensors for star trackers have used frontside illumination and rolling shutter operation. However backside illumination provides higher sensitivity compared to frontside illumination, and therefore is beneficial for detecting the weak signal from stars. In addition, global shutter operation can be used to eliminate rolling shutter distortion (i.e. “motion blur”). In this report we present results of a global shutter, backside illumination (BSI) image sensor with high radiation tolerance, used for star tracking applications.

The prototype image sensor is a backside illuminated (BSI) monolithic CMOS focal plane array with a resolution of 1024 x 1024 pixels (Fig. 1)[2]. The imager uses active pixel sensor (APS) technology and can operate in either global (snapshot) or rolling shutter modes. The focal plane array runs at 10 frames per second (fps) at full resolution. The image sensor signals are read out through column amplifiers which are followed by a 16-bit on-chip, pipelined analog-to-digital converter (ADC). An alternate path to bring the raw analog video out of the sensor is also included. In global shutter mode, true correlated double sampling is possible in the sensor. The digital data is transferred off-chip via a standard parallel CMOS interface.

II. EXPERIMENT

A. Wafer Fabrication and Assembly

The image sensor wafers were fabricated on 200mm Silicon-On-Insulator (SOI) substrates, using a 0.18 μm CMOS process. A number of modifications were made to the standard CMOS logic process, including optimized epitaxial Si thickness (for red and infrared sensitivity), optimized B doping profile in the epitaxial Si layer (for blue light sensitivity) [10], and additional implants for the pixel devices. The backside processing (Fig. 2) consists of wafer bonding, backside thinning and removal of the buried oxide.
(BOX) layer on the device wafer, through silicon via (TSV) etch, dielectric deposition, insulator etch, and metallization[11,12].

![Image 2](image2.png)

**Figure 2. Schematic cross-section of BSI image sensor**

The product chip is mounted in a ceramic Pin Grid Array (PGA) package with a hole and slot configuration for ease of mounting, with active image array centered in the package. Aluminum wedge wirebonding (1.25mil Al wire) is utilized for demonstrated reliability. The Al wire is wedge bonded to an Al pad inside the TSVs (Fig. 2). For this experiment, a clear coverglass (Schott D263 T eco) is applied and taped in place to maintain integrity and cleanliness (Fig 3). There is a future option for an integrated thermoelectric cooler (TEC) with temperature sensor, and ultimately a hermetic sealed coverglass lid option.

![Image 3](image3.png)

**Figure 3. Schematic of package for BSI image sensor.**

### B. Radiation Tolerant Devices

The sensor is designed to be radiation tolerant and able to withstand a Total Ionizing Dose (TID) of 50 Krad (Cobalt 60) without experiencing a significant shift in device parameters.

![Image 4](image4.png)

**Figure 4: Examples of radiation tolerant field effect transistors (FETs); (a) annular gate FET, (b) ringed source FET, and (c) conventional (non-radiation tolerant) FET.**

The pixels are designed to meet the dark current specification after heavy ion testing with 63 MeV protons after a total fluence of $2.6 \times 10^{11}$ protons/cm$^2$. The design includes specialized analog and digital layout techniques for improved radiation tolerance. Annular gate field effect transistors (FETs) (Fig. 4)[8,9] are used to prevent TID damage, and guard rings and substrate/well connections are used to avoid any Single Event Latch-up to a linear energy transfer (LET) threshold of 100 MeV-cm$^2$/mg.

### C. Characterization

A basic question at the start of the program was to determine the effect of backside processing on devices and image sensor arrays. Hence, a number of tests were run before and after backside processing, including standard scribble tests (FETs, resistors, etc.) and image sensor arrays. In addition, the 3.3V nFETs and the 1.8V pFETs were tested for hot carrier lifetime (nFETs)[13] and negative bias temperature instability (NBTI) (pFETs) [14] before and after backside processing. Hot carrier stresses and radiation stresses were also performed on 3.3V annular gate nFETs, to determine how the annular gate affects reliability.

Image sensor arrays and product chips were tested for standard tests, such as photon transfer curve (PTC), dark current, lag, linearity, fixed pattern noise (both dark response non-uniformity or DRNU and photo response non-uniformity or PRNU), global shutter efficiency, defective pixels, and quantum efficiency (QE) [15,16].

Radiation effects in silicon devices can be from ionizing damage or non-ionizing damage [3,5]. Ionizing radiation (X-rays or gamma rays) creates electron-hole pairs in either Si or SiO$_2$. In SiO$_2$, the ionizing radiation can cause permanent degradation in the form of trapped charge. Electrons have relatively high mobility in SiO$_2$ and diffuse away. In contrast, holes diffuse slowly and result in positive charge in the bulk oxide or at the Si-SiO$_2$ interface. The positive charge can cause the threshold voltage to shift in either the gate dielectric or in the isolation.

Non-ionizing radiation damage can be due energetic particles such as protons or neutrons. These particles can displace atoms in the substrate, resulting in a vacancy and an interstitial. These defects can act as generation-recombination centers in Si, and as trapped charge in SiO$_2$.

The radiation tolerance was tested by exposing image sensors to 63 MeV protons at a fluence of $2.6 \times 10^{11}$ protons/cm$^2$. [3]. By using protons, both ionizing and non-ionizing radiation damage can be measured. The image sensors were then characterized for noise (PRNU and thermal noise), photon transfer curves, and dark current.

### III. Results and Discussion

#### A. Pre-Radiation Results

Key parameters were characterized for both frontside and backside illumination image sensors. Frontside illumination images sensors tested at wafer level exhibit good linearity and low noise (Fig. 5). The dark current measured at wafer level is similar for frontside and backside illumination image sensors for temperatures above 40°C (Fig. 6). The FSI devices show one activation energy for the dark current ($E_A \sim 0.99$ eV), which is close to the bandgap of Si (1.12 eV). The BSI devices show two activation energies, with a lower activation energy below 40°C ($E_A \sim 0.17$ eV). The higher dark current for BSI devices compared to FSI devices at 20°C could be due to generation-recombination centers, but more investigation is required.
The simulated quantum efficiency (QE) is generally in good agreement with the measured quantum efficiency (Fig. 7). At long wavelengths (> 700 nm), the simulation underestimates QE because there it does not account for light reflected back into the photodiode from the metal-insulator-metal (MIM) capacitors. At short wavelengths (< 350 nm) the simulation overestimates QE, perhaps due to small discrepancies in the thickness of the ARC layers used in the simulation versus the actual values.

Backside etch and deposition steps introduce additional plasma processing that can potentially damage the gate oxide. Hence, CMOS device reliability was measured before and after backside processing for the more sensitive devices; hot carrier for the 3.3V NMOS devices and negative bias temperature instability (NBTI) for the 1.8V PMOS devices. The hot carrier lifetime shows considerable spread for both FSI and BSI wafers (Fig. 8). However, both types of wafers easily pass the requirement for a 10 year operating life, and there is no obvious degradation associated with backside processing. The NBTI lifetime is more tightly distributed compared to the hot carrier lifetime (Fig. 9). Again, there is no obvious degradation from backside processing, and the wafers pass the requirement for a 10 year operating life at the use conditions (1.8V, maximum temperature = 125°C for the base technology).

B. Post-Radiation Results

The effect of proton radiation (63 MeV protons, 2.6x10^11 protons/cm²) on the image sensor noise and dark current was tested on BSI devices from a photodiode array test chip. Previous reports on 4T FSI image sensors have reported an increase in noise and/or dark current after radiation exposure [3,4,6,7]. In this work, we observed that both temporal noise and photo response non-uniformity (PRNU) increase after radiation exposure. The increase in PRNU is small, whereas the increase in temporal noise is more significant (Fig. 10). The increase in temporal noise could be due to the source-follower, the transfer gate, or the readout device. In a report from Place et al [6], the increase in temporal noise...
after radiation exposure was determined to be mainly due to the source-follower device.

The dark current was also observed to increase after radiation exposure, as expected (Fig. 11). The median dark current increased by ~100x after radiation exposure. The median dark current recovers by ~2x after a low temperature (100°C) anneal. The increase in dark current from proton radiation can be due to either displaced Si atoms in the photodiode or trapped charge in the SiO2 isolation or gate dielectrics (Fig. 12). Virmontois et al. [5] showed that the increase in dark current from proton radiation is 79% from the photodiode perimeter (oxide charge) and 21% from photodiode area (displaced Si atoms). In a number of studies, it is observed that there is some recovery of the dark current after low temperature annealing (80°C to 280°C).[3,5]. The recovery occurs even when the damage is caused by neutron radiation (ie. Si displacement damage only, no oxide charge), suggesting that the recovery is due to annealing of Si defects [5].

IV. CONCLUSIONS

A 1 megapixel global shutter, backside illumination CMOS image sensor has been developed for use in Medium Accuracy Star Tracking (MAST) applications. The chip was fabricated in a commercial 0.18 µm CMOS process, and includes a 16-bit on-chip ADC, allowing for either rolling or global shutter operation, and is radiation tolerant. Radiation was found to impact performance including significant shifts in dark current and temporal noise. To our knowledge, this is the first report on radiation tolerance of a backside illumination image sensor and on a global shutter image sensor.

ACKNOWLEDGMENT

The authors thank the staff of the ON Semiconductor wafer fab in Gresham, OR, for assistance with processing the wafers. The authors also thank Ed Flanigan and Chuck Spinner for their support.

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