Event-Driven Dual-Gain Fully-Depleted SOI Based X-Ray Detector for High Energy Particle Imaging

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Abstract

Astronomical satellite mission requires a detector with wide passband spectral response, low noise and high hit position pixel readout time. This paper presents an event-driven dual-gain pixel circuit using a novel silicon on insulator (SOI) based fully depleted detector. The trigger circuit categorizes the incoming energy into two different groups based on their energy level. The separation of signal strength into two different levels is used for the selection of the in-pixel gain. The designed detector with an in-pixel variable gain selection technique is used for the realization of low noise and wide dynamic range X-ray detector.

Keywords — SOIPIX, Active pixel sensor, X-ray detector, Wide dynamic range, In-pixel gain

1 Introduction

Charge coupled device (CCD) X-ray detectors are the state of art in most astronomical application (e.g. Chandra, Swift, Suzaku, XMM-Newton). It offers good spatial resolution for large format devices, high quantum efficiency and shows very linear behavior [1]. However it has high sensitivity to radiation damage, moderate energy resolution with low to moderate speed causing photon pileup at high count rates. The next generation detector should address these problems with an ability to window readout allowing fast readout of hit pixel, low sensitivity to radiation damage while maintaining the performance similar if not better than the current CCD X-ray detector.

We have been developing an event-driven XRPIX (X-Ray pixel) using 0.2 [μm] SOI based monolithic pixel detector developed by high energy research organization, KEK and OKI semiconductor co. ltd [2] for the future X-ray astronomical satellite missions with the aim of fast readout time (<10 [μs]) of hit pixel, wide passband (0.3-40 [keV]) and low noise (<3 [e$^-$]). The developed detector allows us to implement the on-chip integration of high speed low capacitance detector with CMOS based pixel and readout circuits. Fully depleted thick sensing region of the handle substrate is suitable for high energy imaging [3, 4].

2 SOI Pixel Detector

Pixel detector shown in Fig. 1 uses a fully-depleted SOI (FD-SOI) for the electronic circuitry and a high-resistivity n or p type substrate for the detector [2]. In order to achieve high quantum efficiency for high energy particle imaging (e.g.>10 [keV]) thick depletion layer of 140 [μm] is used [5]. High voltage is applied at the backside of the detector for achieving a fully depleted substrate. High-density buried p-well (BPW) is formed on the backside of the oxide insulator which acts as a shielding layer between the charge detector and the circuit. Backgate-potential pinning SOI pixel (BPSPIX) structure uses a fixed surface potential at BPW to minimize the backgate effect caused by the capacitive coupling between the circuit and charge detector and the dark current generation at the backgate surface [6]. Also, the buried n-well 2 (BNW2) formed under BPW prevents the punch-through effect by creating a potential barrier to holes. The lateral electric field created by the BNW2, BNW3 and BPW2 layer increases the charge collection efficiency by further pushing the electrons into the charge detector.

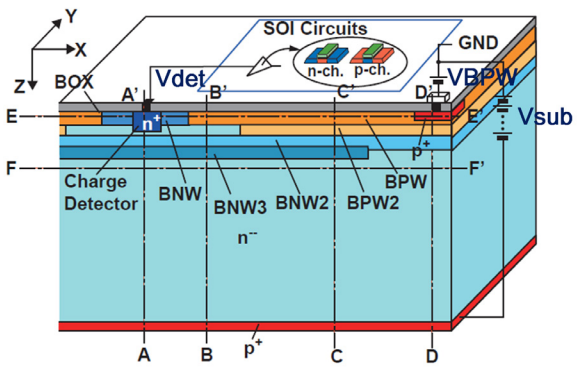


Figure 1: Proposed SOI Pixel Detector

3 Event Triggered Pixel Circuit

Pixel circuit comprises of trigger circuit and signal processing circuit. Fig. 2 shows the unit pixel circuit which uses a charge sensitive amplifier (CSA) with a selective feedback capacitor (C_F) for in-pixel gain and sampling circuits. The CSA type pixel has shown improved spectroscopic performance in our experiments [7]. The design of the charge amplifier is important for obtaining the desired performance. Gain of the charge amplifier should be high enough (>100) to minimize the effect of the floating diffusion capacitance. Also, the conversion gain can be solely determined by the capacity of the C_F if the gain of the amplifier is large in the operating range.

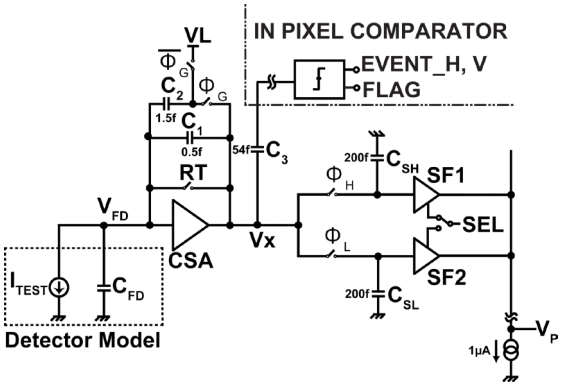


Figure 2: Dual Gain CSA Type Pixel Circuit

Figs. 3a and 3b show the two different configuration for the selection of C_F ($C_1 = 0.5$ [fF] and $C_2 = 1.5$ [fF]). If G_{AMP} is the gain of the charge amplifier and C_t is the total parasitic capacitance including floating diffusion capacitance (C_{FD}) and input capacitance (C_i) for the input transistor of the charge amplifier, then conversion gain (G_C) is given by one of the two cases.

Case 1: $\phi_G = 1$

$$G_C = \frac{G_{AMP}.q}{C_t + (C_1 + C_2).G_{AMP}} = \frac{q}{C_1 + C_2} \text{ (For } G_{AMP} >> 1) \approx 80[\mu V/e-]$$

Case 2: $\phi_G = 0$

$$G_C = \frac{G_{AMP}.q}{C_t + C_1.G_{AMP} + C_2} = \frac{q}{C_1} \text{ (For } G_{AMP} >> 1) \approx 320[\mu V/e-]$$

Timing for the pixel operation is shown in Fig. 4. The operating point of the amplifier is shifted by changing the bias condition and a PMOS reset transistor is used for better dynamic range. After the reset switch closed, there is a charge injection from the reset transistor. The charge injection by the reset transistor is controlled by a proper choice of the transistor size and

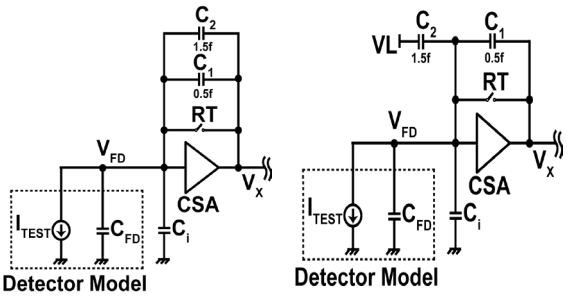


Figure 3: Gain Selection Configuration

low level voltage applied to the reset transistor. Both high and low gain reset voltage is then sampled after the reset operation.

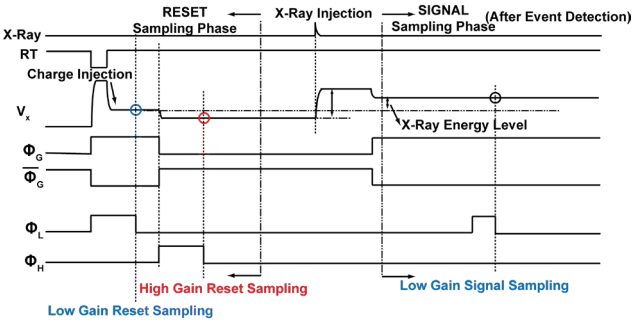


Figure 4: Pixel Timing Diagram

Arrival of X-ray event is continuously scanned using in-pixel event detection circuit. Fig. 5 shows the in-pixel trigger circuit which uses a chopper-type comparator. Circuit is setup at high gain state by default after reset. Upon the arrival of the energy greater than the minimum threshold, an event flag is generated. The trigger circuit categorizes the incoming energy into two different levels. Two threshold voltages are used for event detection and energy level distinction. The separation of signal strength into two different levels is used for the selection of the in-pixel gain. High conversion gain (320 [V/e$^-$]) is applied for low incoming X-ray energy while comparatively low conversion gain (80 [V/e$^-$]) is applied for the X-ray with sufficiently high energy.

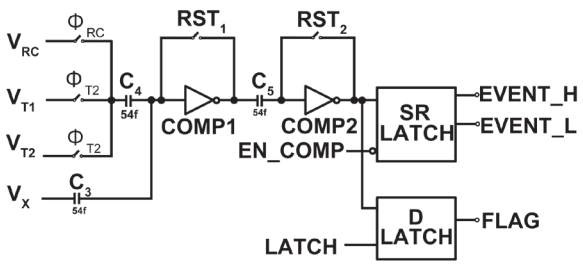
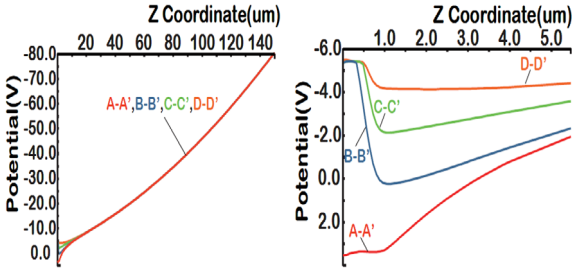


Figure 5: In-Pixel Comparator Circuit

4 Results

Fig. 6a shows the vertical potential distribution of the SOI pixel detector along the axis (A-A′, B-B′, C-C′ and D-D′) as indicated in Fig. 1 for the total substrate depth of 140 [μm]. Generated electrons will be directed towards the higher potential nearer to the surface. Fig. 6b is magnified version of the vertical potential distribution with substrate depth from 0 to 5 [μm]. When BPW is pinned to -5 [V], B-B′, C-C′ and D-D′ shows the potential barrier to holes preventing the occurrence of the punch-though. Voltage at the detector is set to 3 [V]. A-A′ has the highest potential near detector creating an easy path for the electron to be collected in the charge detector.



(a) (b)

Figure 6: Vertical Potential Distribution

Fig. 7 shows the potential distribution along horizontal axis. E-E′ is the potential profile at the surface while F-F′ is the potential near BNW3 showing the capability of fast charge collection in the pixel. Any electron being generated within the pixel detector is collected at the charge detector.

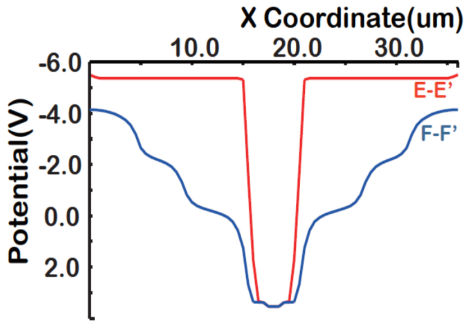
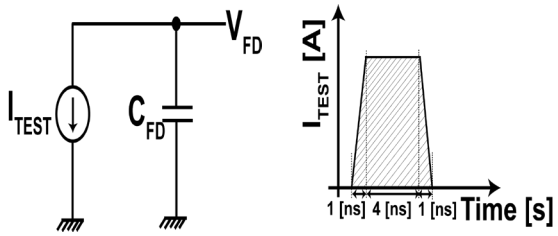


Figure 7: Horizontal Potential Distribution

Fig. 8a shows the photo diode model used for the simulation of the pixel circuit. I_{TEST} is the constant current source for an equivalent X-ray signal injecting the charge by the trapezoidal input as shown in fig. 8b. Equivalent charge generated by the input X-ray energy is given by the shaded area of the trapezoid (Q [C] = I_{TEST} [A] x Time [s]). For example, X-ray energy generated from the Cadmium-109 (109Cd) source of 22.2 [keV], silicon generates about 6082 e- corresponding to the equivalent current of 195 [nA] for the time of 5 [ns] trapezoidal input.



(a) (b)

Figure 8: Photodiode Model with Test Input Source

Fig. 9 is the simulation result of the designed pixel for wide energy range. Plots for both low and high gain are shown. Readout circuit in XRPIX series is designed with 1 [V] peak-to-peak swing. The graph depicts that the detection of target X-ray energy range (0.3 to 40 [keV]) is achievable.

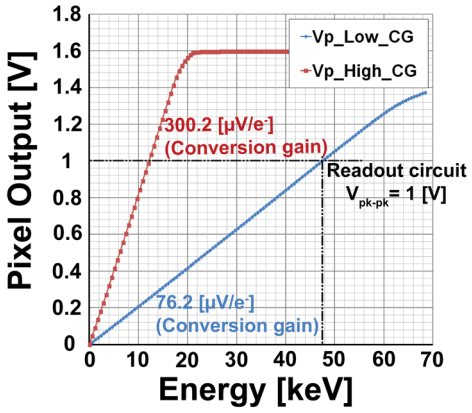


Figure 9: Pixel Output

Total noise of analysis results for two different feedback capacitors with input transistor size (W = 1 [μm] and L = 1 [μm]) of the CSA amplifier are plotted in Fig. 10. N_{Total} is the total noise including thermal noise and 1/f noise for the pixel circuit. The noise for the C_F of 0.5 [fF] is calculated to be 3.5 [e^-] while the noise for C_F of 2 [fF] is 5.7 [e^-] (for C_{FD} = 4 [fF], C_{OX} = 5 [mF], T_{CDS} = 1 [ms], C_L = 200 [fF]). The noise is further increased by the readout circuit.

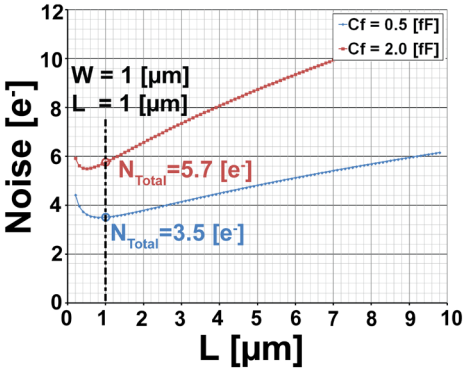


Figure 10: Pixel Circuit Noise

5 Conclusion

An experimental 16x16 pixel array chip shown in Fig. 11 is designed and manufactured using 0.2 [μm] SOI pixel technology. The designed prototype chip consists of two different types of pixel circuits (type 1: continuous-time integration and type 2: CSA). Event driven CSA type pixel is described in this paper.

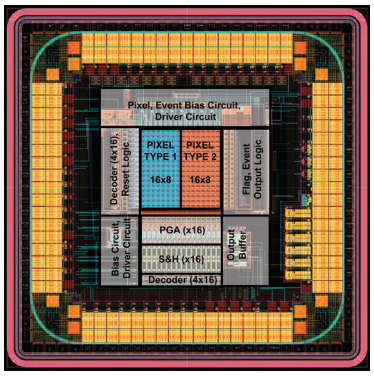


Figure 11: Implemented Chip Layout

The designed BPSPIX detector uses both lateral and vertical electric fields to achieve very fast and high charge collection efficiency. The fully depleted SOI pixel detector with dual gain pixel circuit architecture is used to realize a high charge-to-voltage conversion gain. In-pixel event detection circuit serves two different propose; one is the detection of the X-ray signal arrival and other is the determination of strength of the incoming signal using two bit code. In-pixel variable gain technique is used for low noise and wide dynamic range.

Using the integrated event triggered circuit in the BPSPIX detector X-ray energy particle imaging is feasible. The capability of correlated double sampling (CDS) technique for kTC noise canceling and programmable gain amplifier (PGA) in the readout circuit aids in the further improvement in signal-to-noise ratio (SNR) of the circuit. With the advancement in active pixel sensor (APS) based imager, the SOI based XRPIX is the capable candidate for future satellite missions to replace CCD X-ray detectors.

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