High Speed Backside Illuminated TDI CCD-in-CMOS Sensor

Pierre Boulenc1, Jo Robbelein1, Linkun Wu1,2, Vasyl Motsmy1, Luc Haspeslagh1, Stefano Guerrieri1, Jonathan Borremans1, Maarten Rosmeulen1

1imec, Kapeldreef 75, B-3001 Leuven, Belgium
2Vrije Universiteit Brussel – ETRO Dept., Pleinlaan 2, 1050 Brussels, Belgium

Tel: +32 16 28 15 44, E-mail: pierre.boulenc@imec.be

Introduction
Charge-Coupled-Devices (CCD) continue to be the technology of choice for Time Delay Integration (TDI) imaging. A recent evolution is the emergence of monolithic CCD-in-CMOS [1-2], which combines noiseless charge transfer of CCD with the efficiency of CMOS high speed drivers and readout. However, the limited voltage budget available in CCD-in-CMOS challenges this technology to deliver on the trend of higher line rates.

This work presents the successful characterization of a Backside Illuminated (BSI) high speed CCD-in-CMOS sensor up till 1 MHz. The first section of this paper describes the concept and implementation of the CCD-in-CMOS sensor. Characterization in darkness is then presented and first figures of merit are extracted. Charge Transfer Inefficiency (CTI) measurements are discussed in a dedicated section. Finally, the fourth section focuses on optical characterization.

CCD-in-CMOS sensor description
Imec’s CCD-in-CMOS platform is realized by adding a few process modules to a standard 0.13 μm CMOS process flow containing dual gate oxide standard nMOS and pMOS transistors with 1.2 and 3.3 V flavors [1-2]. Dedicated buried channel, isolation, well and junction implants for the CCD elements and readout transistors have been used to ensure CMOS compatible operating voltages (Figure 1).

Advanced single-poly gate patterning is employed to enable narrow poly-to-poly spacing of 110 nm between the CCD gates. In order to limit the dark current, no Shallow-Trench-Isolation (STI) is used for column separation. Imec’s CCD-in-CMOS process includes dedicated steps at the end of the production flow to enable Backside Illumination (BSI).

The 1024x512 pixel TDI image sensors have been designed and manufactured using the CCD-in-CMOS technology previously mentioned. On-chip CMOS logic and CCD drivers with slew rate control (Figure 2) clock the 1024 column 4-phase CCD array, with 512 rows and stage selection. Analog column-parallel readout samples Reset and Video signals, serializes and buffers the output to off-chip Analog-to-Digital-Converters (ADC). Correlated Double Sampling (CDS) is then performed to cancel out reset noise. The sensor uses CMOS-rated supply voltages up to 3.3 V and a negative supply of -1.4 V, while being fully compatible with standard CMOS readout.

Figure 2: CCD-in-CMOS sensor block diagram.

The CCD column sampling circuits share a limited amount of buffers. As a result, the readout bandwidth per buffer is limiting the full-frame line rate to 20 kHz. This test vehicle can be improved thanks to higher circuit integration like column level ADCs [3]. In this work, line rates greater than 20 kHz have been reached by reducing the number of sampled columns accordingly.

Darkness characterization
Dark Signal Transfer Curves (DSTC) have been measured at 15°C, 25°C and 60°C by means of flush / integration / readout sequences with increased integration time. The flush and readout cycles are performed at 200 kHz in order to limit the amount of charges collected during these cycles. Figure 3 shows noise vs. signal plot used for Conversion Gain (CG), Full Well Capacity (FWC) and noise floor determination. A lower noise floor is measured for lower temperature, indicating that dark current shot noise during readout sequence is still dominant above 15°C. The CG is 23 μV/electron and the saturation FWC is greater than 20000 electrons. Maximum noise is reached for a signal level of 15000 electrons. This corresponds to the onset of blooming, when electrons get redistributed in neighboring pixels within the same column. In the next sections, this specific signal level will be referred to as the bloomed FWC [4].

Figure 1: CCD-in-CMOS column schematics.
Pixel level dark current at each temperature has been derived from full frame linearity measurements, enabling the extraction of the dark current activation energy distribution as plotted in Figure 4.

As a comparison, a FSI sensor exhibits a peak around 0.64 eV, commonly associated with the Phosphorus-Vacancy defect “E-center” [4-6]. A BSI sensor with the same process but additional backside thinning and passivation steps, reveals a single peak around 0.79 eV possibly linked to more complex vacancy clusters and oxygen defects [7].

**Charge Transfer Inefficiency**

CTI measurements [8] have been carried out with line rates ranging from 2 kHz up to 1 MHz at various temperatures and signal levels. A pulse train is injected at the top of the sensor thanks to a dedicated input structure common to all the CCD columns. The injected signal level can be controlled by the voltages of the input Floating Diffusion (FD) and Input Transfer Gate (ITG) (Figure 1). CTI degradation because of traps is visible at low line rate for signal levels below 8000 electrons (Figure 5) [4-6]. A slow transfer allows traps to capture electrons before the next transfer takes place and release them in subsequent transfers.

For signals between bloomed and saturation FWC, electrostatic potential buckets are almost completely filled with charges. Compared to empty pixels, full pixels exhibit smaller fringing fields thus have a degraded transfer efficiency [4, 5]. From Figure 5, the signal level above which CTI is degraded changes with the line rate. The faster the CCD is clocked, the higher is the signal that can be transported with negligible losses.

Figure 6 shows the DSTC variance with respect to mean signal for various readout line rates at 25°C.

The dependence of the bloomed FWC with respect to the readout line rate is clearly visible. When line rate increases, electrons have less time to escape the almost completely filled potential buckets. Therefore, clocking the CCD faster allows to reach a greater bloomed FWC.

Bloomed FWC has also been measured at 15°C, 25°C and 60°C for line rates of 2, 20 and 200 kHz (Figure 7). A clear decrease of bloomed FWC is observed when temperature increases. At higher temperature, electrons have more thermal energy to jump over the barrier between a filled pixel and its neighbor (in the same column) which contains slightly less charges.

These results can be explained by thermionic emission over the electrostatic potential barriers between pixels combined with the time limitations set by the CCD gates clocking period [4].
Therefore, observations from Figure 5 can be explained by the difference in bloomed FWC with respect to the line rate. An injection level of 50% saturation FWC will be below the bloomed FWC provided the CCD is clocked faster than 2 kHz and at a temperature below 25°C. CTI has been measured at different temperature for line rates between 2 kHz and 1 MHz (Figure 8). The degradation of CTI with increasing temperature and slow line rates is two-fold. Firstly, injected then transferred signal can be greater than the bloomed FWC as observed in Figure 5. One needs to clock the CCD sensor fast enough to increase the bloomed FWC above the injected signal. Secondly, traps become more active in trapping and releasing electrons at higher temperature [4-6].

When trap emission time constant is comparable to transfer time, charges can be trapped and released in the subsequent transfers, thereby increasing CTI. When transfer time gets much shorter than the trap emission time constant, transfer and readout occur before charges are released, no apparent impact on CTI is thus visible and CTI below $10^{-3}$ is obtained up till 800 kHz. The CTI increase above 400 kHz is related to the output stage bias. Changing the Output Gate (OG1 in Figure 1) bias from 0 to -0.7 V increases this effect. The electric field between the last CCD gate and the bottom FD during transfer gets smaller, degrading transfer efficiency at the output stage.

**Optical characterization**

As mentioned previously, the sensor manufacturing process includes backside thinning and passivation steps leaving a 5 μm thick P-type substrate with Anti-Reflective Coating (ARC) tuned to maximize sensor response in visible light. Since the TDI sensor does not have electrical nor mechanical shutter, special care must be taken when performing measurements under illumination. The optical measurement method consists of flush / integration / readout sequences with illumination triggered only during integration. This technique avoids gathering photo-generated charges during readout which would increase the noise floor because of the associated photon shot noise. By increasing the light pulse duration within the fixed integration time, the Photon Transfer Curve (PTC) is generated (Figure 9) confirming CG and FWC extracted from measurements in darkness.

**Figure 8: CTI vs. line rate for 10000 electrons transferred signal at 15°C, 25°C and 60°C.**

**Figure 9: Photon Transfer Curve with increasing light pulse duration within fixed integration time compared to 25°C DSTC. Readout at 200 kHz.**

Quantum Efficiency (QE) measurement on a TDI CCD is more complex than on a standard CMOS image sensor since no per pixel shutter or transfer gate is available. Flush / integration / readout sequences have also been used with increased integration time but light is always on since our QE setup cannot be pulsed accurately enough to control the integrated amount of incoming photons. Like for the DSTC, clocking the sensor at 200 kHz during flush and readout cycles reduces the background signal and its associated noise floor. Provided the photon flux is known from calibration data at each wavelength, QE is derived from the slope of signal with respect to integration time linearity plots with equation (1):

$$QE(\lambda) = \frac{dS}{dt \times A \Phi_{photons}(\lambda)}$$  

(1)

where $S$ is the signal in number of electrons, $t$ is time in s, $A$ is the pixel area in cm², $\Phi_{photons}(\lambda)$ is the photon flux at wavelength $\lambda$ in photons/s·cm².

As shown in Figure 10, QE with respect to wavelength peaks at 89% at 530 nm. The shape of the curve for wavelengths below 450 nm strongly depends on the ARC optimization. Red / near IR response is directly impacted by the thickness of the substrate.
The sensor has been designed with a slanted metal edge of 0.2 degrees on top of the pixel array enabling horizontal edge spread function extraction [9]. The horizontal Modulation Transfer Functions (MTF) has been computed and plotted in Figure 11 at 3 different wavelengths. As expected for a BSI sensor, MTF at Nyquist is higher at longer wavelengths since the electrons are generated closer to the collection wells and have less distance to travel to neighboring pixels in the silicon substrate.

Conclusions

In depth analysis of signal transfer curves for different temperatures and readout line rates is reported in this paper. The bloomed FWC was found to depend on line rate and temperature. Such observations are critical if one wants to operate the CCD sensor in optimal conditions. Moreover, this work demonstrates best-in-class low-light and high-speed capabilities of Imec’s CCD-in-CMOS technology (Table 1). With CTI below 5.10^{-5} up till 800 kHz and peak QE of 89% with MTF greater than 0.4 at Nyquist, such a sensor is an attractive alternative to CMOS-only devices for light starved TDI applications.

Acknowledgements

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Table 1: Comparison with published state of the art CCD-in-CMOS technologies.

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References