

12-bit Column-Parallel Single-Slope ADCs with Operation-Period-Reduced Time-to-Digital Converters for CMOS Image Sensors

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Abstract—The Single-Slope (SS) ADC is a simplified architecture; therefore, it is widely used in a variety of image sensors. But, to achieve a high-speed operation without using a high-speed clock is almost impossible. In order to achieve a high speed operation, using a very high-speed clock will increase the power consumption of the ADC significantly. In this paper, we propose a 12-bit column-parallel single-slope (SS) ADC with operation-period-reduced time-to-digital converter (TDC) and the application of these ADCs to two types of CMOS Image Sensors. By reducing the operating period of the TDC, the developed ADC has been able to decrease the power consumption per column by approximately 70%. The architecture of the ADC with the proposed TDC achieves 1.728-GHz operation with the same power consumption as the conventional SS ADC at 108-MHz.

I. INTRODUCTION

For mirrorless interchangeable lens cameras, demand for high-quality imaging, high-speed shooting, and a large number of recordable pictures has been increasing. Therefore, a low-noise readout, a high-speed operation, and low-power consumption are required for CMOS image sensors. In order to achieve a low-noise readout, a high-speed operation, and low-power consumption, we propose a 12-bit column-parallel SS ADC with operation-period-reduced TDC, and apply these ADCs to two types (small type, or large type) of CMOS Image Sensors.

II. ARCHITECTURE

Figure 1 shows a block diagram of the image sensor. The ADC mainly consists of a voltage controlled oscillator (VCO) and a ramp generator arranged outside column-parallel ADCs area, and Column-Parallel Single-Slope ADCs with Operation-Period-Reduced TDCs, which has a comparator that compares ramp signal (V_{RAMP}) and pixel signals (V_{PIX}), a counter, a timing controller, and a 16-bit latch (LAT [15:0] & ENCODER). Figure 2 shows a timing chart of 1 Horizontal (1H) Period. First, comparing the pixel signal (V_{PIX}) corresponding to reset level with the ramp signal (V_{RAMP}) is done during the 1) period. Next, encoding logic states held in the 16-bit latch is done during the 2) period. Then, inverting the count value held in the counter (complementary operation) is done during the 3) period. Next, comparing the pixel signal (V_{PIX}) corresponding to signal level with the ramp signal (V_{RAMP}) is done during the 4) period. Finally, encoding logic states held in the 16-bit latch is done during the 5) period. Herewith, a digital data (CODE [11:0]) corresponding to a difference between the reset level and the signal level is obtained. The digital data is transmitted to a subsequent circuit in the background of the ADC operation described above.

Figure 3 shows a block diagram of the ADC with the proposed TDC [1]. Figure 4 shows a timing chart. The 16-bit latch, the counter, and the timing controller comprise the TDC. During a ramp period (the start timing is when the ramp generator starts to generate a slope; the stop timing is when it stops), the VCO which includes an asymmetric ring oscillator generates 16-phase (multi-phase) clocks (CK0, CK1, ..., CK15) whose frequency is 108-MHz, and each clock has a $\pi/8$ (579 ps) phase shift [2]. The counter counts a clock (CK15) via the latch (LAT [15]) like a conventional SS ADC at 108-MHz and composes the upper bits (8 bits) of the ADC, and the 16-bit latch latches the signal state of the multi-phase clocks (one of states 0 to 15). The state is converted to 4-bit binary code by using an encoding method that uses the thermometer code used in Flash ADC in time series and composes the lower bits (4 bits) of the ADC [3]. The timing controller (Type 1, or Type 2) that consists of only basic gates, generates two signals (V_{LSTART} , V_{LSTOP}), which have a very short predetermined time difference (latch period of about 10 ns), when the output signal (V_{COUT}) of the comparator changes. In small type, Type 1 is used to generate the two signals by using the propagation delay of the basic gates. In large type, Type 2 is used to generate the two signals by using the difference between the threshold levels ($V_{th,L}$, $V_{th,H}$) of the basic gates (A, B). The latches (LAT [14:0]) except the latch (LAT [15]) receive the two signals and operate during the latch period. Therefore, the latches (LAT [14:0]) operate only for about 20 ns ($10 \text{ ns} \times 2$ for digital CDS) within the ramp period of about 3.3 μs . Since this period is less than 1/100 of the ramp period, the consumption during this period has hardly any effect on the total power consumption of the ADC. If the 16-bit latch operates with 108-MHz multi-phase clocks in the ramp period, it will have a large operating current. Therefore, reducing the operating period of the 16-bit latch for the ramp period results in an ADC with low-power consumption. Actually in our study, the ADC with a conventional TDC (TDC without using the timing controller) in a column consumed 50.9 μA per A/D conversion period. Furthermore, the increase in size of the circuit area is suppressed better than most other column-parallel ADCs that do include amplifiers and capacitors. These are very strong points that the ADC has among other ADC architectures.

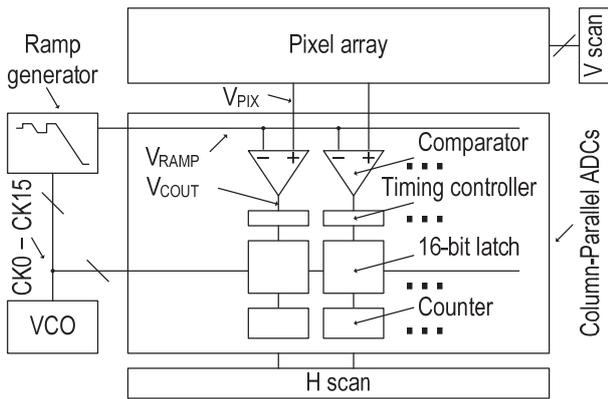


Figure 1: Block diagram of image sensor

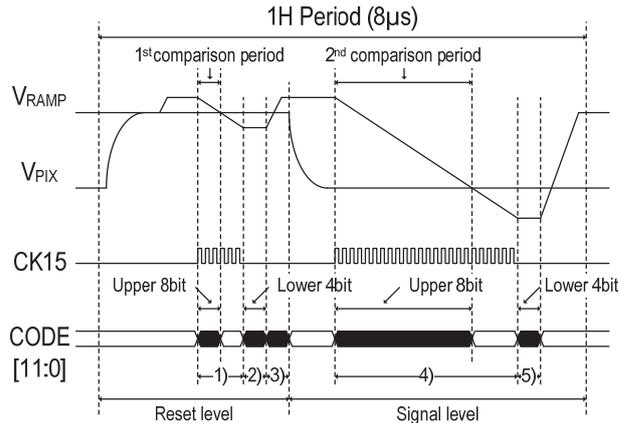


Figure 2: Timing chart of 1H Period

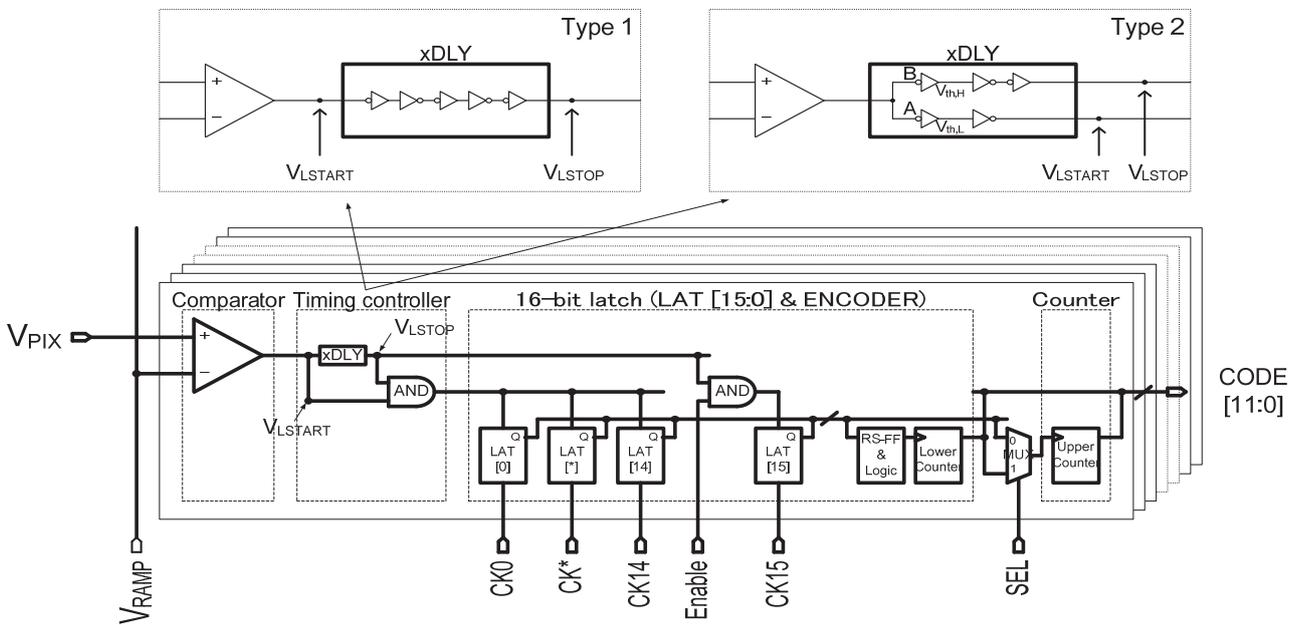


Figure 3: Block Diagram of ADC

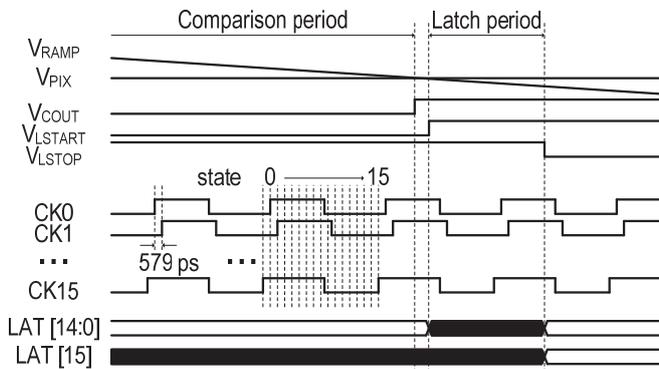


Figure 4: Timing chart for TDC operation

Table 1: Chip Characteristics

| Item | 1 Mpixels | 18 Mpixels |
|--------------------|-------------------------------|---------------------|
| Process | 0.11 μ m 2Poly4Metal | ← |
| Power supplies | 3.3V / 1.5V | 3.3V / 2.1V |
| Max. clock freq. | 108 MHz | ← |
| Time resolution | 579 ps | ← |
| Voltage resolution | 244 μ V/LSB (Gain:0dB) | ← |
| ADC DNL | ± 0.3 LSB | ± 0.5 LSB |
| ADC INL | 2.2 LSB | 8.2 LSB |
| ADC area | 3.2 x 1700 μ m | 3.2 x 2150 μ m |
| ADC current | 21.4 μ A/Column | 15.9 μ A/Column |

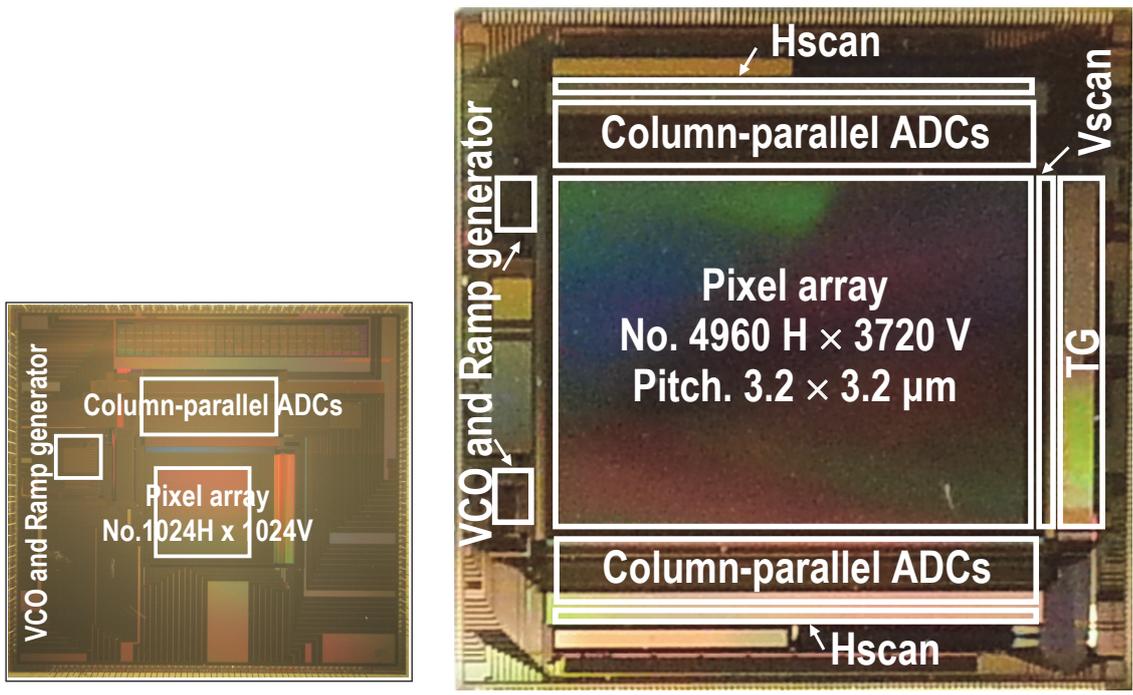


Figure 5: Chip micro-photographs

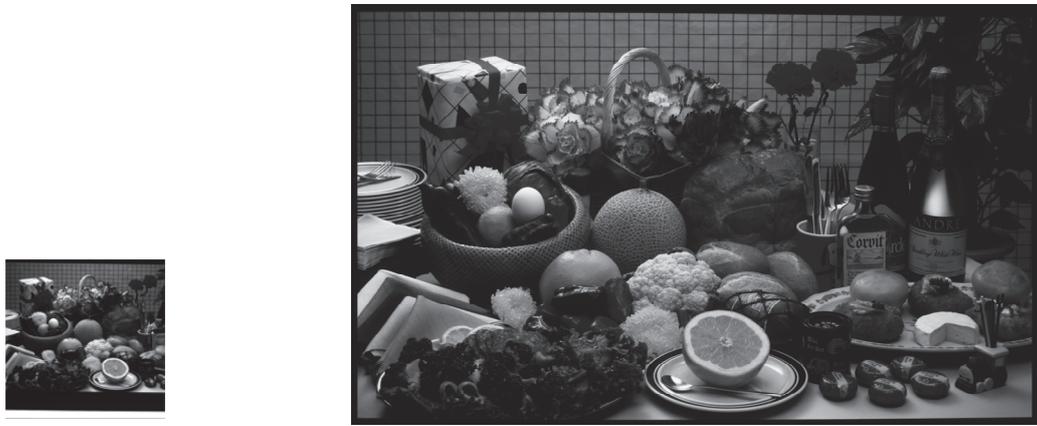


Figure 6: Sample Images

III. MEASUREMENT RESULTS

Figure 5 shows chip micro-photographs, and figure 6 are sample images. Table 1 summarizes the chip characteristics [4-5]. These chips were fabricated in the same process (0.11- μm 2-poly 4-metal CMOS). The numbers of pixels are 1 Mpixels (1124 H \times 1024 V) and 18 Mpixels (4960 H \times 3720 V) respectively, and the pixel pitch is 3.2 μm . The maximum clock frequency is 108 MHz, and the time resolution is 579 ps. The ADC resolution is 12 bits, and the voltage resolution is 244 $\mu\text{V}/\text{LSB}$. The ADC currents in a column are 21.4 μA in 1 Mpixels and 15.9 μA in 18 Mpixels respectively.

IV. CONCLUSION

We proposed 12-bit Column-Parallel Single-Slope ADC with Operation-Period-Reduced Time-to-Digital Converter, and applied them to two types of CMOS Image Sensors. By using this technology, the power-consumption of the developed ADC has been decreased by approximately 70 %. Furthermore, because of the non-necessity of analog circuit elements, the architecture of the ADC with the proposed TDC is more suitable for fine CMOS processes and column-parallel ADCs.

References

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