A 5-Megapixel 100-frames-per-second 0.5erms Low Noise CMOS Image Sensor With Column-Parallel Two-Stage Oversampled Analog-to-Digital Converter

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Abstract - This paper reports a CIS readout channel conceived for half-electron noise by combining semi-empirical pixel noise model fitting, S&H-free two-stage ADC with over-sampling, optimized pixel control and Correlated Multiple Sampling (CMS). The ADC architecture consists of a first-order ΣΔ modulator that generate the MSBs followed by a ramp converter. Closed loop self correction is employed for low non-linearity. Correlated Double Sampling (CDS) is implemented in the 1st ΣΔ modulator by integrating signal and reset in opposite directions.

I. Introduction

Image and vision sensors are flooding all application territories, their usage and markets are increasing at exponential pace, and they are expected to play important roles in practically all IT domains [1]. Such extensive usage poses quite diverse design challenges, including high-speed, low-light, depth estimation, high dynamic range or on-the-fly extraction of the information conveyed by visual stimuli [2], among others.

Sensors suitable for sub-mililux light can be implemented by using either conventional active pixels with integrating photo-diodes or other highly sensitive devices, such as for instance SPADs (Single Photon Avalanche Diodes). However, architectures based on conventional APSs feature larger fill factors without dead times [5][6] and are hence suitable for high-quality applications including scientific imaging, medical imaging and high-reality video systems [7].

Low-light sensors based on integration-mode photo-diodes call for low-noise pixel and readout channels [3][4]. Sub-electron low-noise applications demand also large dynamic range. The sensor in this paper improves the architecture reported in [3] and employed in [4]. It achieves 83dB with half-electron readout noise owing to the combination of different strategies including noise model fitting, multi-stage ADCs, over-sampling and CMS.

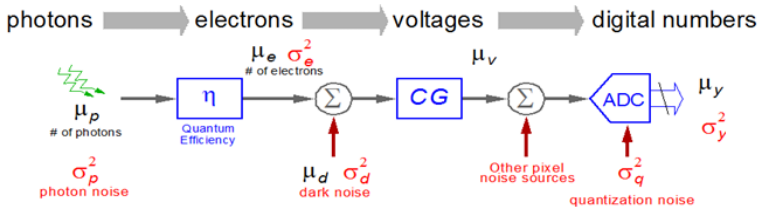
Fig.1 shows an overview of the noise sources arising in the path from photons to DNs (Digital Numbers). Some of them are not addressed in this paper for the reasons listed below:

- Dark charges are very small in pinned photodiodes (~10e/s) and dark noise is negligible for standard exposures times. They can be further reduced by active cooling packages.
- Shot noise is negligible under dark conditions.
- *kT*/*C* is cancelled by CDS.

Emphasis is hence placed on pixel noise sources and ADC noise. Strategies adopted for these sources are outlined in the Table inset of Fig.1.

II. ADC Converter

ADCs and mixed-signal readout channels are crucial for image and vision sensor performance [8]. Our strategy relies on a per-column, two-stage ADC which resolution can be tuned from 14-bit to 16-bit and that is designed to operate at 100fps. Similar ADC strategy has been employed previously in the LoNIS CIS [3][4]. This latter readout channel employs S&Hs (Sample-&-Hold) at the ADC front-



Pixel Noise Sources	
Source follower thermal noise	• over-sampling • S&H-free operation • CMS
Source follower low-frequency noise	• CDS-CMS (partially) • SF sizing • LF model fitting
Transfer (TX) Noise	• control waveform shapes
ADC noise	• two-stage ADC • adaptive gain correction • over-sampling

Figure 1: Overview of Noise Sources in the Photon-to-DN Path.

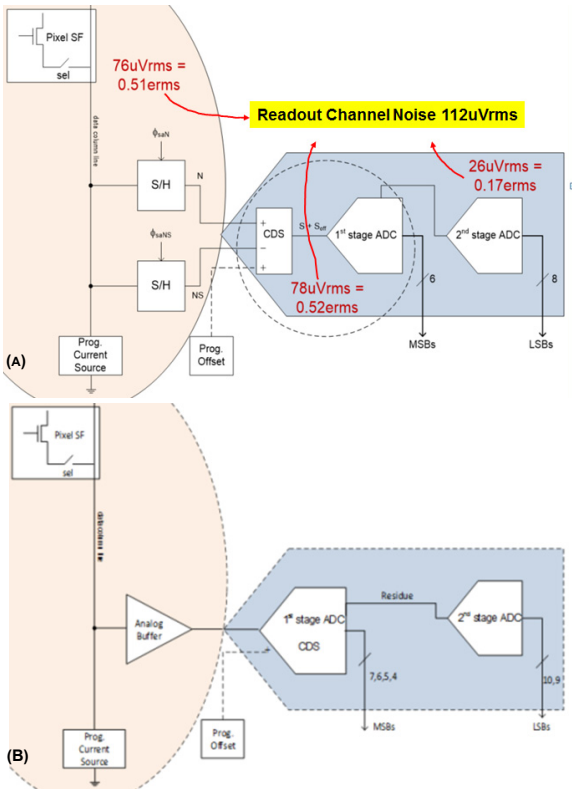


FIGURE 2: (A) READOUT CHANNEL OF THE LONIS SENSOR [3]; (B) PROPOSED S&H-FREE, TWO-STAGE ADC.

end – see Fig.2(a). The figure includes a summary of the rms noise levels featured by the architecture. The different noise contributions amount to an accumulated readout noise of 112μVrms – close to 1erms. To go below this value, the new architecture removes the S&Hs, see Fig.2(b), and relies on empirical pixel noise model fitting and subsequent pixel optimization.

Fig.3(a) shows a conceptual schematic of the ADC excluding clock waveforms. Fig.3(b) shows the global readout timing diagram. The line time value of 5μs labelled in the diagram corresponds to 14-bit resolution. Note in Fig.3(b) that each column is selected two times within a line interval. During first selection, the reset value is sampled and integrated during N iterations, without S&H required. The accumulated data is compared during each iteration to half the reference value; if larger, the reference is subtracted from the accumulated capacitor. During second selection, the photo-diode charge is transferred to the sense node and the signal value gets integrated by the first ADC stage. CDS operation is completed while the signal is being integrated. To that purpose, the signal value gets integrated in opposite direction to the reset value – see Fig.3(c) for the concept. It involves interchanging the pixel and the reference sampling phase. The converted data is the number of times the full-scale reference voltage has been subtracted. After N iterations, the residue is contained in the output capacitor and it is sampled by a single slope ADC second stage.

Because the first stage is over-sampled, pixel noise contributions are reduced as compared with LoNIS ADC [3] where signals coming from the pixel are sampled and remains "constant" during integration. Hence In fact, the thermal noise coming from the pixel is reduced by a factor sqrt(N), whereas the flicker noise is attenuated by the CDS operation.

CMS is also included as a design option of the new low-noise architecture. When CMS technique is used the readout is reconfigured to first convert M samples of the reset value, and then M samples of the signal value. CDS is performed externally after averaging reset and signal values separately.

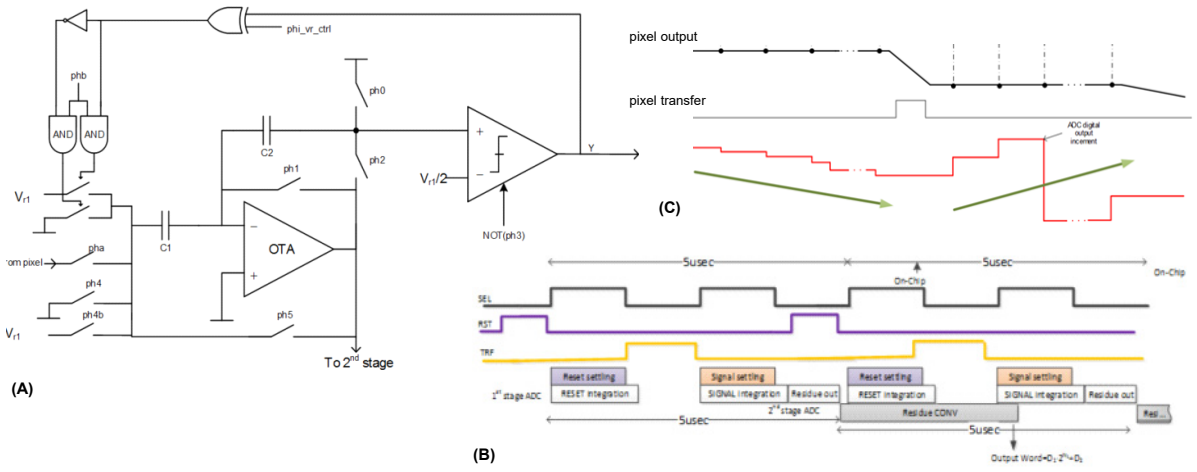


FIGURE 3: (A) CONCEPTUAL SCHEMATICS OF THE S&H-FREE, TWO-STAGE ADC; (B) LINE TIMING DIAGRAM; (C) ILLUSTRATION OF CDS OPERATION.

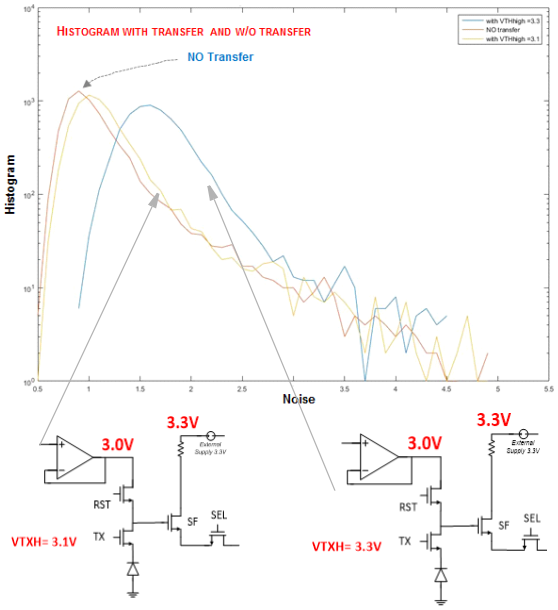


FIGURE 4: NOISE HISTOGRAMS FOR TWO TRANSFER GATE LEVELS.

Analog and digital ramps are common to all columns. The analog ramp swings over the whole signal range synchronized with the digital ramp. When the analogue ramp crosses the input the digital code is sampled. As a summary of ADC performance, Table 1 shows the readout noise excluding pixel contribution.

RESOLUTION	14bit	15bit	16bit
READOUT NOISE [UVRMS]	84.11	53.31	35.32

TABLE 1: READOUT NOISE WITHOUT PIXEL CONTRIBUTION

III. PIXEL NOISE REDUCTION

Noise during charge transfer to the floating diffusion is caused by electrons that remain in the overlap capacitor between the transfer gate and the photodiode. This noise is addressed by setting levels and skews of the control waveforms. Fig.4 illustrates the impact of level control by showing noise histograms for two different transfer gate levels.

Source follower noise is a crucial for low-noise design. Fig.5 shows a conceptual block diagram for calculation of the source follower noise. Noise is first filtered by the column capacitor with pole ω_c and then further filtered due to the CDS operation which involves a delay by T_o. Analysis returns the following result:

$$\overline{v_{nCDS}^2} = \overline{v_{nCDS}^2}\Big|_{th} + \overline{v_{nCDS}^2}\Big|_{pink} =$$

$$= \frac{S_{N,th}}{2} \cdot (1 - e^{-\omega_c \cdot T_o}) + 2N_f \cdot [\gamma - \ln(\omega_c \cdot T_o] \approx \quad (1)$$

$$\approx \frac{S_{N,th}}{2} + 2N_f \cdot [\gamma - \ln(\omega_c \cdot T_o]$$

where $\gamma = 0.577215$. This model can be employed

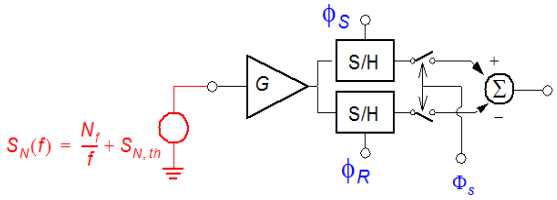


FIGURE 5: CONCEPTUAL BLOCK DIAGRAM FOR CALCULATION OF THE SOURCE FOLLOWER NOISE.

to guide design parameter choice. Particularly it shows that the shorter T_o the more effective the filtering of low-frequency components. However, T_o value has constraints, namely:

i) margin must be given for transfer operation – minimum $0.5\mu s$;
ii) transients must be large enough to make settling errors negligible.

Also, measurements from test chips show that the model of eq.(1) has inaccuracies, due among other things to deviations from the $1/f$ law happening at very low frequencies. These inaccuracies manifest particularly with T_o changing as Fig.6 illustrates. Similar deviations from design models are observed regarding the other parameters available for noise reduction. It motivates the extraction of semi-empirical noise models which are fitted using measurements from test chips with different source follower sizes and the readout channel of LoNIS; the methods consists of:

i) Comparing different pixel sizes based on measurements with LoNIS readout channel; Table 2 sows the measured values, where **v0**, **v1** and **v2** denote three different pixels instances included in the test chip.
ii) Extracting N_f value for each pixel by fitting time domain simulations and frequency domain simulations.

Models extracted this way are used to explore the design space for lower possible noise performance.

PIXEL LABEL	v0	v1	v2
CONVERSION GAIN (μVrms/e)	112.07	108.39	95.63
PIXEL NOISE(μVrms)	98.05	93.59	62.61

TABLE 2: PIXEL NOISE MEASUREMENTS FROM ULN TEST CHIP

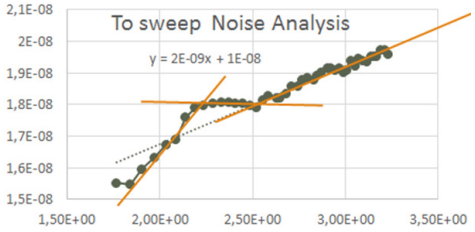
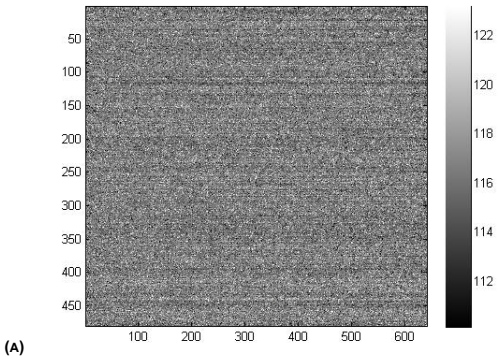


FIGURE 6: ILLUSTRATING NOISE LEVEL VARIATIONS WITH CHANGING T_o.



(A)

(B)

FIGURE 7: (A) TEMPORAL NOISE MEASUREMENTS FROM LONIS CG=1.23DN14BITS/E (VFS=1.5V; CG(UV/E)=112.6UV/E). TEMPORAL NOISE=1.69E-
(B) ILLUSTRATIVE LONIS CATURE.

IV. RESULTS

Mismatch is a prevalent problem of two-stage ADCs which is addressed through embedded self-adaptive error correction [3]. It results into artefacts-free images as Fig.7 illustrates. Fig.8 shows some representative plots regarding the impact of design parameters for the S&H-free readout channel. These plots highlight that 0.5erms can be reached by configuring the ADC for 16-bit and using external multi-sampling. It is worth mentioning that the low-noise behavior is achieved with rather low energy consumption amounting up to 0.24pJ/LSB per channel.

V. ACKNOWLEDGMENTS

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VI. REFERENCES

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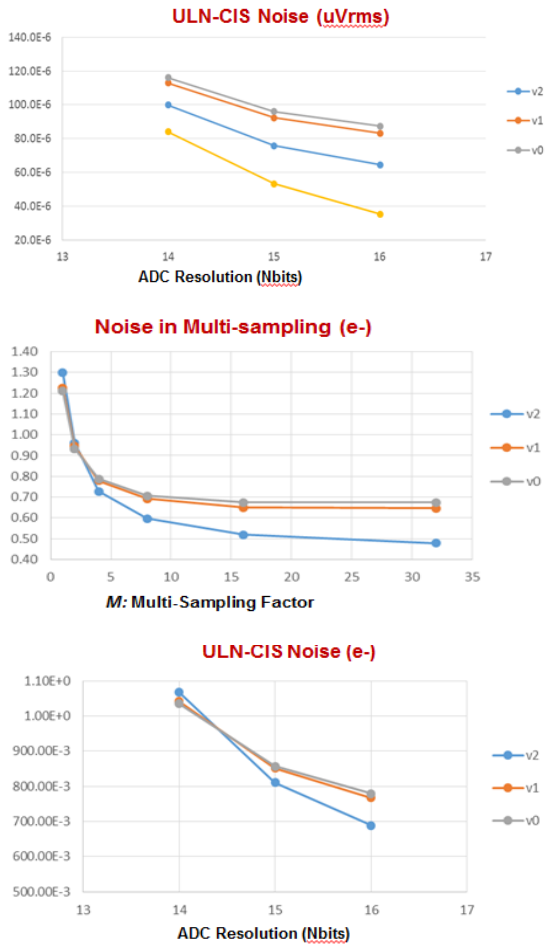

FIGURE 8: IMPACT OF DESIGN PARAMETERS ON THE ULTRA LOW-NOISE CIS.