A 12-bit Column-Parallel Flash TDC-Interpolated Ramp ADC with Online Digital Delay Element Correction

Deyan Levski[1]*, Martin Wäny[2], Bhaskar Choubey[1]

Abstract
This work presents a hybrid column-parallel TDC-interpolated Single-Slope ADC which uses a digital feedback to solve the delay element and clock period matching problem in Flash TDC-Interpolation of SS ADCs. The presented feedback correction scheme is applied in-column and occurs online after the end of each conversion, occupying less than 5% of the ramp time at 12-bits. The concept of the architecture is proven on a 1024 ×128 linescan testchip manufactured in a 0.13 µm 1P3M CMOS process, achieving 1 µs ramp time for a 12-bit linear A/D conversion.

[1] *Department of Engineering Science, University of Oxford, OX1 3PJ, Oxford, United Kingdom*
[2] *Austria Microsystems AG, Madeira Tecnopolo, 9020-105, Funchal, Portugal*
***Corresponding author**: deyan.levski@eng.ox.ac.uk

1. Introduction

The 2^N big-O limiting behavior of Single-Slope (SS) ADCs has led to the exploration of various search space optimization techniques reducing conversion time, while keeping the simplicity and process scalability properties of SS ADCs. A way to increase conversion rate is to perform a coarse quantization in conjunction with a quantization error measurement using a second stage quantizer. This work presents a hybrid column-parallel ADC scheme employing a coarse-fine SS architecture from the Nutt-interpolation family [1].

2. Proposed Flash TDC-Interpolation with Digital Delay Element Correction

The concept of Flash TDC interpolation is presented on Fig. 1. A count clock incrementing an SS ADC counter is fed through a chain of delay elements, providing an N number of clock taps, phase shifted by time τ. During an A/D comparator toggle event the state of the main and delayed clocks are latched. Each additional clock tap adds one quantization step whose value, after thermometer to binary code conversion, is directly concatenated as an LSB word to the MSB word of the main binary SS counter. Direct word concatenation in TDC-interpolated SS ADCs can be successful only if both the SS counter and interpolating TDC yield a radix-2 output word. Thus, for the general case of a Flash TDC interpolating a DDR SS counter, the total sum of the delay line must equal 1/2 the clock period T. In order to maintain DNL of <0.5 LSB, the delayed clocks must be designed such that the cumulative deviation of the sum of all delays is less than $\pm$ ½ τ_{dly}, as well as their matching in-between. The design of fixed analog delay elements, which maintain stable delay time within PVT corners is challenging, if not impossible, without the use of some form of referenced feedback, which is the case of the previously presented DLL-based scheme in [2]. The current work uses a digital feedback and solves the delay element and clock period matching problem by employing TDC code redundancy with a follow-up TDC code retraction back to radix-2, owing to an online in-column calibration operation. Fig. 2 shows a high-level overview of the proposed scheme, which, to achieve a target goal

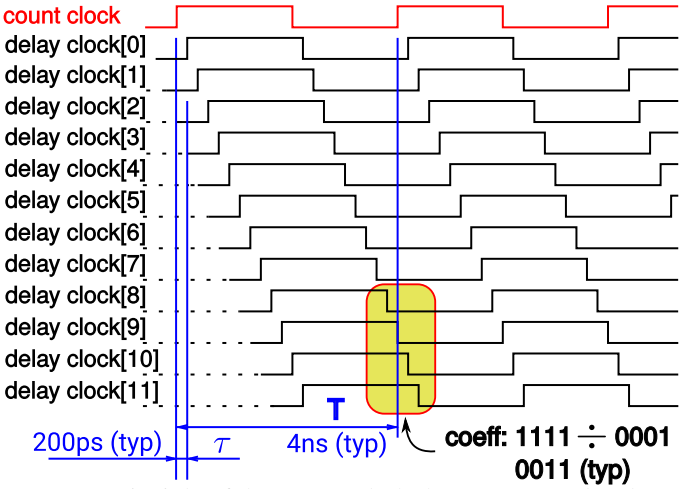


Figure 1. Principle of the proposed Flash TDC-Interpolated SS ADC

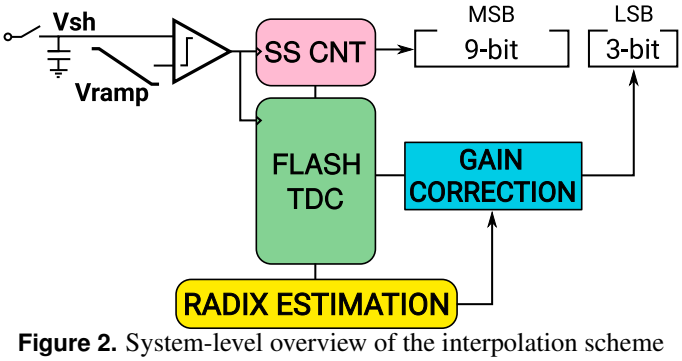


Figure 2. System-level overview of the interpolation scheme

of 1 µs conversion time at 12-bits, uses a 3-bit TDC interpoating a 9-bit DDR SS counter at 250 MHz. The interpolating TDC is formed by eight primary clock phases plus four additional clocks which introduce the redundancy and lower the TDC radix varying from 1.45 to 1.8. The delays are designed such that under all PVT corners yield an overlap with the main count clock edge within the limits of "1111" - "0001", as shown on Fig. 1, with a typical targeted overlap value of "0011" (radix 1.55), so as to maximize the room for delay drift with PVT corners in both directions.

Radix Estimation and Correction

A measurement of the overlapping phases with the main clock, as sketched on Fig. 1, provides a correction coefficient feedback, determining the intrinsic TDC gain and allowing the correction of its radix to 2 using a scaling multiplication operation. Following the overlap, we derive four scaling coefficients:

$$c = f(s)\begin{cases} {}^{8}/_{9} = 0.89, & s = \text{"1111"} \\ {}^{8}/_{10} = 0.80, & s = \text{"0111"} \\ {}^{8}/_{11} = 0.72, & s = \text{"0011"} \\ {}^{8}/_{12} = 0.67, & s = \text{"0001"} \end{cases} \quad (1)$$

where c is the multiplication coefficient and s is the latched coefficient value. The multiplication coefficients are derived by the normalization of all 12 possible quantization levels in the range between the rise and fall edges of the main clock, with the four redundant quantization levels. Fig. 3 shows a binary map of

CORRECTION COEFFICIENT: "0011" / RADIX: 1.55

CK	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
J0	0	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0
J1	0	0	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0
J2	0	0	0	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0
J3	0	0	0	0	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
J4	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0
J5	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0
J6	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0
J7	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	0	0	0	0
J8	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	0	0	0
J9	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	0	0
T	0	1	2	3	4	5	6	7	8	9	10	0	1	2	3	4	5	6	7	8	9	10
C	0	1	1	2	3	4	4	5	6	7	7	0	1	1	2	3	4	4	5	6	7	7
S	0	0	1	1	1	1	2	2	2	2	3	0	0	1	1	1	1	2	2	2	2	3

Figure 3. Binary map of the valid quantization levels with delay overlap of 0011 (typical PVT case)

the quantization combinations for the typical overlap coefficient scenario of "0011". Each column represents a single discrete state in time, rows *CK* and *J*0 to *J*9 show the latch states of the information retaining clock phases (phases J10– J12 in the case of coefficient "0011" are discarded as they go beyond 1/2 Tclk). Row T shows the sum DN of the raw (uncorrected) TDC signal, C presents the ideal signal value after correction, obtained by applying the coefficients in Eqn. 1, and S shows the difference between T and C. As floating point multiplication operations are generally unsuitable for column-parallel implementations, a primitive signal-dependent fixed-point subtraction is implemented. Following Fig. 3 it can be observed that S (the signal-dependent subtraction) increases with the increase of T (the raw TDC DN count), thus representing the subtraction count needed for correcting each signal value, which is equivalent to a fixed-point multiplication operation.

3. Implementation

To test the proposed architecture a 1024 column × 128 line lines-can image sensor was designed, providing a realistic enough test scenario for power routing voltage drop sensitivity of the in-group clock delay elements and TDC latches.

System-Level Design of the Proposed Hybrid ADC

Fig. 4 shows a principle schematic diagram of the hybrid ADC core, shown is 1 out of 8 groups. Each ADC group contains individual TDC control blocks: clock delay line, a global correction coefficient memory and an error correction block. Every column contains 11 TDC latches which are differentially driven by the clock delay line and are differentially gated by the comparator. All TDC latches share a vertical bitline through individual switches, which is used for latch data readout after the end of the ADC ramp phase. Through the *bitline*, the value of the TDC register is scanned and converted sequentially from thermometer to binary code by incrementing a 3-bit LSB counter. The TDC gain correction occurs during the TDC latch scanning process by correction-coefficient-driven control of the opening of the SW0-SW10 switches, sequenced by the error correction module. As the TDC interpolates a DDR SS counter, depending on the LSB value of the MSB SS counter, the counted states in the TDC latch should be high (ones) if the MSB counter LSB value has stopped high, or low (zeros) if the MSB counter LSB has a low state. It is easy to convey the reason for state inversion by looking at the first row *CK* (the LSB state of the MSB counter) in the binary maps on Fig. 3. When *CK* is low (zero) the TDC latch states *J*0-*J*10 are inverted. To achieve the former operation, the *bitline* signalling, after being sensed, passes through an XOR which is controlled by the LSB of the MSB counter. Performing DCDS of the entire interpolated 12-bit word requires a borrow-out operation ensuring a single count decrement from the MSB counter, only when the

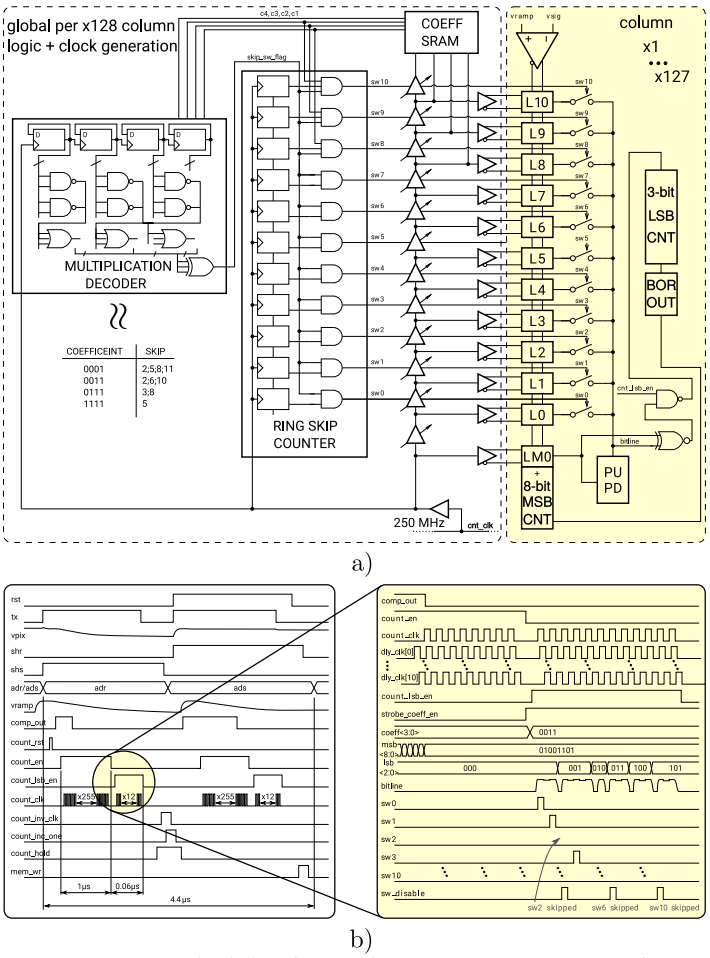


Figure 4. ADC principle of operation: a) one ADC group of x128 columns; b) timing diagram for DCDS operation and calibration sequence

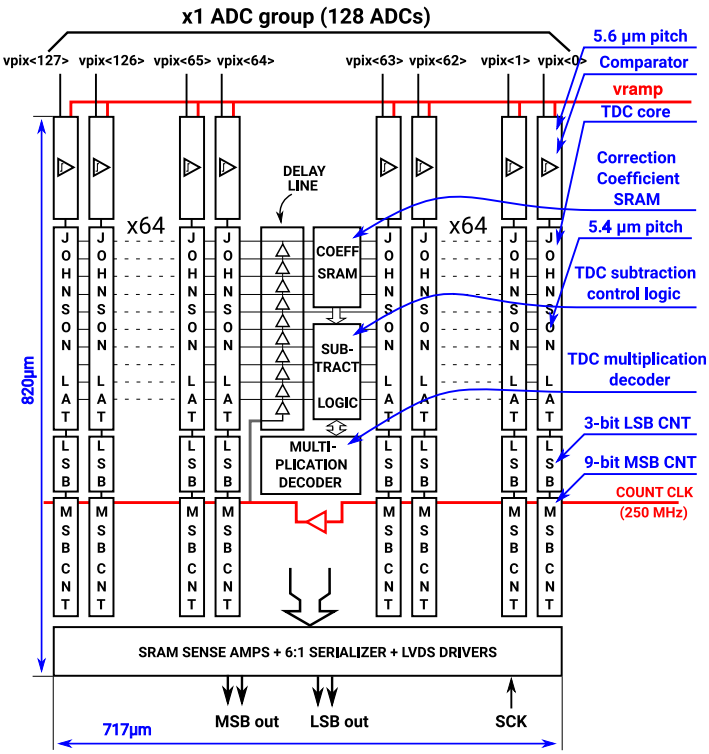


Figure 5. ADC group physical diagram

subtracted TDC words from SHR and SHS sampling result in an underflow. The latter is executed by the BOROUT block, which ensures a borrow out propagation link between the LSB and MSB counters. Fig. 4b displays a simplified timing procedure of a single DCDS conversion. Each column features dual swappable sample and hold capacitors which allows for a fully pipelined mode of operation. During the count period the digital sequencer introduces 255 count clock cycles, while at the same time the ramp reference is slewed. At the time point when the input sample and ramp cross, the comparator toggles, freezing the MSB counter and TDC latch content. When *count_en* is disabled, the conversion operation is finished and the last correction coefficient acquired during the conversion phase is stored into the coefficient storage memory *coeff[3:0]* by the *strobe_coeff_en* signal. After the MSB count phase, the LSB counter is enabled with *count_lsb_en*, while the sequencer issues twelve count clocks on *count_clk* which drive the ring skip counter. The latter addresses each TDC latch consecutively, while skipping latches depending on the state of the *sw_disable* signal, issued by the multiplication decoder and controlled by the stored correction coefficient and algorithm on Fig. 3. To perform DCDS the values of both counters are inverted, followed by a second A/D conversion operation of SHS. Finally the counter state is transferred to a shadow SRAM for readout via per-group 2 × 6:1 serialization blocks and LVDS Tx.

4. ADC Characterization Results

A 1024 column x 128 line testchip was manufactured in 0.13 µm 1P3M CIS process. Table I provides the characterized ADC performance at 1 µs ramp time mode. The latter implies a count clock of 250 MHz, which imposes a typical Flash TDC delay unit time of 200 ps, thus, being ≈ 6× the intrinsic gate propagation delay in the used process. Fig. 6 and 7 show the INL and DNL of a single column (mid-array column 512), although the linearity

Table 1. ADC Performance Results

Parameter	This Work
Process	0.13 µm 1P3M FSI CIS
Array Size	1024 (H) × 128 (V) RGBW
Pixel Pitch / Height	5.6 µm / 820 µm
Resolution	12-bit
Row Time (incl. DCDS)	4.4 µs
Ramp Time	1 µs
Counting Scheme	Flash TDC-Interpolated
ADC Count Clock Frequency	250 MHz
INL	+5.8/-8.2 LSB
DNL	+1.1/-0.4 LSB
Input Range	1.5 – 2.9 V (341 µV/LSB)
Noise Stdev. at 1x gain (LSB)	477 µV (1.48 LSB)
CFPN (at >3000 DN)	≈ 0.15 %
Data Output	16 LVDS ports at 250 Mbps
Power (incl. refs, excl. LVDS)	177 µW/column
Temperature Range	-20 – 70 °C
Power Supply	1.5 V (dig), 3.3 V (ana)

performance is well matched within all columns. The observed DNL glitches occur at the interpolation point between the MSB and LSB counter (every 16th count) which are due to misfortunate design-influenced propagation delay difference in the TDC latch elements (L0– L10) and the DDR latch zero (LM0) of the MSB counter. Partial degradation of the count clock duty cycle by the LVDS clock receiver also contributes to the observed non-linearity peak at the interpolation point codes. The latter should be taken care of and can be easily eliminated with the use of an accurate on-chip PLL and careful latch optimization. The DNL floor below 0.5 LSB is primarily due to the numerical noise introduced by the fixed point multiplication (truncation of numerical residue for radix correction), which is architecture-inherited. The INL measurement is likely to be influenced by the dynamic histogram test measurement setup and finite settling of the S/H circuitry which filter and distort the pure sinewave test signal. Fig. 8 shows the total output ADC noise of a full DCDS conversion at 1x, 2x and 4x gain, which is achieved through ramp slope modulation. The input range of the ADC at 1x gain spans between 1.5 – 2.9 V (1.4 V abs) with an LSB of 341 µV, yielding an input-referred noise of 477 µV RMS at 1x gain. Fig. 8d shows the mean column output with an identical input test voltage to all 1024 columns averaged over 30 K samples. The worst case column fixed pattern noise normalized over full scale (4096) is 0.11-0.15 % which is influenced by a slight inefficiency of the comparator kickback noise compensation scheme affecting the ramp reference line. The latter is generated via a global constant-current discharge of local (per-column) 100 fF MIM capacitors. The calibration coefficient capture is within the designed recoverable range. Group-to-group correction coefficient matching spans between ±1 digital code and does not induce a noticable group-to-group offset. Tests under uniform (DAC-provided) and random (pixel-provided) input voltage confirm that load-induced calibration coefficient drift is insignificant, owing to a strong digital power supply network and locally distributed decoupling. Fig. 9 shows the floorplan of the device, which employs eight individual ADC groups of x128 columns, each possessing dual 6:1 serialization channels and 250 Mbps Sub-LVDS drivers. Fig. 10 and Fig. 11 show images of the top-level chip layout and test board.

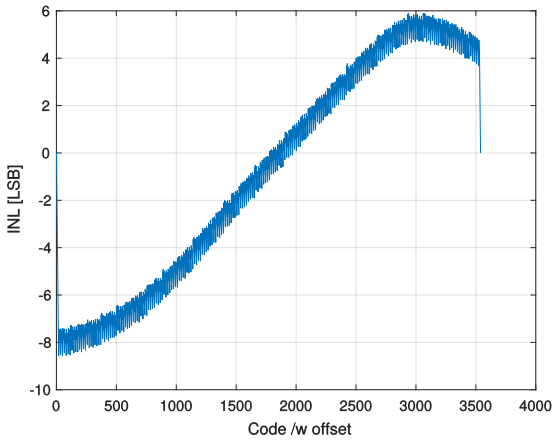


Figure 6. Integral Nonlinearity

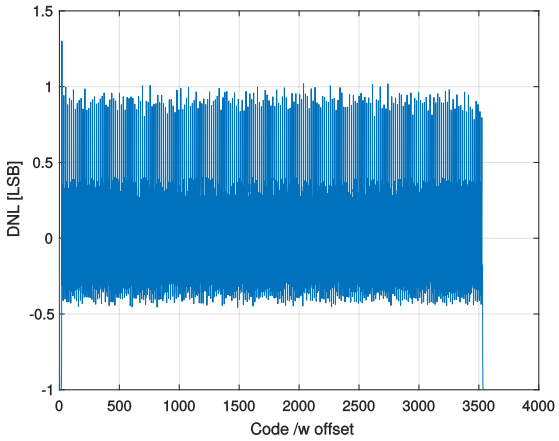
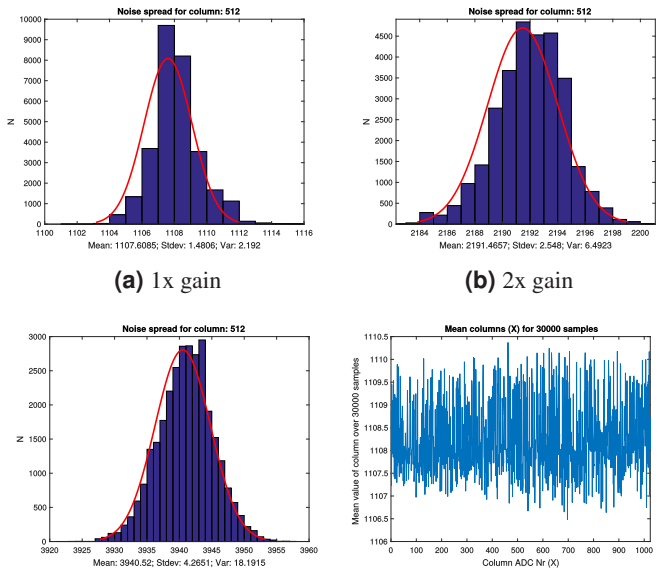


Figure 7. Differential Nonlinearity



(a) 1x gain **(b)** 2x gain

(c) 4x gain **(d)** Mean of Columns (X)

Figure 8. a – c) output noise for a full DCDS conversion (SHR+SHS), hist: 30 K samples; d) mean of columns (X) in DCDS mode

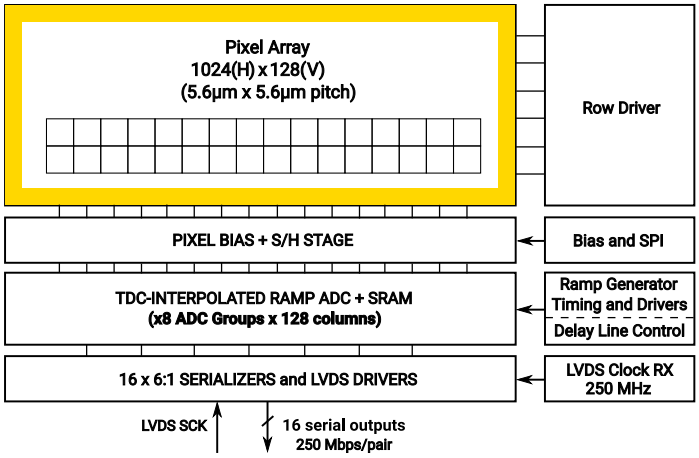


Figure 9. ADC testchip floorplan

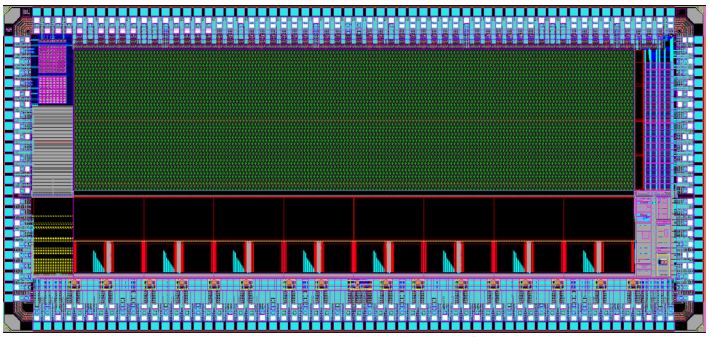


Figure 10. Top-level overview

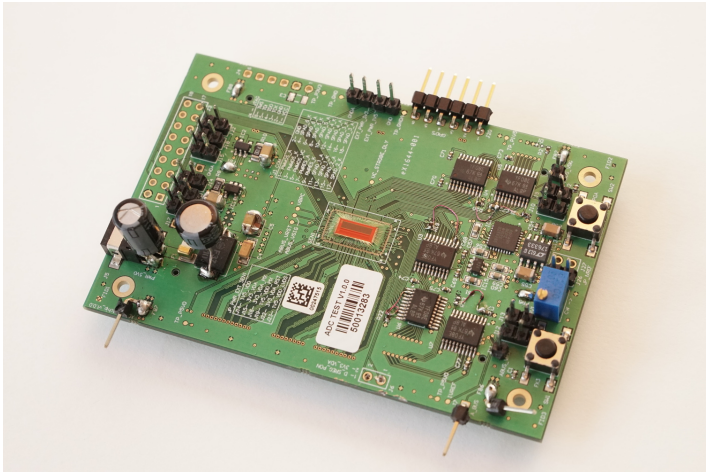


Figure 11. Outlook of the test system

Acknowlegdements

This work was sponsored by the EU FP7 ”Marie Curie” Programme under Grant Nr. 317497. The authors would like to thank R. Sousa for the fruitful discussions on FPGA synthesis, C. Nobrega for the layout of the ramp generator, and P. Aveiro for providing help with the PCB.

References

[1] R. Nutt, “Digital time intervalometer,” *Review of Scientific Instruments*, vol. 39, no. 9, pp. 1342–1345, 1968.

[2] W. Gao, D. Gao, D. Brasse, C. Hu-Guo, and Y. Hu, “Precise multiphase clock generation using low-jitter delay-locked loop techniques for positron emission tomography imaging,” *IEEE Transactions on Nuclear Science*, vol. 57, no. 3, pp. 1063–1070, June 2010.