A SAR-ΔΣ ADC with Dynamic Integrator for Low-Noise CMOS Image Sensors

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ABSTRACT This paper proposes a SAR-ΔΣ ADC with dynamic integrators for low-noise CMOS image sensors. The ADC combines a low power SAR ADC and a low noise ΔΣ ADC. The reference voltage of the ΔΣ ADC is much reduced and the effective quantization noise can be reduced effectively. The multiple sampling can reduce the reference noise and the source follower noise as well as thermal noise. The nonlinearity due to the capacitor mismatch in a SAR ADC can be avoided by the CDS operation with fixed capacitor connection. The integrator is formed by capacitors and dynamic amplifiers in an open-loop architecture. No static current flows from the supply resulting in inherently low energy consumption. A low noise of 17 μV rms is expected up to the conversion frequency of 8 MHz with a Schreier’s FoM of 175 dB.

Keywords: CMOS, image sensor, analog to digital converter, SAR ADC, ΔΣ ADC, low noise, low power, low energy, integrator, dynamic amplifier.

I. Introduction

A single-slope analog to digital converter (SSADC) has been widely used for CMOS image sensors (CIS) [1][2][3]; however, it has two fundamental limitations. One is the conversion frequency limitation of around 500 kHz for 12 bit resolution because of the maximum clock frequency is about 2 or 3 GHz. The other is the noise limitation of about 80μV at the conversion frequency of 100 kHz. Fig.1 shows a conventional comparator circuit for the SSADC.

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\begin{equation}
\frac{V_{n}}{V_{FS}} = \sqrt{16kT/F_{c} + \frac{4kT\gamma}{C_{S}} + \frac{1}{12} \frac{F_{c}}{F_{CLK}} V_{FS}^{2}}
\end{equation}
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where $k$ is the Boltzmann’s constant, $T$ is the absolute temperature, $\gamma$ is the noise constant, $V_{FS}$ is the full scale voltage, $g_{m}$ is the trans-conductance of the input transistor, $V_{L}$ is the logic swing, $C_{L}$ is the load capacitance, $f_{c}$ is the conversion frequency, $f_{CLK}$ is the clock frequency, and $C_{S}$ is the sampling capacitance. The second term, the sampling noise can be neglected if correlated double sampling (CDS) method is used.

![Fig. 1 Comparator circuit for the SSADC.](image)

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The noise voltage of the comparator is derived based on [4] and the sampling noise and the quantization voltage terms are added as

![Fig. 2 Estimated noise voltage and the power dissipation of the SSADC.](image)

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Fig. 2 shows the estimated noise voltage and the power dissipation of the SSAD, where the sampling noise is neglected in the CDS operation. Basically the noise voltage increases with the increase of conversion frequency. Noise voltage of 70 μV is expected at the conversion frequency of 100 kHz. The typical value of the noise voltage of the SSADC is about 100 μV [3]. Therefore high frequency conversion with low noise voltage is quite difficult using the SSADC.

The power dissipation is another issue. The FoMs of the SSADC is about 162 dB without CDS operation [3], however a FoMs of 173 dB has been achieved for this conversion frequency [5][6]. This means the power...
dissipation of the SSADC is about 10 times higher than that of the best ADC for realizing same noise level. A novel ADC architecture is expected for the low noise, high speed, and low power CMOS image sensors.

II. ADC architecture

We propose a novel ADC for CIS combining a successive approximation register ADC (SAR ADC) that is superior in conversion energy and speed [7] and a ΔΣADC that is superior in noise reduction [8]. Fig. 3 shows the architecture of the proposed ADC.

Fig. 4 shows the conversion steps. The input signal is sampled by a capacitive digital to analog converter (CDAC) and converted to the digital value by a 6bit SAR ADC composed by the CDAC and a dynamic comparator. The residue voltage of the CDAC is converted by the incremental 2nd order ΔΣ ADC. The over sampling ratio of 32, 64, and 128 can be set according to the target noise voltage.

The ADC requires only a trigger pulse; the conversion timings for each conversion steps are generated by the gated ring oscillator internally. The reset pulse is also generated internally to reset the ADC. The frequency of the trigger pulse is very low compared with a SSADC that needs a GHz clock. The required trigger pulse is at most 10 or 20 times higher than the horizontal scanning frequency, which relaxes the clock routing and noise issue in a CIS.

Fig. 5 shows the CDS and the conversion range in the SAR-ΔΣ ADC.

The effective quantization noise voltage $V_{qne}$ of the 2nd order incremental ΔΣADC is

$$V_{qne}^2 = \left[ \frac{2V_{FS\_DS}}{m(m+1)} \right]^2$$

where $V_{FS\_DS}$ is a full scale reference voltage of the CDAC and m is the oversampling ratio.

The effective thermal noise $V_{nc}$ is

$$V_{nc}^2 = \frac{4kT}{3mC_s}$$

where $C_s$ is the sampling capacitance.

Therefore the total noise $V_{nt}$ is

$$V_{nt}^2 = V_{qne}^2 + V_{nc}^2 = \left[ \frac{2V_{FS\_DS}}{m(m+1)} \right]^2 + \frac{4kT}{3mC_s}$$

Conventionally, the capacitor mismatch limits the effective resolution of a SAR-ΔΣ ADC. However, we can eliminate this limitation by keeping the same conditions for the CDAC in the reset phase and the sampling phase by using CDS. The quantization voltage for the ΔΣ ADC is only 30 mV with overlap voltage ranges.

The input signal is oversampled to reduce the noise in the ΔΣ ADC and the residue voltage is generated by the CDAC using converted data without additional SAR conversion steps, as shown in Fig. 6. In this figure, $\alpha$ means the capacitor ratio between capacitors connecting to the reference voltage and ground. Oversampling can also reduce the source follower noise in the pixel and reference voltage noise by the averaging operation.

The charge in the sampling capacitor is not wasted but reserved and the sampled voltage is recovered. This can relax the drivability of the source follower in the pixel.

Fig. 6 Signal sampling and residue generation in the ΔΣ ADC.

The expected total noise voltage is very small such as 17 μV.
when \( m \) is 64 and 7.5 \( \mu V \) when \( m \) is 128, even though small capacitance of only 1 \( pF \) is used.

During phase 1, \( S_1 \) and \( S_3 \) are turned on while \( S_2 \) and \( S_4 \) are turned off. During phase 2, \( S_1 \) and \( S_3 \) are turned off. The output voltage of the integrator \( V_{\text{out}} \) can then be expressed as \( (1 + A_2)\frac{V_{\text{out,n-1}}}{3} + A_1V_{\text{in}} \). For the case of \( A_1=3 \) and \( A_2=2 \), \( V_{\text{out}} = \frac{V_{\text{out,n-1}}}{3} + V_{\text{in}} \) which is the same as the conventional perfect integrator.

### III. The open-loop integrator with dynamic amplifier

The integrator of the \( \Delta \Sigma \)ADC is conventionally composed with an OpAmp in a feedback loop, which results in slow response and static power consumption. To address this issue, we propose the novel open-loop dynamic integrator using a passive integrator and a dynamic amplifier [6] to increase the speed without any static current, as shown in Fig. 8 and 9.

\[
V_{\text{out}}[n] = V_{\text{out}}[n-1] + V_{\text{in}}
\]

#### Fig. 8 Open-loop dynamic integrator.

\[
\begin{align*}
\text{Phase 1:} & \quad V_{\text{out}} = (1 + A_2)\frac{V_{\text{out,n-1}}}{3} + A_1V_{\text{in}} \\
\text{Phase 2:} & \quad V_{\text{out}} = \frac{V_{\text{out,n-1}}}{3} + V_{\text{in}}
\end{align*}
\]

The proposed integrator in Fig. 8 consists of three capacitors, four switches \( S_1-S_4 \), and two amplifiers \( A_1 \) and \( A_2 \). During phase \( \phi_1 \), \( S_1 \) and \( S_3 \) are turned on while \( S_2 \) and \( S_4 \) are turned off. During phase \( \phi_2 \), \( S_1 \) and \( S_3 \) are turned off. The output voltage of the integrator \( V_{\text{out}} \) can then be expressed as \( (1 + A_2)\frac{V_{\text{out,n-1}}}{3} + A_1V_{\text{in}} \). For the case of \( A_1=3 \) and \( A_2=2 \), \( V_{\text{out}} = \frac{V_{\text{out,n-1}}}{3} + V_{\text{in}} \) which is the same as the conventional perfect integrator.

### IV. Experimental results

Fig. 10 shows the layout of the prototype ADC designed in 65nm CMOS. The size is 20 \( \mu m \) x 770 \( \mu m \). The decimation filter is not embedded for this prototype.

The estimated noise voltages, dynamic range, maximum conversion frequency, and conversion energy with LPE simulation are 58 \( \mu V \), 17 \( \mu V \), 7.5 \( \mu V \), 85 dB, 95 dB, 102 dB, 16 MHz, 8 MHz, 4 MHz, 300 pJ, 600 pJ, and 1200 pJ for the oversampling ratio of 32, 64, and 128. Fig. 11 shows the estimated noise voltage and power dissipation of the proposed ADC as a function of the conversion frequency. The noise voltage is very small (7.5 \( \mu V \) to 58 \( \mu V \)) and remains constant up to the maximum conversion frequency, which is between 4 MHz to 16 MHz. The power dissipation is proportional to the conversion frequency.

The Schreier’s FoMs is high enough (168 dB to 179 dB) for the conversion frequency of 16 MHz to 4 MHz. Therefore, low noise, low power, and high speed ADC for CIS is expected.
Fig. 11 Estimated performances in LPE simulation.

Table 1 Summary of the estimated performance.

<table>
<thead>
<tr>
<th>Architecture</th>
<th>SAR+ ΔΣ</th>
</tr>
</thead>
<tbody>
<tr>
<td>Technology [nm]</td>
<td>65</td>
</tr>
<tr>
<td>Area [μm x μm]</td>
<td>20 x 770</td>
</tr>
<tr>
<td>Supply voltage [V]</td>
<td>1.0</td>
</tr>
<tr>
<td>Full scale Voltage [V]</td>
<td>1.0</td>
</tr>
<tr>
<td>Over sampling ratio, m</td>
<td>32 64 128</td>
</tr>
<tr>
<td>Max. conv. freq. fcm [MHz]</td>
<td>16 8 4</td>
</tr>
<tr>
<td>Noise voltage, Vn [μV, rms]</td>
<td>58 17 7.5</td>
</tr>
<tr>
<td>Dynamic range, DR [dB]</td>
<td>85 95 102</td>
</tr>
<tr>
<td>Conversion energy, Ec [pJ]</td>
<td>300 600 1200</td>
</tr>
<tr>
<td>FoMs [dB]</td>
<td>168 175 179</td>
</tr>
</tbody>
</table>

FoM_s = DR − 9 − 10\log(2Ec)

Table 1 summarizes the estimated performance.

V. Conclusion

This paper proposes a SAR-ΔΣADC with dynamic integrators for low-noise CMOS image sensors. A low noise of 17 μV rms, high conversion frequency of 8 MHz, and high Schreier’s FoM of 175 dB are expected.

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References