Single photon counting hybrid pixel detectors with 85 ns dead time, 70 kfps frame rate and TSV option

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Abstract: We present a single photon counting hybrid pixel detector called UFXC32k with 85 ns dead time, 123 e- rms equivalent noise charge, 9 e- offset spread, double threshold setting, tunable gain and a framerate up to 70 kfps. The detector can be used in various applications including imaging, XRD and time-resolved experiments and has an option for building edgeless large area detectors due to TSV option included in the design.

Keywords: X-ray imaging, Time-resolved, XPCS, high count-rate, high frame rate, CdTe, TSV

INTRODUCTION

An advantage of single photon counting (SPC) detectors is very high dynamic range, noiseless imaging (properly set discriminator threshold cuts the noise and counts only the hits) and possibility of counting photons only within a given energy window. Recent years show increased effort in development of smaller pixel-sized detectors capable of working with higher fluxes of photons what is possible utilizing new technologies but also a 3D CMOS technology [1-6].

UFXC32k Hybrid Pixel Detector Readout

We present the SPC hybrid pixel detector readout ASIC named UFXC32k (Ultra-Fast X ray Chip with 32 thousands channels) [7], which can be connected to Si sensor (low energy X-ray applications) or CdTe detector (medical applications). The core of the UFXC32k chip is a matrix of 256×128 pixels with 75 μm pitch (fig. 1). Each square-shaped pixel size is 75 μm and consists of a charge amplifier with selectable gain and a Krummenacher feedback circuit for leakage current compensation, a shaper with tunable gain and a multilevel offset compensation circuits placed before two independent discriminators. Digital part of the pixel consists of two 14-bit counters with serial readout.

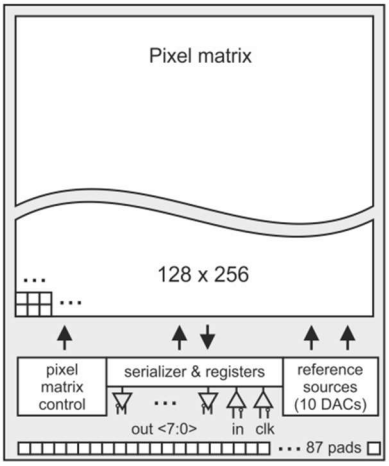

Fig. 1 UFXC32k – simplified block diagram

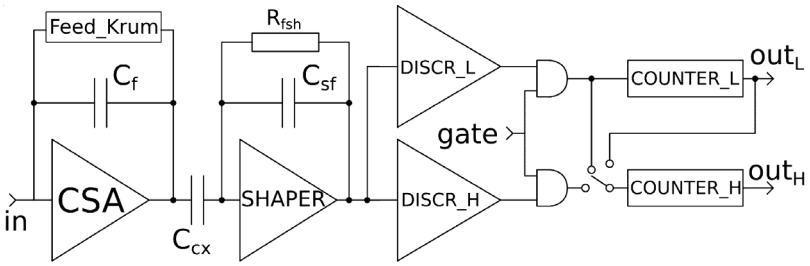

Fig. 2. UFXC32k chip - simplified scheme of a single pixel.

Main parameters (tab. 1) of the analog front-end are: the noise level of 123 el. rms, offset spread 8.5 el. rms, and dead-time (paralyzable counter model) of only 85 ns [3].

TABLE I
Main parameters of UFXC32k chip

Parameter	**Value**
Process	130 nm
Chip area [mm^2]	9.6 ×20.1
Pixel matrix	128×256
Pixel size [μm^2]	75×75
Power/pix. [µW]	26
Input pulses	holes or electrons
Offset spread [e^- rms rms]	8.5
Gain spread [std/mean %]	1.9
ENC [e^- rms] (for dead time [ns])	123 / 163 / 235 (232) / (101) / (85)
Double threshold	Yes
Counters per pixel	2 ×14-bit
TSV option	Yes
Frame rate max [kHz] (readout bits)	70 (2-bit)

Applications

The UFXC32k large size allows to use it in various applications. As the readout circuit has the possibility to operate with both positive and negative input pulses it can work with standard silicon detectors but also with CdTe detectors. Direct comparison of both Si and CdTe detectors was done in the same measuring conditions with 17.4 keV photons and is presented in fig. 3.

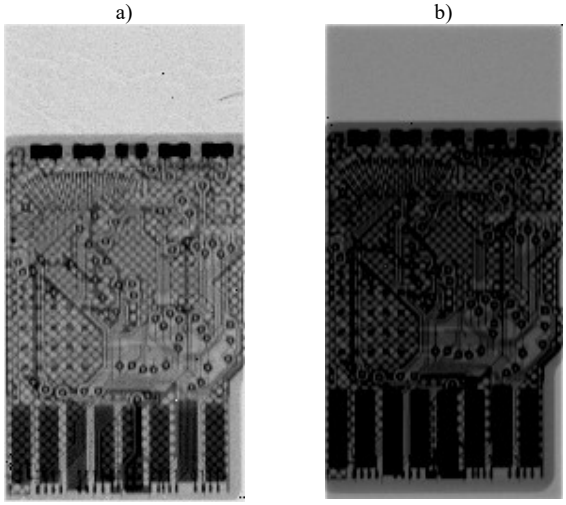

Fig. 3. Examples of the micro SD card raw X-ray radiograms taken with X-rays of energy 17.4 keV and a single UFXC32k chip bump-bonded a) CdTe detector (750 µm thick) – electron collection, b) Si detector (320 µm thick) – holes collection.

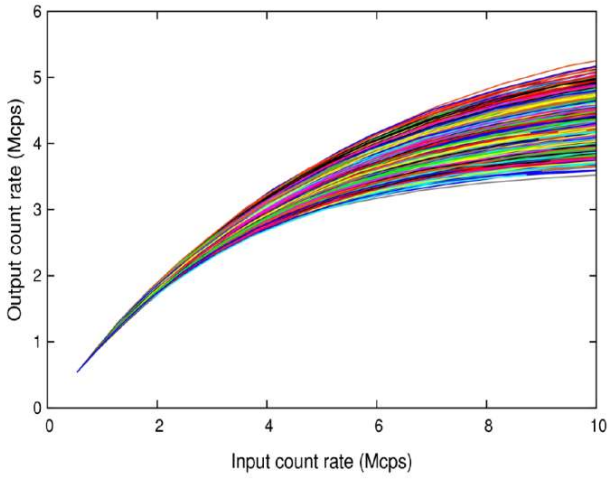

Fig. 4. High count-rate performance of UFXC32k chip. The plots present the results for about 1200 pixels – the measured mean dead-time per single pixel is only 85 ns.

The higher efficiency of CdTe is clearly visible but also the quality of an image is good enough for digital imaging applications with high energy-photons. Furthermore a short dead time (Fig. 4) of the front-end allows for high flux of input photons for even more efficient imagining.

Different modes of operation of the single pixel are possible: standard 2-threshold counting mode (with energy window), a high dynamic range mode, where two 14-bit counters are combined to single 28-bit long counter and a zero dead-time mode, where two counters are connected to single discriminator alternatively (while counter L is read out, counter H is counting incoming pulses and vice-versa). Moreover, in zero dead-time mode there is a possibility of choosing the counter bit length to be 14, 8, 4 or 2 bit long. With 2-bit long counter the detector can operate with the fastest frame-rate dependent on the readout clock. The data are read-out from the chip using 8 LVDS serial outputs clocked with the speed defining detector frame rate. When the serial clock to the chip is 100 MHz, the data is read out with the speed of 11.7 k frames per second (fps), while 305 DDR MHz serial clock allows 70 kfps without any data compression. This mode was tested for time-resolved studies at Advanced Photon Source Synchrotron in Argonne. The preliminary results (fig. 5) prove the stated frame-rate is adequate and therefore it is more than twice faster than current world record of 22 kfps.

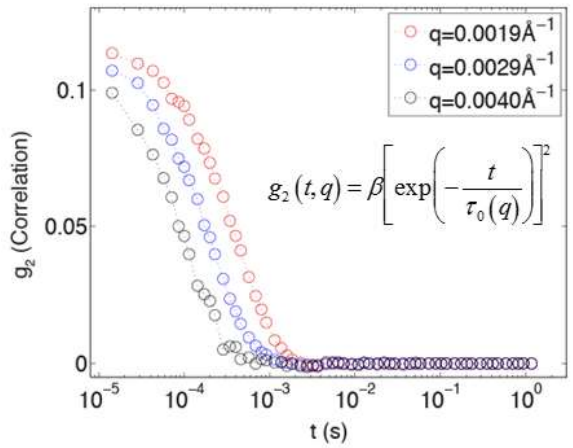

Fig. 5. Intensity decorrelation measured from Brownian motion of 150 nm diameter silica particles dispersed in water (β is the contrast of the measurement) – data were taken at at Advanced Photon Source at Argonne with UFXC32k chip oparated with 70.000 frames per second

A single-side bootable chip allows for building multi-chip structures. One example can be a two-chip module (Fig. 6) built at our Department, which shows a very good chip uniformity whole over detector area. Therefore, satisfying images, like the ones shown in fig. 7, can be achieved without any software correction.

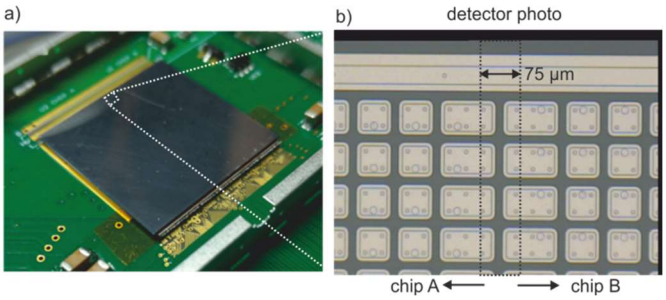

Fig. 6. An example of the 2-chip module sharing the same detector die. a) photo of the wire-bonded module in a camera prototype, b) microphotograph of the area between two chips,

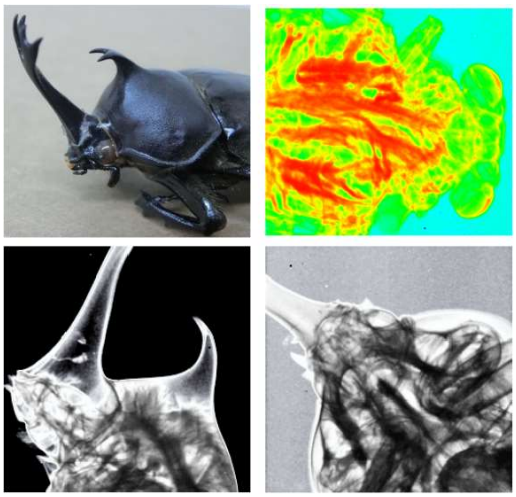

Fig. 7. *Rhinoceros beetle* – photo and radiograms taken with two UFXC32k chips bump-bonded to a Si sensor (320 µm thick).

Construction of a very large area detectors, which are built of multi-chip modules, brings another requirement for readout ASIC design. Usually those large area detectors require minimization of a dead area between the modules which is limited by the technology of the ASIC connection to the PCB. In order to solve this problem, we have implemented a Through Silicon Vias options in our chip. The TSVs aim to minimize the dead area to enable development of 4-side buttable large area detectors (fig. 8). The TSV diameter 20 µm was chosen while

the wafers were thinned to 100 µm. The redistribution layer and the array of pads for solder bumping were placed at the bottom side of the chips. Two UFXC32k chips with TSVs were attached to a single, 320 µm thick silicon sensor and finally, the chip-detector modules were attached to LTCC boards. The 2 × 2 cm^2 plug-in detector modules were successfully built and tested (fig. 9).

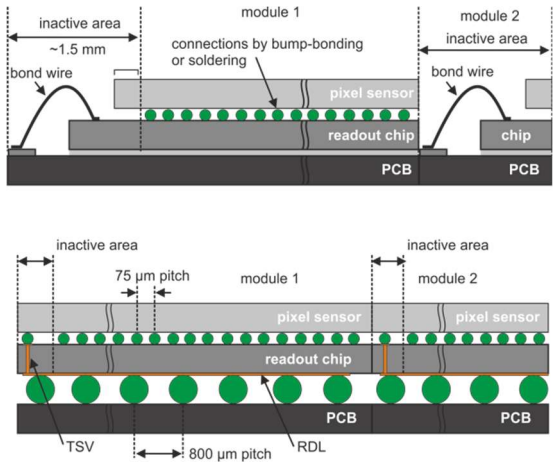

Fig. 8. Applying TSV allows reducing the dead area in multi-chip detector module. Pictures are not to scale.

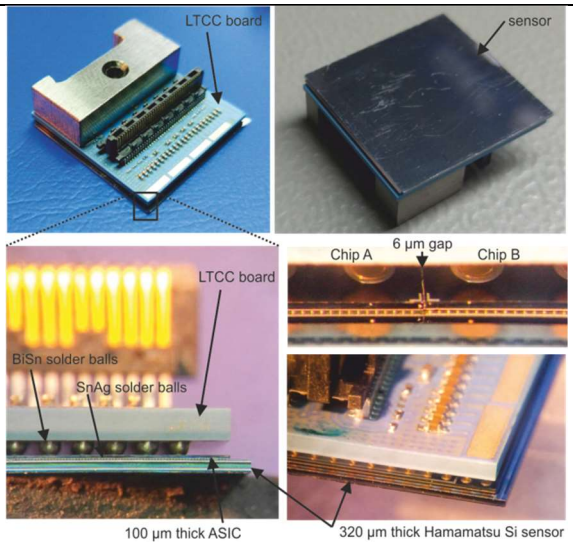

Fig. 9. Fully assembled 2 cm × 2 cm detector module with Silicon sensor and LTCC printed circuit.

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