A 98dB Linear Dynamic Range, High Speed CMOS Image Sensor

Tomas Geurts, Bart Cremers, Manuel Innocent, Wiet Vroom, Cedric Esquenet, Thomas Cools, John Compiet, Burak Okcan, Genis Chapinal, Carl Luypaert, Nicolas Bresson[*], Peter Deruytere[*], Patrick Pintens, Roel Aerts

ON Semiconductor, Schaliënhoevedreef 20B, 2800 Mechelen, Belgium.
tomas.geurts@onsemi.com

This paper discusses a high speed image sensor, manufactured in a 180nm CMOS process. The sensor has a unique combination of large format, a 2560x2560 array of 6um pixels, high-speed read-out, and a linear single exposure dynamic range of 98dB. The dual gain pixel operates in overflow mode achieving a noise floor of 4.75e- over a 375ke- full-well charge. The sensor's native frame rate is 600fps, enabling a 300fps HDR mode. The read-out architecture is an evolution of [1], where the column parallel 14-bit delta-sigma A/D converters were optimized for lower power and structured noise. The row temporal noise is as low as 3% of the noise floor without using any reference pixels. Special care was taken to minimize any scene dependent power consumption so as to avoid any horizontal banding and other related artefacts.

Recently, more effort has been spent extending the dynamic range of CMOS imagers even though initial concepts were already proposed in the early days of CMOS imaging [2,3]. A detailed review of HDR techniques is outside the scope of this paper, but several overviews can be found in literature [4, 5, 7]. Typically, without special measures, dynamic range is limited to ~72dB in most commercial sensors. The most common HDR implementation, using multiple exposures [6], is not suitable for many applications due to the large SNR drop at the transition of exposure ranges and the introduction of motion artefacts. Multiple photodiode techniques [7, 8] are prone to signal dependent optical crosstalk, and a similar SNR drop issue. High speed, large format imagers [1, 9], on the other hand do not offer HDR capability.

The sensor block diagram is shown in Figure 1. For HDR readout, each of the column parallel 3rd order delta sigma A/D converters, which were optimized for noise-speed trade-offs converts 2 signal and 2 reset values for each pixel. The optimized power supply management for the pixel array and analog signal path ensures ultra-low row noise (3% of the noise floor). With a pixel read-out scheme which doesn't rely on a current source, minimizing power consumption of the array, any row noise contributions from the pixel current source were effectively eliminated.

The digital filter was optimized for lower power by resorting to parallel processing of the modulator outputs, allowing to run the filter at lower speeds, and as a result at lower power supply. With this technique the power supply for the digital filter could be reduced to 1.4V.

The pixel schematic is shown in Figure 2. In a conventional dual conversion gain (DCG) pixel, the sensor globally selects which conversion gain shall be used for the readout and the full well charge (FWC) will be limited to the charge that can be held within the photodiode. In overflow mode [10], during the integration time, once the photodiode (PD) has saturated, charges will spill over into the Floating Diffusion node (FD) and overflow capacitor Cext.

Figure 3 shows the signal in the PD (blue) and on the overflow capacitor (red) during integration with overflow for both low and high illumination cases. Note that these signals are not the outputs of the pixel reads with the proposed readout method. The low gain read will represent the total charge, which is the sum of the charge collected on floating diffusion in parallel with the extension capacitor and the charge collected in the photo diode. Special care must be taken to ensure overflow occurs before the PD blooms into neighbouring photodiodes, which would cause severe crosstalk and color artefacts.

The fluid diagram in Figure 4 illustrates the proposed operating method for both illumination cases. The typical readout sequence is:

- High Gain Reset
- High Gain Signal (CDS)
- Low Gain Signal
- Low Gain Reset (no CDS)

The proposed readout sequence results in a correlated double sampling (CDS) High Gain read, and a double sampling (no CDS) Low Gain read where the noise is not correlated between the R and the S signal. An alternative is reading the Low Gain Reset at the time of the reset at the start of the integration time. In this case this reset value has to be stored in a frame buffer until the associated signal value is available. This results in a CDS read where the kT/C noise that is sampled on the low gain capacitor is cancelled. However, due to the very low gain, the read-noise dominates over this kT/C noise.

[*] Previously with ON Semiconductor

Therefore, for practical reasons, a DS read is preferred for its easier implementation.
In order to accommodate a high speed readout, the pixel timing had to be slightly modified relative to a conventional timing. The transfer of photodiode charge to FD takes a substantial time which eats into the time available for pixel readout. In order to relax the requirements on the column settling, a pipelining scheme [Figure 5] is proposed where the array is addressed such that the transfer time overlaps with an operation on another row in the array. As a result, additional memory is required in each column, and special care needs to be taken to avoid signals and reset values from different pixels coupling into each other. This is especially intricate given the fact that the read-out of the array does not use a current source [1] and therefore never completely settles. This makes that it is crucial to ensure the same initial conditions and trajectory for each read from the pixel array.

Due to the significant speed, power consumption and large format, several artefacts were encountered. Two of those will be discussed, and the techniques to mitigate these artefacts will be described.

First, an electrically induced type of image lag was observed. Due to the rolling shutter readout, the previous frame signal read overlaps with the line-by-line reset operation signaling the start of integration and providing the reference for the overflow signal. This reset signal is not used for the Low Gain double sampling readout and the DS reset performed after reading the Low Gain signal value does not see the same coupling as its counterpart at the start of integration. Due to column lines and A/D converters coupling to the substrate, the reset at start of integration ends up being dependent on the signals being read at the same time. In order to mitigate this effect, proper referencing of the overflow capacitor and careful timing, is absolutely critical. This timing involves scheduling the reset operation during a ‘quiet’ moment, and a timing sequence that keeps the power consumption on the pixel supply as independent as possible from the signal level. Doing so introduced a ~25-fold improvement in electrical lag [Figure 6]. In a second phase, more substrate shielding was implemented which helped to practically eliminate the lag.

Secondly, due to the very high power consumption required to maintain high quality low noise readout at high speed, both static and dynamic IR drop on-chip, as well as dynamic power supply variations due to finite inductance, led to row banding. Row banding manifests itself as shown in Figure 7. The dark pixels in rows with significant saturated content show either positive or negative deviations from dark pixels in all-dark rows. This effect results from power supplies, bias signals, controls and other references to be slightly different depending on the signal values being processed by the pixel array and readout circuitry.

In order to minimize the impact of power consumption variations in this type of scene, first, the resistance and inductance in the supply path had to be minimized. Conventional image sensor layout techniques, driving control, reference signals and power supplies horizontally routed across the columns will most certainly fail. A segmented layout floorplan with vertical power strapping at regular distance is required. However, due to the stacking of analog, digital and interface circuits, the available routing space for power supplies is limited. Therefore, multiple power supply rails were implemented that each can be bonded to. These bondwires go down to several millimetres into the die as illustrated in Figure 8. In addition to this, in order to optimize the substrate resistance, the sensor was contacted from the backside by applying a conductive coating and adhesive between the sensor and the heatslug in the package.

In order to further mitigate the impact of scene dependent power consumption, low PSRR circuits were implemented, but while these techniques are absolutely necessary and useful, they are not sufficient and substantial attention went into ensuring the readout circuits minimized signal dependent power consumption and loading on other references. This also implied the use of proper clamping throughout the signal chain in order to avoid any circuits turning off all together when processing fully saturated pixels.

In nominal mode, the sensor captures 300 HDR frames per second and achieves a 4.75e- noise floor on the high gain read while the low gain read has a full well charge of 375ke- stored on an in-pixel capacitor. The 98dB dynamic range can be further extended to 101dB when operating at 120fps. After (external) recombination of the two signals, the SNR in the blending region remains above 40 [Figure 9]. Since this sensor uses a single integration time and a single photodiode for the entire dynamic range, it is free of any HDR related motion artefacts or color crosstalk effects. The high speed readout operation further mitigates rolling shutter distortion for most practical viewing applications, making this technology suited for the most demanding applications.

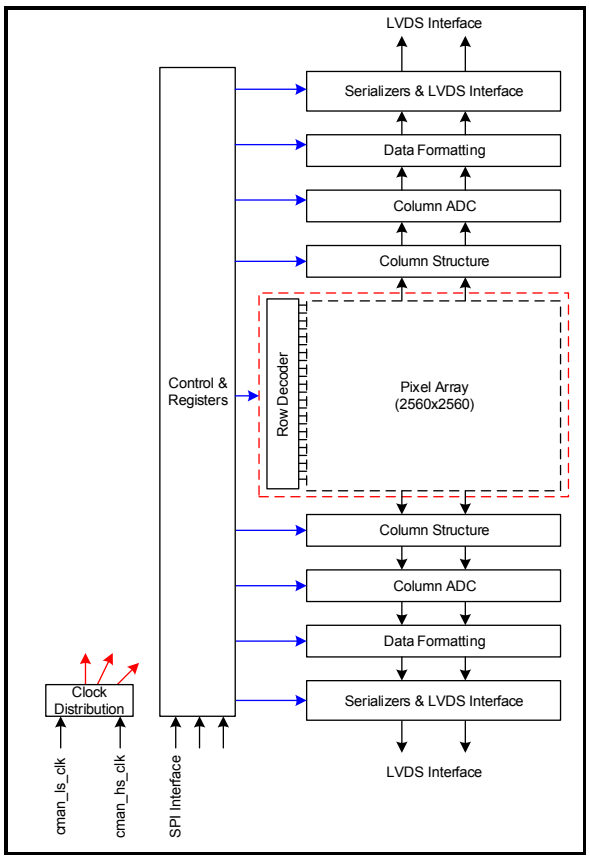

Figure 1: Sensor Block Diagram

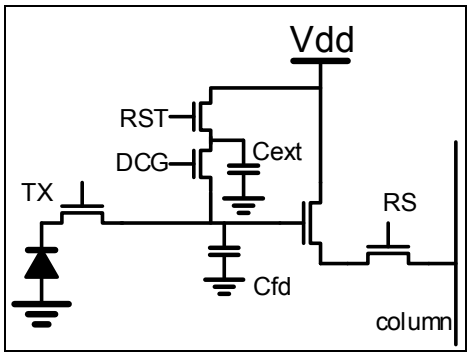

Figure 2: Overflow Pixel Schematic

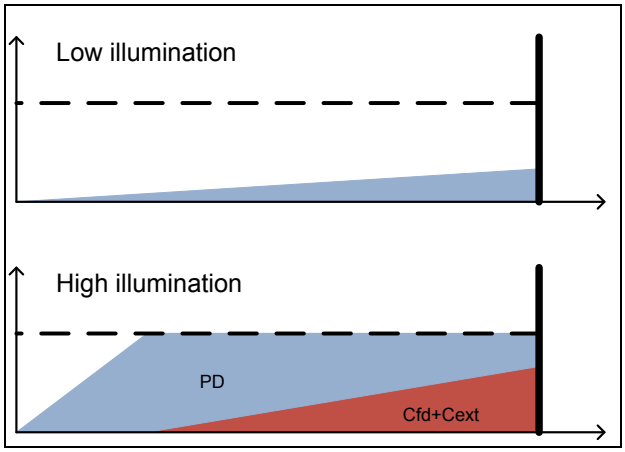

Figure 3: Overflow Principle

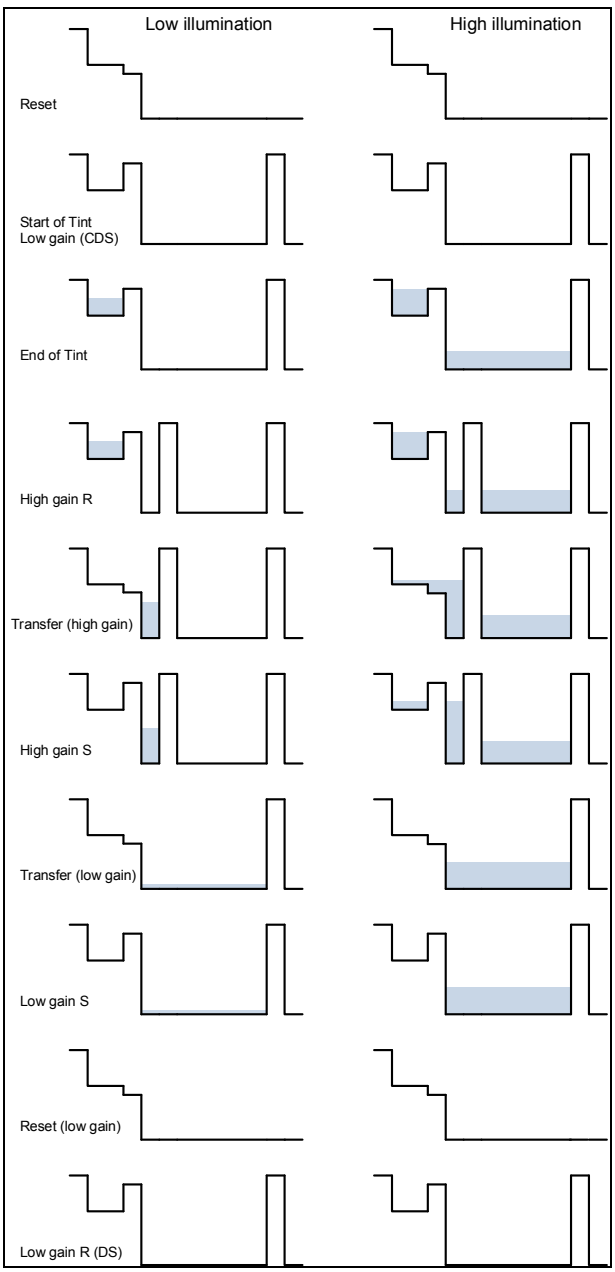

Figure 4: Fluid Diagram

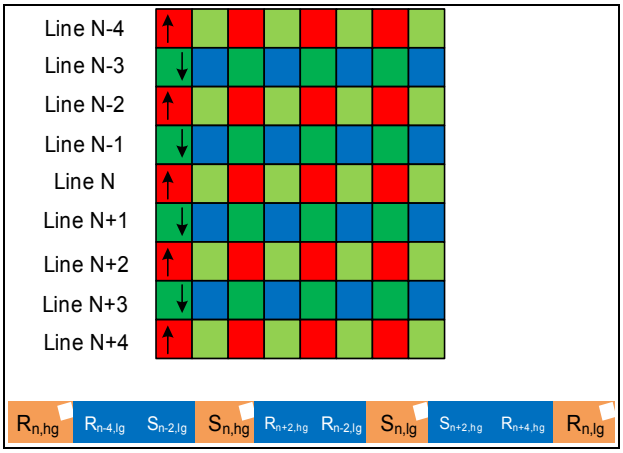

Figure 5: Pipelined Readout

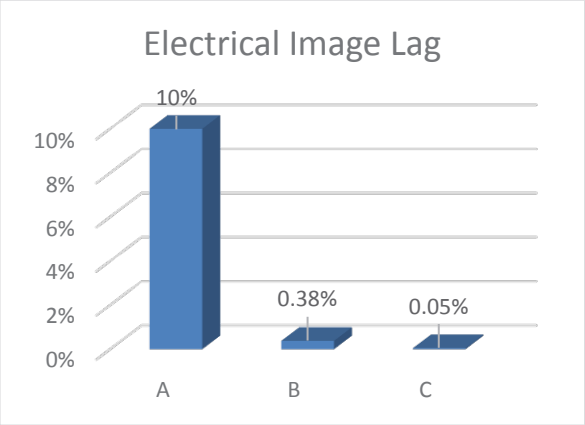

Figure 6: Image Lag Improvement – A: Original, B: Clean reference Cext & Optimized timing, C: Improved substrate shielding

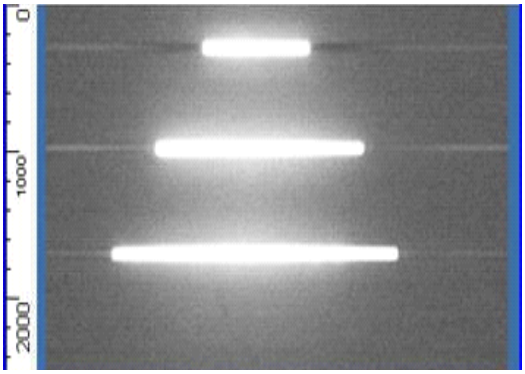

Figure 7: Horizontal Banding: 1000x amplified

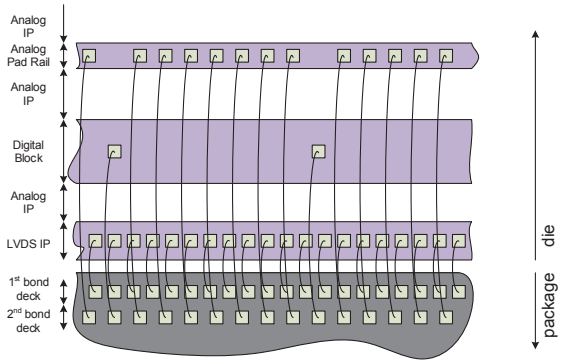

Figure 8: Bonding Scheme

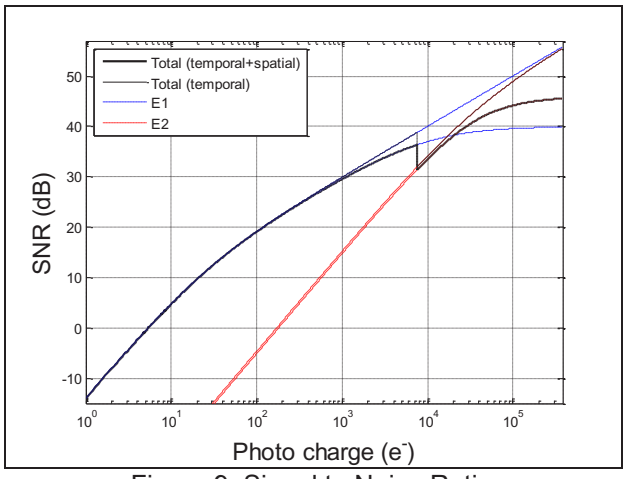

Figure 9: Signal to Noise Ratio

Table 1: key specifications

Parameter	Value	Remark
Pixel size	6 x 6 μm^2	
Pixel array	2560x2560	
Pixel type	5T+1C	
Frame Rate	300fps	
Main power supply	1.4, 1.8 & 3.3 V	
Full well	375 ke$^-$	
Temporal noise	4.75 e-	
QE	>65%	peak
DR	98dB (>100dB)	Intra-scene, single integration time; DR can be increased at lower speed
ADC resolution	14-bit	12-bit ENOB after rescaling
Package	ceramic μPGA	Double bonding decks, integrated TEC

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