A native HDR 115dB 3.2µm BSI pixel using electron and hole collection.

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Abstract
A new pixel architecture providing HDR capability coupled with excellent low-light performance and compatibility with pulsed light sources or fast moving objects is presented. The pixel concept is based on a combination of electron collection via a pinned diode for low signal levels, and hole collection with capacitive storage for higher signal levels. The accumulated electrons and holes are generated by the same incident photons. We demonstrate this concept with a 3.2µm pixel fabricated in a back-side illuminated (BSI) process including capacitive deep trench isolation (CDTI).

Introduction
Several methods of implementing high dynamic range (HDR) capabilities in a CMOS image sensor have been developed thus far. In most cases these rely either on additional devices within the pixel, or on multiple successive integration sequences [1,2]. These solutions generally result in degraded low light sensitivity due to poor fill factor, or image artefacts depending on illumination conditions respectively. The pixel presented in this work aims to address both of these weaknesses.

Hole collection and storage
Electron collection, storage and readout is performed in a similar manner to the standard 4T operations, therefore the focus of this section is the novel hole management functionality.

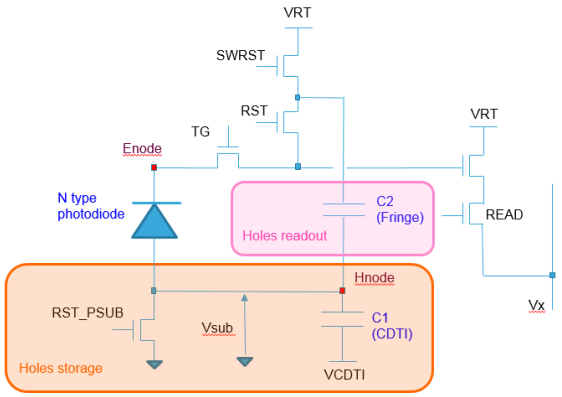

Fig. 1: Pixel schematic

With a typical 4T-style pixel, once an electron-hole pair has been generated by an incident photon, the electron is collected but the hole – which is considered to be redundant – is drained through the substrate contact and lost. To permit hole collection, the substrate of each pixel is electrically isolated with respect to the neighboring ones. This isolation is achieved through the use of deep trenches which penetrate the full silicon depth of the BSI sensor and fully surround the photodiode area. Such deep silicon trenches have already been used to prevent electrical crosstalk in BSI sensors [3]. As shown in figure 1, an NMOS transistor (RST_PSUB) is used to reset the pixel substrate to ground at the beginning of the integration or during the readout phase.

The HDR performance of this pixel architecture is directly linked to the capability to store holes in quantities greatly exceeding the electron full well capacity. The hole full well is a function of the pixel substrate capacitance (C1): a 73 fF capacitance will store 912 kh+ over a 2V swing. This capacitance value is achieved by utilizing the isolation trenches. These are fabricated with an oxide liner and subsequently filled with polysilicon to form capacitive deep trench isolation (CDTI). Negatively-biased CDTI is known to improve dark current metrics compared to oxide-only isolation trenches [4]. A schematic cross section view of such a pixel is presented in figure 2.

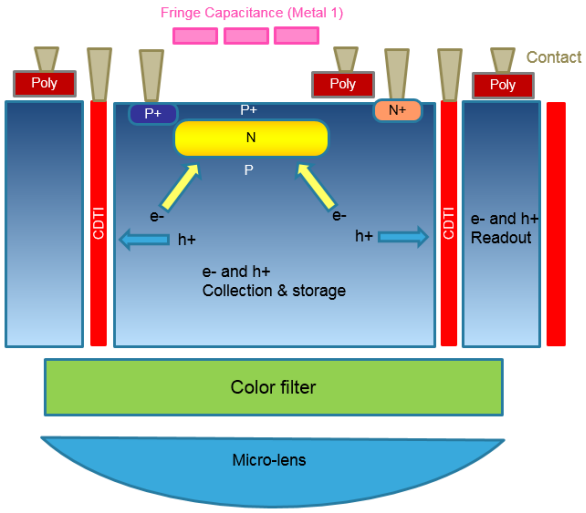

Fig. 2: schematic cross section of the pixel

Hole read out
The hole signal is the voltage reached by the pixel substrate (Vsub). Starting from 0V, and with a potentially large swing, it is not practical to directly measure this with an NMOS transistor, therefore a capacitive-coupling design has been chosen instead. The pixel substrate is connected to the sense node with a dedicated capacitor (C2, Fig. 1).

The hole readout design has multiple benefits: firstly, it efficiently reuses the existing pixel circuitry; the only active device added to the pixel is the RST_PSUB transistor. Secondly, it offers ample flexibility of the capacitance ratio C2/Csn (sense node capacitance) to enable the high voltage swing on Vsub to be converted

to a lower swing acceptable for the read out chain. Finally, it must be noted that although the hole signal is positive, the 3T-like timing with signal sampling preceding the reset sampling produces – like the electron signal readout – a negative voltage swing at the column, hence the same analog to digital conversion (ADC) scheme can be used for both electrons and holes.

As for any 3T readout scheme, the kTC noise must be considered. Given the extremely large hole storage capacitance and the C2/Csn coupling ratio, its contribution is not as dominant as might initially be expected. Indeed, the kTC noise for C1 = 73 fF with a 68% C2/Csn ratio is calculated to be 216 µV – within the expected range of typical source follower noise or 12bit ADC quantization noise.

The pixel schematic is illustrated in figure 1. The pixel includes a nominal N-type photodiode, 6 transistors and 2 built-in capacitances. Transfer gate (TG), reset transistors (RST and SWRST), source follower (SF) and READ transistors enable electron operation with 2 conversion gains (high and low). C1 is the CDTI capacitance used to store holes during integration, C2 is the fringe capacitance coupling the Hnode to the sense node for hole readout. C1 and C2 do not negatively impact the photodiode fill factor: C1 is at the pixel edges and also serves as the pixel isolation; we take advantage of the BSI process in order to implement C2 in the back end layers above the photodiode.

Read out interference considerations

The pixel timing is presented in figure 3. After an initialization period for cleaning the photodiode and the substrate, TG and RST_PSUB are turned off, which enables the start of electron and hole integration. During this integration, the CDTI capacitance C1 is used to store the holes in the substrate while limiting the substrate voltage increase.

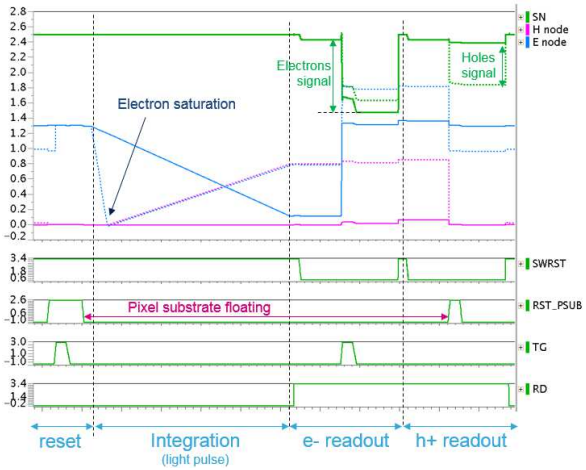

Fig. 3: Pixel timing and simulation
Signal: 30k(Solid line), 400k(Dotted line)

At the end of the integration period, the N photodiode will have collected a number of electrons and the substrate voltage will have increased by up to +Vsub. The readout sequence starts with the readout of the electrons, followed by the readout of the holes. When RST_PSUB is asserted, Hnode is reset to Vss and the voltage variation –Vsub is injected to the sense node voltage through the capacitance C2. For HDR image reconstruction, we combine the electron and hole signal data for each pixel.

Compared to a standard 4T pixel the electron readout slightly differs in that the diode is embedded in a floating pixel substrate and the sense node is coupled to this same floating node (Hnode). For signals significantly above electron full well, Hnode rises towards a high voltage and can potentially impact electron readout. However, in these circumstances the electron data is irrelevant since the pixel information is provided by holes anyway. For low signals, Hnode is always close to 0V, and due to the strong coupling to the CDTI trench, the only likely artefact to be found is a harmless increase of the conversion factor.

While the hole signal has a limited effect on the electron readout, the converse is not true. Electrons in the photodiode can directly impact the hole readout and the decision on which charge carrier to extract first must be carefully considered. Indeed, hole-first timing shows no sensitivity at low signal until the diode reaches its full capacity. The generated holes are stored in the pinned junction embedded capacitance to balance their electron counterpart. Hence Vsub is not rising until the diode becomes full and the additional electrons start to overflow through the transfer gate channel. As a consequence, the image reconstruction is the sum of the hole and the electron signals. This also implies that all the electrons stored in the photodiode are accurately counted which may not be always true, for example, when high conversion gain is used.

Because of the issues highlighted with hole-first readout, we consider electron-first timing as a more robust approach. During the electron readout phase, the photodiode is reset and the hole signal is restored on Hnode. The subsequent hole readout is then fully linear from the first photon. At the other side of the curve this electron-first approach may induce a slight non linearity when Hnode approaches VRT. At some point the pinning voltage of the photodiode will be higher than VRT and the reset will not be completed. For each electron kept in the diode there will be a corresponding hole missing in the readout. This effect will progressively increase at very high signal levels, but it is only expected to reach a maximum of 3 % non-linearity and should therefore not be detrimental to image quality.

Simulated Enode and Hnode behaviors for various illumination conditions are plotted in figure 3.

SNR : measurements vs. theory

In figure 4, the measured SNR (signal to noise ratio) for this native HDR pixel are plotted for a 30 ms exposure. The total dark noise for the hole readout in this condition is 550 h+, with the main contributor being the dark current non uniformity (DSNU, 515 h+). Theoretical SNR curve is computed by removing this DSNU contribution and considering 0.6% PRNU.

With HDR sensors, one of the major image quality criteria is the SNR value when the signal level is in transition between the low-light and high-light regions of operation. This SNR dip is usually dominated by photon shot noise because the amount of charges is substantially lower in the high light image. Here, there is a continuity in amount of charges and the SNR dip is purely the consequence of increased read noise.

At a transition point of e.g. 30 kh+ signal, the theoretical noise breakdown is almost equally shared among shot noise (173 h+), kTC noise (163 h+), combined ADC and source follower noises (135 h+) and ideal 0.6 % PRNU (180 h+). Combining these contributors bring the total noise to 325 h+. This noise corresponds to 39 dB SNR at transition, which is the best performance that can be achieved with this pixel design. The actual SNR dip value measured on our sample at image transition is 32 dB, limited primarily by dark current non uniformity and pixel response non uniformity. Both of these metrics can be improved by process tuning.

Pixel performance

The manufacturing process used for the sensor is a back-side illuminated (BSI) bulk process including capacitive deep trench isolation (CDTI), color filter with Bayer pattern and micro-lens. The pixel pitch is 3.2µm. For this first implementation a 600 x 650 image sensor test chip was produced comprising sub-arrays of different pixel variants (with 65k pixels per variant).

The measured optical performance is presented in table 1. Usable linear full well for electrons is 33 ke- in low CVF mode and usable linear full well for holes reaches 750 kh+. The ratio between the latter and the electron noise floor in high CVF mode yields a dynamic range of 116dB. Clearly, the dark current for holes is the foremost image quality detractor. It is due to junction leakage at the transfer gate drain. No specific process optimizations have been made to contain this leakage on the measured samples. Fine tuning of this drain junction should enable a significant reduction of the dark current.

The measurement of conversion factor for holes is an area of interest here. Using the photonic noise approach, the measured noise is in the low-millivolts region regardless of the signal and could be easily increased by any parasitic noise. As shown in figure 5, this small noise is linearly dependent upon the square root of the signal and the value of 1.33 µV per hole is extracted from the curve.

Figure 6 shows electron and hole signal linearity with either hole-first or electron-first extraction. We see that in the first part of the curve, the electron signal is the same for both modes but starts to diverge after the full well is reached. For the hole signal there is the expected flat response at the beginning for the hole-first mode whereas in the electron-first mode, this artifact is absent, giving a highly-linear response. For the electron-first mode, the full linearity curve with common X and Y axis for electrons and holes is plotted in figure 7 to demonstrate the good overlap and the slope matching for both charge carriers.

The PRNU (Fig. 8) exhibits very good behavior with a value of 0.4% maintained across the majority of the signal range, validating the overall hole capture concept. A degradation of up to 1.5% is visible around the electron full well level and this is attributed to incomplete reset of the photodiode as described previously.

Quantum efficiency has been measured in both modes (Fig. 9). Matching between both measurements over the full spectrum guarantees good HDR image reconstruction.

Perspectives

The pixel presented here can be improved in multiple directions.

First of all, by tuning the process for hole dark current reduction and lower photodiode full well, SNR at transition should be significantly improved. Then, it is expected that with further design and setting optimization 120 dB HDR would be achievable.

Conclusion

A native HDR pixel concept based on concurrent electron and hole collection has been demonstrated. It possesses a full well signal equivalent to 750 ke- with no compromise of sensitivity at low level. It operates with a single integration time, thus providing immunity to flicker or motion artifacts. Finally, the pixel operation is compatible with existing circuit design.

Acknowledgment

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[3] J. Michelot et al., "Back Illuminated Vertically Pinned Photodiode with in Depth Charge Storage," International Image Sensor Worshop, 2011

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Performance	Unit	Value
High Conversion gain electrons	µV/e-	163
Low Conversion gain electrons	µV/e-	29.6
Conversion gain holes	µV/h+	1.33
Usable Full Well electrons	e-	33000
Usable Full Well holes	h+	750000
HF PRNU electrons		0.55%
HF PRNU holes		0.41%
Idark electrons	e-/s	45
Idark holes	h+/s	2300
Noise Floor in High CVF Mode	e-	1.2
Dynamic range	dB	116
Green QE peak		73%

Table 1: Measured optical performance

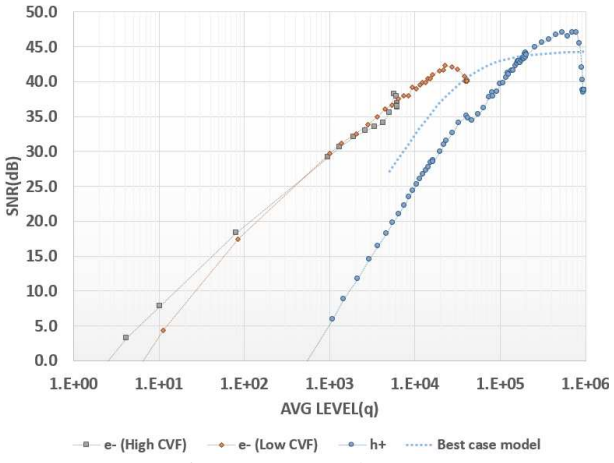

Fig. 4: SNR vs. charge

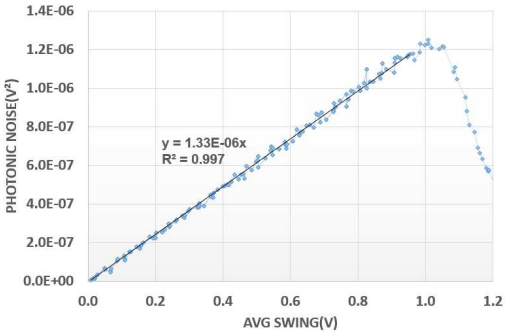

Fig 5: hole photonic noise

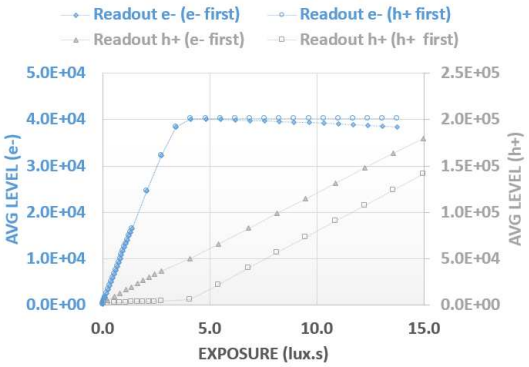

Fig. 6: Linearity vs. readout mode

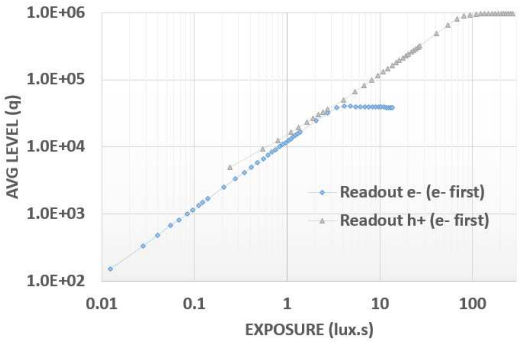

Fig. 7 Linearity vs. exposure

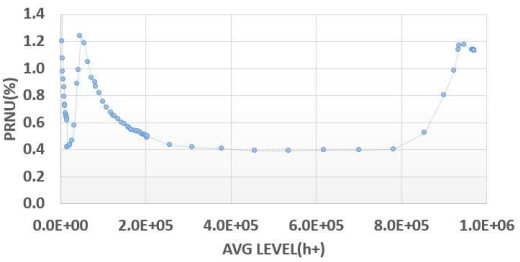

Fig 8: PRNU vs. signal for holes

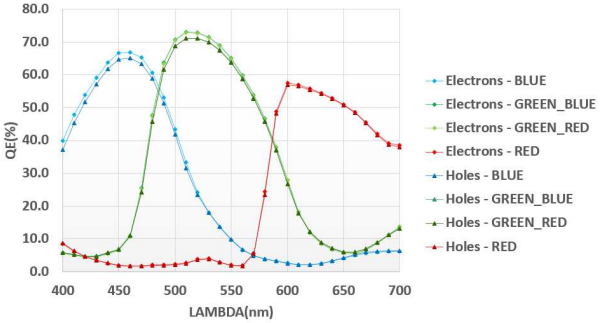

Fig. 9: QE electrons and holes