An 87dB Single Exposure Dynamic Range CMOS Image Sensor with a 3.0μm Triple Conversion Gain Pixel

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Abstract

A 2M pixel single exposure high dynamic range image sensor utilizing a 3.0μm pixel that has 3 kings of conversion gain and a dual-gain single amplifier is presented. With the pixel and the signal chain, intra-scene dynamic range of 87dB has been obtained in a single exposure operation by merging low gain readout signal and high gain readout signal. The image sensor also employs an on-chip linearization function, yielding a 16bit linear signal at 60fps. In this single exposure high dynamic range (SEHDR) approach, no SNR degradation occurs in a whole photo conversion range. Also, it can suppress artifacts from moving objects or time variant of light sources, could appear in the multiple exposure high dynamic range (MEHDR) approach.

1. Introduction

High image quality in low light condition is highly demanded in many applications, such as security, surveillance, automotive, IPC applications, to name a few. To obtain high sensitivity, image sensors are usually operated in a high gain condition, and image quality suffers from low signal saturation due to limited dynamic range. To expand image sensor dynamic range, many approaches have been introduced.

Among them, the multiple exposure high dynamic range (MEHDR) is the most common approach, where images with different exposure times are captured then merged into a high dynamic range image [1]. Line interleave exposure control or pixel interleave exposure control schemes are also included in this category. However, this approach has fundamental issues associated with different exposure timings for a long exposure frame and a short exposure frame, which could generate artifacts with moving objects or time varying light sources like pulsed LEDs. Another issue is SNR degradation at the conjunction point of the two images. To suppress the artifacts from the pulsed LEDs, chopping integration has been introduced [2]. However, the SNR drop at the conjunction point is still an issue.

The second majority approach is that two kinds of pixel, one has lower sensitivity and the other has higher sensitivity, are implemented in a same pixel array, and different sensitivity signals are combined into a linear signal [3]. This approach needs redundant pixels. Also, it needs careful optical design to obtain uniform optical performance of angular dependence, cross-talk and spectral response between the two kinds of pixels.

An ideal solution is to expand pixel saturation while keeping high sensitivity in low light conditions. The lateral overflow integration capacitor (LOFIC) approach is considered as one of solutions, and high dynamic range more than 100dB has been demonstrated in a single exposure [4]. On the other hand, LOFIC needs a charge accumulation node outside the photodiode. Reduction of junction leakage and defect control of the charge accumulation node are challenging issues in terms of fabrication.

Concept of the image sensor presented in this paper is simple. Firstly, PD saturation is increased as high as possible, then intrinsic pixel performance from its noise floor to saturation level is fully utilized in a single exposure. Introducing a triple conversion gain pixel, dual gain preamplifier and on-chip linearization function, signal chain of the image sensor covers from noise floor of $1e^-$ to pixel saturation, and a linear 16bit digital signal is obtained in a single exposure operation. The image sensor is fabricated in a standard BSI CMOS image sensor process without special devices.

2. Pixel configuration and operation sequence

The developed 3.0μm pixel has a vertically two-shared structure as shown in Fig.1. The charge detection node is connected to a vertical binning line through a binning transistor BIN1. The charge detection node is isolated from the vertical binning node by the BIN1 transistor, so that influence of parasitic capacitance of the binning node are removed when high pixel gain is required. Another binning transistor BIN2 acts as a vertical binning switch.

Not only for the binning purpose, the BIN1 and the BIN2 transistors are utilized for pixel gain control. When the BIN1 transistor is turned on during the pixel readout, gate capacitance of the BIN1 transistor and metal capacitance of the vertical binning line serve as an additional capacitance of the charge detection node and thus reduces the pixel gain. Turning on the BIN2, further capacitance is added to the charge detection node. Thus, by controlling the BIN1 and the BIN2 transistors, the pixel is capable of having three different gains without additional devices like poly-insulator-poly (PIP) capacitors or metal -insulator-metal (MIM) capacitors.

The presented sensor can read out a pixel two times with different pixel gains. Fig. 2 shows a pixel operation timing

for the dual pixel gain readout. Firstly, RST, BIN1 and BIN2 are all turned on to initialize voltages at the vertical binning node and the charge detection node. After RST turned off, low pixel gain (LPG) offset signal is sampled as RST SH (Low pixel gain). Next, BIN1 and BIN2 transistors are turned off, and high pixel gain (HPG) offset RST (High pixel gain) is sampled. A first change transfer pulse is applied on the TG, followed by sampling of the HPG signal, SIG SH (High pixel gain). LPG signal is obtained after BIN1 and BIN2 are turned on again and sampled as SIG SH (Low pixel gain). Before the LPG signal readout, second transfer pulse is applied to the TG gate so that remaining charge in the photodiode is transferred to the charge detection node in case of high light conditions.

When the BIN2 transistors are turned off (dotted line in Fig.2) during the signal readout period, the pixel operates in the middle pixel gain (MPG) condition.

3. Sensor architecture

Top architecture of the image sensor is shown in Fig. 3. Odd column pixels and even column pixels have individual TG control as TG1a/TG1b and TG2a/TG2b, so that even and odd column pixels are read out serially in one row time, which allows us to assign one signal chain for two pixel columns.

The column signal chain consists of an amplifier array, a 13bit SAR ADC array and column memory. The column amplifier has two separated signal input paths, which enables two independent CDS operations with different gains. In combination with the multiple gain pixel and the dual-gain column amplifier, flexible control with wide gain ratio is available. For the LPG readout, amplifier gain of either 1x or 2x is chosen, and in the HPG readout, amplifier gains of 1x, 2x, 4x, 8x are selectable.

After A/D conversion, the two sets of signals are fed to an on chip digital processor, yielding a high dynamic range 16bit linear signal. Finally, the 16bit linear signals or compressed 12bit signals are output through 4-lane MIPI or SLVS interface.

The image sensor is capable of operating at 120fps in a normal signal readout mode or 60fps in the SEHDR mode.

4. Fabrication and Characterization

The sensor is fabricated in a 65nm BSI CMOS image sensor process and assembled in a 48-pin PLCC package as shown in Fig. 4.

Photo conversion characteristics in normal modes are shown in Fig.5. Pixel conversion gains in the HPG condition, the MPG condition and the LPG condition are measured as 152μV/e^-, 38μV/e^- and 21μV/e^-, respectively. When the MPG is referenced as a base pixel gain, the pixel gain ratio is 4.0:1:0.57. Pixel linear full well is larger than 27ke^-. Noise floor at HPG and 8x amplifier gain is 1.0e^-.

Fig. 6 shows an example of photo conversion characteristics obtained under the SHEHDR mode with a gain setting of [MPG + Analog gain of 1x] and [HPG + Analog gain of 8x]. Effective gain ratio between the two signals is about 1:32. In this setting, signal is clipped at 23ke^- due to the 16bit digital output range. Dark noise floor in the SEHDR mode is identical to the noise at the highest gain setting of 1e^-. Therefore, maximum dynamic range of 87dB is obtained. The number of signal electrons at the conjunction point of the HPG signal and the LPG signal is about 800e^- in this setting.

The signal exhibits linear characteristics in the whole range from lower than 1e^- to the saturation level, which suggests charge transfer error from the photodiode to the charge detection node is smaller than 1e^- and doesn't affect low light image quality.

Random noise, pixel FPN and column FPN are also plotted in Fig.6. Column FPN in low exposure conditions are lower than 1/20 the random noise and one can hardly see it.

When the amplifier gain is changed at the conjunction point, an excess noise and excess FPN are generated due to its circuit operation, and the excess random noise affects SNR by -3dB. Except for the excess noise, random noise characteristics follow the shot noise model of $\propto S^{-0.5}$ in a whole range. Comparing to the MEHDR scheme, no significant noise at the conjunction point is seen. When we suppose 1:1/32 integration time ratio in the MEHDR scheme, shot noise degrades about 15dB at the conjunction point as illustrated by the dotted line in the figure. This is one of benefits of the SEHDR scheme because no signal charges are lost.

Photo response non-uniformity (PRNU) of the sensor is lower than 0.5%, which suggests process variations of the gate capacitance and parasitic metal capacitance are acceptably small to be used for pixel capacitance.

Fig.7(a) and Fig.7(b) are captured images in the conventional MEHDR mode and SEHDR mode reported in this paper, respectively. Obviously, motion artifacts or LED flicker artifacts are suppressed in the single exposure image.

5. Summary

An image sensor which has an SEHDR feature is reported. Introducing a triple conversion gain pixel and a dual gain readout scheme, the sensor can cover intra scene dynamic range of wider than 87dB in a single exposure. Because of no signal loss in the high light condition unlike MEHDR, there is no significant SNR drop. In addition, the SEHDR scheme mitigates moving artifacts or flicker artifact in high dynamic range image applications.

Reference

[1] M. Mase, et al., "A wide dynamic range CMOS image sensor with multiple exposure-time signal outputs and 12-bit column-parallel cyclic A/D converters," in IEEE Journal of Solid-State Circuits, vol. 40, no. 12, pp. 2787-2795, Dec. 2005

[2] C. Silsby, et al., "A 1.2MP 1/3" CMOS image sensor with light flicker mitigation," Dig. IISW, June 2015

[3] T. Willassen, et al., "A 1280x1080 4.2μm split-diode pixel HDR sensor in 110nm BSI CMOS process," Dig. IISW, June 2015

[4] W. Wakashima, et al., "A linear response single exposure CMOS image sensor with 0.5e- readout noise and 76ke- full well capacity," Dig. VLSI Circuits, pp. C88-C89, June 2015

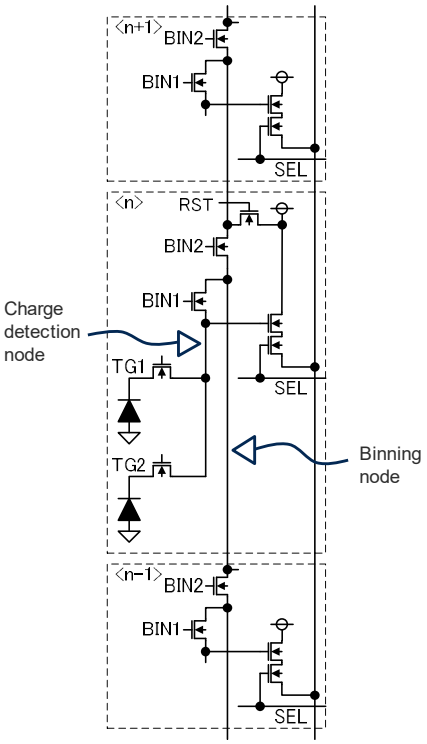


Fig. 1 Configuration of the triple gain pixel. RST transistors in top/bottom neighboring pixel are not drawn.

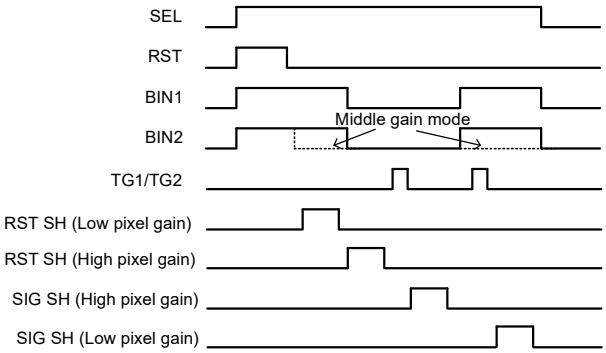


Fig. 2 Pixel operation timing sequence for dual gain pixel readout, combination of LPG mode and the HPG mode. When BIN2 control timing is changed to the dotted line timing, the middle pixel gain MPG signal is obtained.

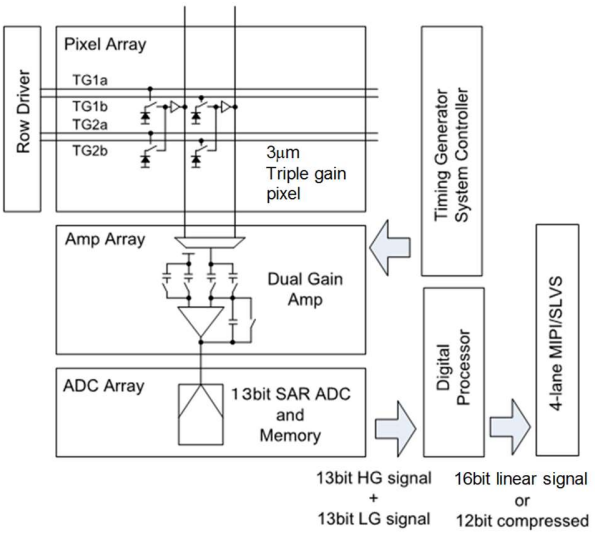


Fig.3 Sensor architecture. In order to readout even column pixel and odd column pixel serially, two TG bus lines (TG1a/TG1b and TG2a/TG2b) are introduced in a row.

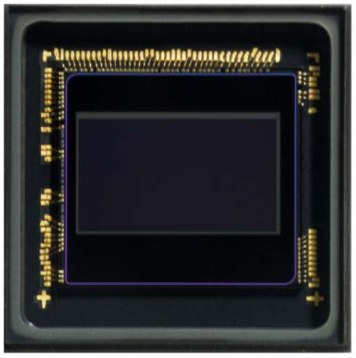


Fig. 4 Chip photograph. Assembled in a 48pin PLCC package.

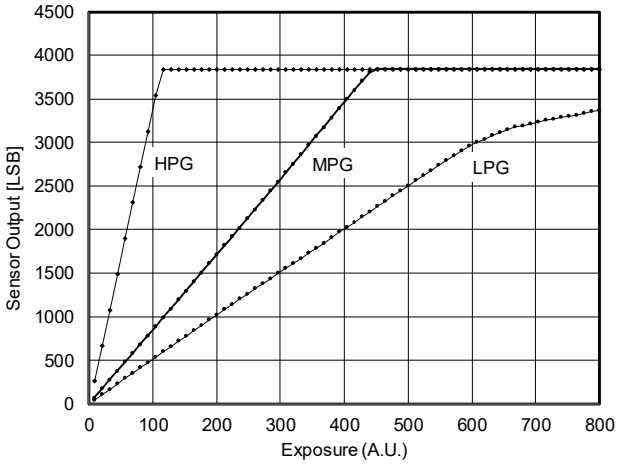


Fig. 5 Photo conversion characteristics measured in the HPG, MPG and LPG modes. In the LPG mode, photodiode saturation occurs before ADC saturation.

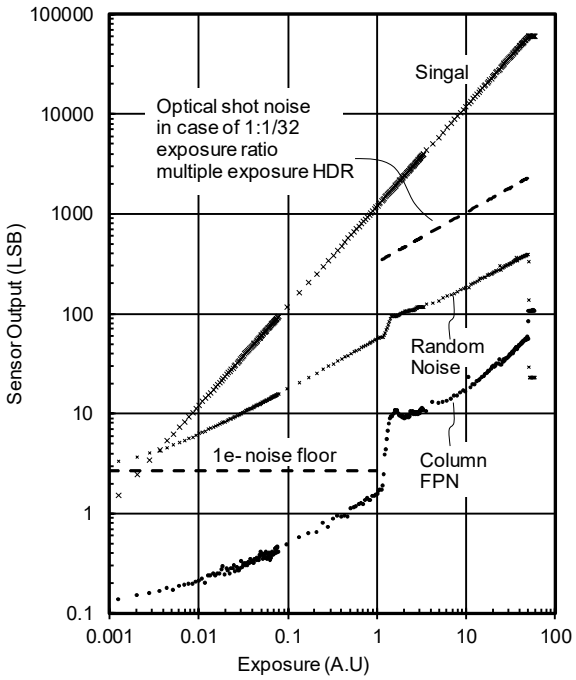
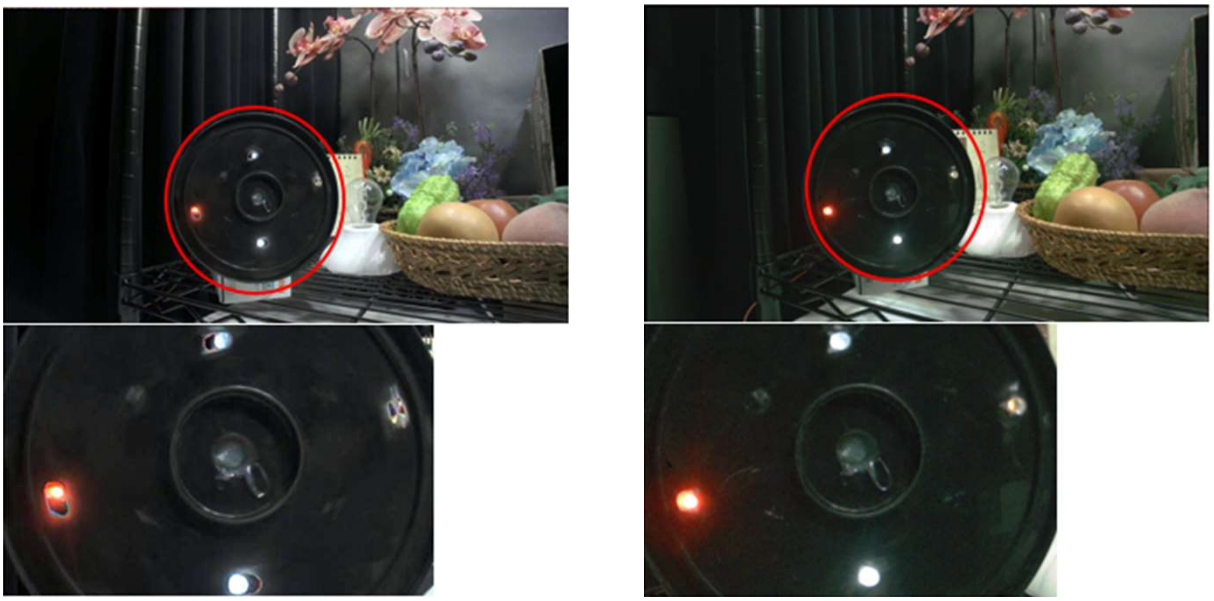


Fig. 6 Photo conversion characteristics are plotted with random noise and column FPN in the SEHDR mode. Gain combination is MPG + Analog gain 1x and HPG + Analog gain 8x. Output conversion factor in this condition is 2.68LSB/e^-.

TABLE I SPECIFICATIONS AND PERFORMANCE

Optical Format	1/2.7”
Pixel size	3.0μm
Effective pixels	1928x1088 pixels
Frame rate	120fps (Normal mode) 60fps (SEHDR mode)
Digital output	12bit (normal mode) 16bit or compress 12bit (SEHDR mode)
I/F	MIPI 4 lanes, SLVS 4 lanes
Max readout signal	23ke^- (SEHDR mode) >27ke^- (Normal mode)
Responsivity	24ke^-/lx·s
Peak QE in Green	78.8% (w/o glass)
Overflow blooming	<1%
Lag	<0.5%
Readout noise	1.0e^-_{rms} (max gain)
Column FPN	0.045e^-_{rms} (max gain)
Power consumption	280mW (120fps normal mode)



(a) Conventional multiple exposure dynamic range mode (b) Single exposure dynamic range mode.

Figure 7 Captured images of a rotating LED plate