Indirect ToF Pixel integrating fast buried-channel transfer gates and gradual epitaxy, and enabling CDS

Boris Rodrigues[1,3], Marie Guillon[2], Nicolas Billon-Pierron[2], Jean-Baptiste Mancini[2], Olivier Saxod[2], Benoit Giffard[2], Yvon Cazaux[2], Pierre Malinge[3], Patrice Waltz[3], Auguste Ngoua[3], Yannick Kerleguer[3], Alisée Taluy[3], Sarah Kuster[3], Sylvain Joblot[3], François Roy[3], Guo-Neng Lu[1]

[1] *Institut des Nanotechnologies de Lyon, Univ. Claude Bernard Lyon 1, 69622 Villeurbanne, France*
[2] *Univ. Grenoble Alpes, CEA, LETI, MINATEC campus, F38000 Grenoble, France*
[3]*STMicroelectronics, 850 rue J. Monnet BP16, 38926 Crolles cedex, France*
Tel: +33 4 38 92 23 11 - E-mail: boris.rodriguesgoncalves@st.com

***Abstract*-- In this paper we propose a time of flight (TOF) pixel with implementation of 3-sample phase-shifting (3-tap) technique. The pixel integrates a pinned photodiode (PPD) and 3 charge-transfer paths. Each path is delimited by deep trenches and integrates a fully depleted memory (storage site) enabling Correlated Double Sampling (CDS). In order to achieve fast and efficient charge transfer, each path also integrates a low-noise buried-channel Transfer Gate (TG) built on a doping-controlled epitaxial layer with a potential gradient to create both fringing field and vertical one for draining charges. The proposed pixel was designed in a size of 6.2µm x 6.2µm, and a test image sensor chip was fabricated in several configurations with variations of process parameters. Testing results show a dark current of 30 e-/s @60°C, readout noise of 3.2e- and a demodulation contrast (DC) of 73% @110 MHz using a 930nm light source. The pixel compatibility with common imaging process and voltage supply is an advantage for developments of imaging systems providing depth and color information within the same die.**

INTRODUCTION

Depth mapping is one of new challenges that we have to face for color image restitution. Several methods based on time-of-flight (TOF) have been realized for acquiring a depth image. One of them is based on a continuous wave (CW) modulation method for measuring distance [1]. The ultimate goal being the integration of depth and color pixel in the same die (RGBZ), we developed a pixel fully compatible with standard RGB pixel process and power supply. We propose here a 3D indirect TOF pixel based on the CW modulation method with implementation of a multi-tap approach [2, 3]. The number of storage sites is minimized to 3. The proposed pixel integrates a pinned photodiode (PPD) and fully depleted memories as storage sites. To optimized charge collection and charge transfer efficiency from PPD to different storage sites, it also integrates low-noise buried-channel Transfer Gates (TGs) built by optimized implantation on a doping-controlled epitaxial substrate to create electric fields: fringing field and vertical one. The pixel was designed in a size of 6.2µm x 6.2µm, integrated in a QVGA image sensor chip. The chip was fabricated in different configurations with variations of process parameters and tested.

PIXEL DESCRIPTION

The distance measurement of the pixel operates as follows. The scene is illuminated by a modulated near infra-red light source and the reflected light with delay is detected by the PPD of the pixel. Photo-generated electrons are then successively drained and stored in 3 different memory sites. Fig. 1a shows the 3-sample phase-shifting (3-tap) technique. The incoming signal is sampled at a high frequency, typically in the range from 10MHz to 130MHz [4]. The phase difference between the emitted light signal and the received one by reflection is then calculated and the distance is determined through the following relations [1]:

$$\varphi = \arctan\left(\sqrt{3}.\frac{C_2 - C_1}{(C_1 - C_0)+(C_2 - C_0)}\right) \qquad (1a)$$

$$D = \frac{c_{light}}{4\pi f}\varphi \qquad (1b)$$

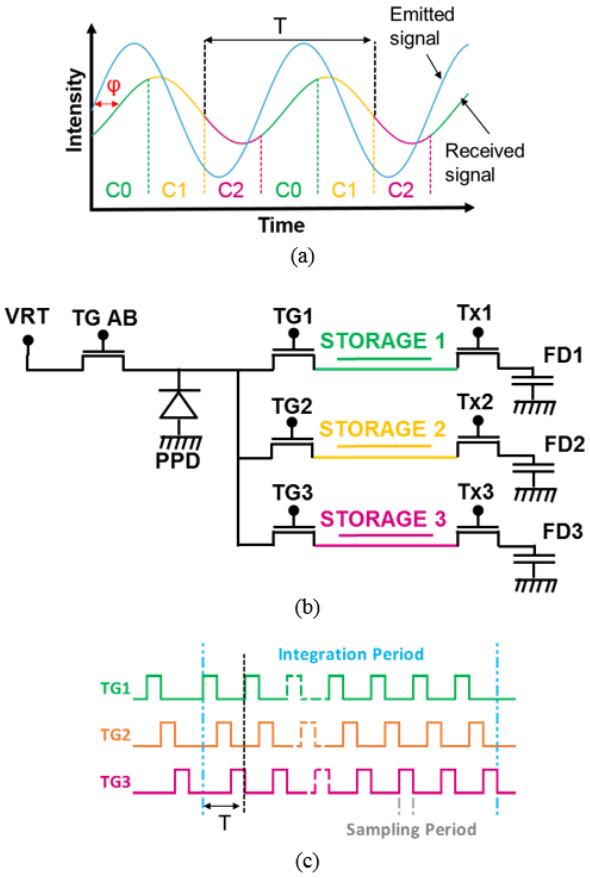


Figure 1: (a) Continuous wave (CW) modulation method with 3-sample phase-shifting (3-tap) technique for distance measurement; (b) Our proposed 3D TOF pixel implementing the 3-tap technique; (C) Controlling signals of buried-channel transfer gates (TGs) for signal sampling and charge transfer.

Fig. 1b shows the proposed pixel with 3 charge-transfer paths performing successive sampling over an integration period. An additional fourth path is also included for anti-blooming (AB) purpose. Each path is controlled via a buried-channel TG for transfer of signal charges. For a signal sampling with charge transfer in one path, the corresponding TG is switched ON by a succession of pulses during the integration time.

Fig. 2 shows charge transfer of one path from PPD to FD (floating diffusion) node through storage site.

When TG is ON, photo-generated electrons from PPD are temporary stored beneath its gate (Fig. 2a). When it is OFF, the packet of electrons is transferred into the memory (storage site) (Fig. 2b). After a succession of switching TG with charge transfer, when the integration period is over, the whole sampled signal in charges is stored in the memory (Fig. 2c). For signal reading, the stored charges can be transferred into the FD node by turning Tx gate ON (Fig. 2d). This architecture allows CDS (before and after charge transfer through Tx gate), which eliminates KTC noise and rejects most 1/f noise.

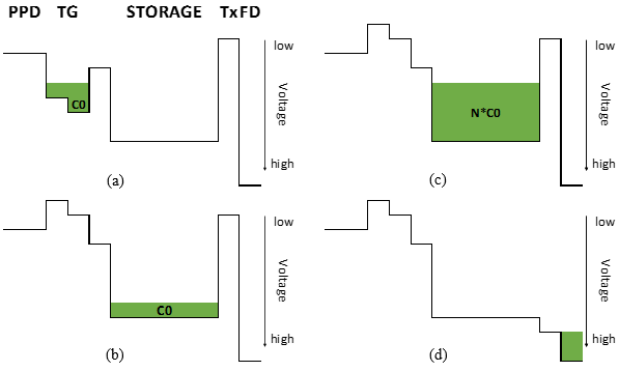


Figure 2: Signal-sampling and charge transfer process of a path from PPD to FD node.

Each charge-transfer path is delimited by deep trenches. Major process parameters need to be optimized to ensure a gradual potential for complete transfer of charges, such as layer shapes and doping concentrations. Fig. 3 shows 3D TCAD simulations of electrostatic potential between PPD and storage in a charge-transfer path, for the switched TG in ON and OFF states respectively.

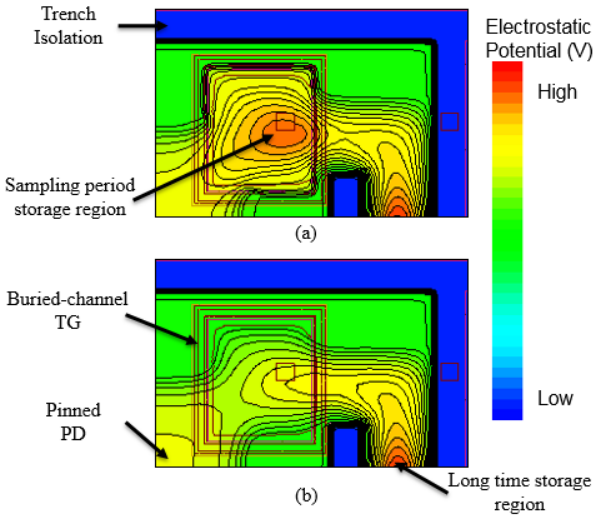


Figure 3: 3D-TCAD simulations showing electrostatic potential in a charge-transfer path between PPD and storage site, for TG is ON (a) and OFF (b)

The TG in each path plays a key part in the charge transfer. We propose integration of a buried-channel TG structure to avoid interface trapping effect and to create horizontal fringing field. This device structure has been optimized for fast and efficient charge transfer. Furthermore, when integrating it on a doping-controlled epitaxial substrate with a desired potential gradient, a vertical electric field is created to help draining the charges. The charge-transfer performance is optimized with fully depleted path, which also improves noise performance. Fig. 4 shows the TG structure on either uniform-doping epitaxial substrate (Fig. 4a) or doping-profile-controlled epitaxial one (Fig.4b). It is worth mentioning that high charge-transfer performance is required to successfully demodulate the received signal by sampling it in different storage sites without loss of charges.

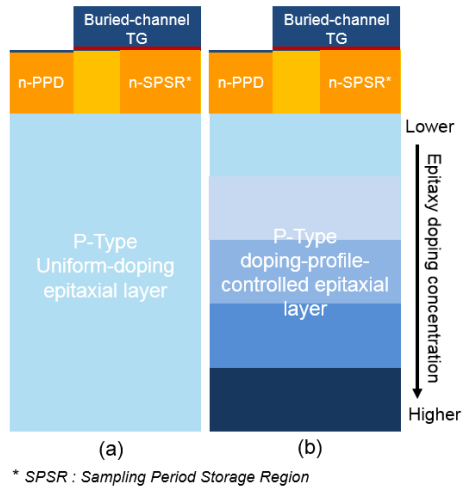
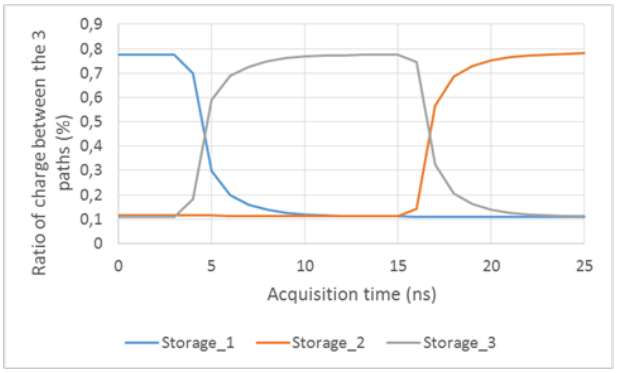


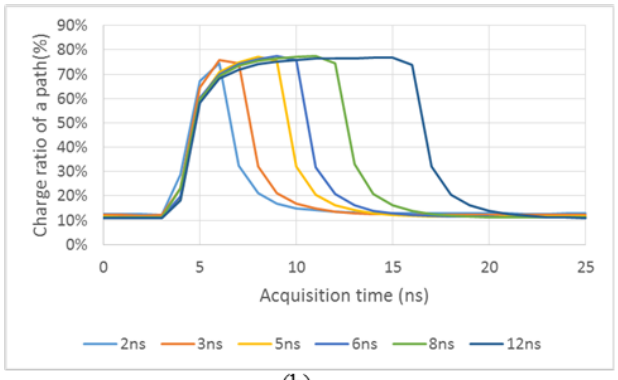
Figure 4: Structure of the buried-channel TG fabricated on a (a) uniform-doping epitaxial layer; (b) doping-profile-controlled epitaxial layer

EXPIRIMENTAL RESULTS

The designed 464x197-pixel (QVGA) test chip was fabricated in different configurations: uniform-doping epitaxy (UDE), doping-profile-controlled epitaxy (DPCE) and DPCE with optimized implantation and shape of TG (DPCE+O). A "burst characterization" was performed to evaluate charge-draining capability of the TGs. It consisted in synchronizing a received laser pulse with one TG's opening time during integration. Then the sampled signal (in charge packet) stored in the corresponding memory (after integration time) was compared to the sum of the stored charges in all memories. Fig. 5a shows charge ratios of different storage sites for the DPCE+O configuration, indicating that more than 70% of photo-generated electrons go to the desired storage site. The charge-draining via TG control is efficient for opening time down to a few nanoseconds (Fig. 5b).



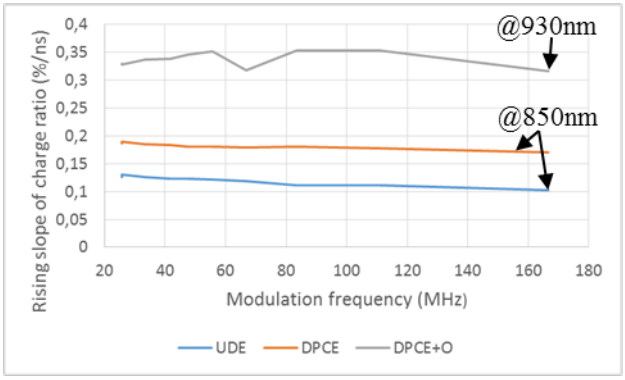
(a)



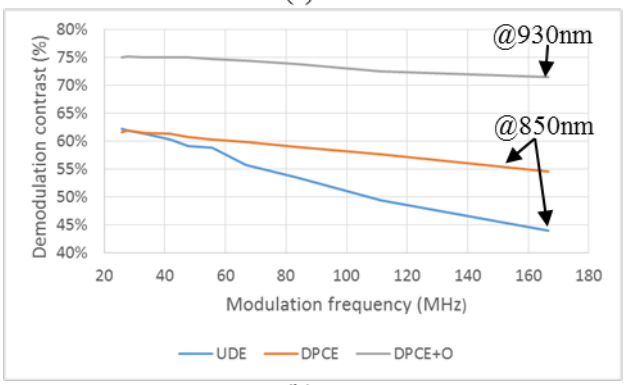
(b)

Figure 5: Ratio of charges in a memory to those in all the memories (measured at 930nm): (a) comparison between the 3 paths for a sampling period of 12ns; (b) Charge ratio of a path for different sampling periods

Fig. 6a compares charge-transfer speed in terms of rising slope of charge ratio between the three configurations. The DPCE configuration exhibits a 50% increase compared to the UDE one, while the DPCE+O configuration almost doubles. The improvement in charge-transfer speed leads to higher demodulation contrast (DC): DC = (A-B)/(A+B), where A and B correspond to the maximum and minimum of the charge ratio respectively. Fig. 6b shows that, compared to UDE configuration, DPCE improves the DC especially at high frequencies, with 58% at 110 MHz (3ns of corresponding sampling period), while DPCE+O enhances the DC in all the frequency range, with up to 75% at 50 MHz and 73% at 110 MHz.



(a)



(b)

Figure 6: (a) Rising slope of charge ratio versus modulation frequency; (b) Demodulation contrast versus modulation frequency

Table 1 presents a summary of our pixel's characteristics, in comparison with recently reported studies [4, 5]. Our achievements include high demodulation contrast ratio, low dark current, and low readout noise. Fig. 7 shows an acquired 3D image from the (QVGA) test chip in DPCE configuration, illuminated by a 25MHz 870nm LED.

Table 1: Main measured characteristics of our 3D TOF 3-tap pixel in comparison with results from two reported studies [4, 5].

Parameter	Our pixel	A. Payne et al. [4]	E. Tadmor et al. [5]
Pixel size	6.2µmx6.2µm	10µmx10µm	6.7µmx6.7µm
Array resolution	464 x 168	512 x 424	360 x 180
Conversion Gain	62 µV/e-	26 µV/e-	64µV/e-
FWC	3 x 12 ke-	100 ke-	4 x 9.5 ke-
Read out Noise	3.2e-	12.3e-	7.5 e-
Dark current	30 e-/s @60°C	-	30000 e-/s @50°C
Demodulation Contrast	75%/73% @930nm @50Mhz/110MHz	68%/57% @860nm @50Mhz/130MHz	98% @850nm @100Mhz
QE	6% @850nm	6% @850nm	10% @850nm
Volatge swing	2.5V	3.3V	7V
Max Frequency	160MHz	130MHz	>100MHz

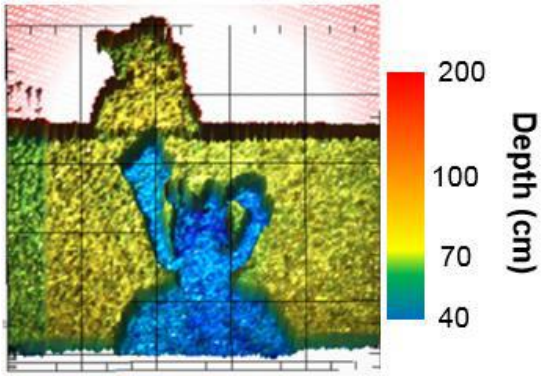


Figure 7: 3D image taken using a QVGA test chip with a 870nm LED source modulated at 25 MHz (Modulation frequency limited by the led source)

CONCLUSION

This paper present a novel pixel structure for depth map acquisition. We have developed 6.2µm-pitch 3D TOF pixel using pinned photodiode, fully depleted memories and operate with a standard 4T reading architecture. Integration of buried-channel TGs built on a doping-profile-controlled epitaxial layer improves charge-transfer efficiency and speed, which lead to improvement in demodulation contrast. The proposed pixel could be applied to 3D imaging systems such as RGBZ camera with an integration advantage in compatibility with common imaging process and voltage supply.

REFERENCES

[1] R. Lange, PhD Thesis "3D Time-of-Flight Distance Measurement with Custom Solid-State Image Sensors in CMOS/CCD-Technology", 2000.

[2] B. Bûttgen, et al., "Demodulation Pixel Based on Static Drifts fields", in IEEE Transactions on Electron Devices, vol.53, no.11, pp.2741-2747, 2006.

[3] D. Stoppa, et al., "An 80×60 Range Image Sensor Based on 10µm 50MHz Lock-In Pixels in 0.18µm CMOS", in Proc. ISSCC, 2010.

[4] A. Payne et al., "A 512×424 CMOS 3D Time-of-Flight Image Sensor with Multi-Frequency Photo-Demodulation up to 130MHz and 2GS/s ADC", in Proc. ISSCC, pp134-135, 2014.

[5] E. Tadmor et al., "Development of a ToF Pixel With VOD Shutter Mechanism, High IR QE, Four storages, And CDS", in IEEE Transactions on Electron Devices, Vol.63, no.7, July 2016.