Mutually Coupled Ring Oscillators for Large Array Time-of-Flight Imagers

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Abstract — **Time-of-flight (TOF) image sensors require high levels of accuracy and precision on time quantization, typically through a Time-to-Digital Converters (TDCs). Achieving such performance, while keeping power consumption low, is not trivial, even more for large arrays. Although offsets (from asymmetry, overall speed variation, IR-drop induced variations, etc.) can be calibrated and corrected, varying offsets are harder to compensate for. In this paper, we present a simple and robust method for synchronization that drastically reduces process-voltage-temperature (PVT) variations, while providing noise filtering to reduce accumulated jitter. An 8 x 8 array of ring oscillators (RO), serving as many TDCs, is implemented. About 18 dB better phase noise and 14 dB better jitter is obtained, under 200 µW/GHz power efficiency and better than 100 ps resolution.**

Index Terms — **ring oscillators, coupled-oscillators, brusselator, time-to-digital converter, TDC, LIDAR, time-of-flight, TOF, noise reduction.**

I. Introduction

Time-resolved optical sensors have become important for various applications, such as PET, FLIM and LIDAR [1]. Those imagers, when implemented in CMOS, generally comprise avalanche photo diodes (APDs), operating in Geiger mode, known as single-photon avalanche diodes (SPADs), and time-to-digital converters (TDCs), which determine the time-of-arrival (TOA) of photons. In time-correlated operation mode, the incoming photons, which are periodically generated by a laser, can be precisely measured to lead to an accurate 3D map reconstruction of the scene. However, when a large number of pixels exists on a sensor, uniformity and precision on timing information becomes a major asset to obtain, especially for long range measurements, where non-linearity and jitter play big roles. Few solutions have been proposed and adopted, but they all suffer from one constrain or another.

In the most common case, a single, high-quality and PVT robust TDC is obtained through an always-on PLL/DLL [2], where most of the power consumption and non-linearity arise from the distribution network, where multiple phases of the oscillator are routed over large areas – potentially hundreds of square millimetres of silicon. A second solution is based on one TDCs per pixel [3], which can consume less power than the first case (depending on the activity), due to its event-driven operation, however, those TDCs may operate in open-loop and independently from each other, which is highly susceptible to PVT variations, jitter accumulation and non-linearity, offering no or limited synchronization between the TDCs. As a result, often elaborated calibration is required, yet these systems are still susceptible to dynamic fluctuations. Hybrid solutions exist [1], where high-quality and relatively low frequency is distributed over the chip and the fine resolution is implemented locally, but they are very complex and they still present issues from both approaches, although less stringent.

In this paper, we investigate a solution where a high-quality reference frequency is obtained locally, without excessive power consumption and complexity. It operates under phase and frequency locking, independently of the conditions on the chip, such as process variation, static and dynamic voltage and temperature drifts as well as external disturbances. The solution is based on various ultra-low power oscillators, cross-coupled to their neighbours and shared among several pixels, to be used as fine TDCs. A re-sampled asynchronous 10b counter is then clocked by the fine TDC to be used as coarse TDCs.

The paper is divided as following: in section II, the concept is discussed and system analysis and simulation is performed. In section III, the TDC architecture is reviewed and in section IV, the experimental results are presented and discussed, to conclude at section V.

II. System analysis and Simulation

The key challenge of providing an accurate reference phase/frequency for TDCs over a very large sensor area is limited by physical constrains, being subjected to silicon imperfections, manufacturability variations, temperature, IR drop, circuit asymmetries, etc. While some of the static variabilities in performance can be compensated for, dynamic variations are very hard to calibrate. The problem becomes even worse with gradients that affect the performance of the sensor in a non-uniform way, typically produced by temperature and voltage differences over the chip.

Moreover, for long-term measurements, the accumulated jitter may cause larger imprecision than the quantization noise itself. Thus, a coherent design of the TDC, considering the jitter and resolution, is sensible and finer TDC resolution is only justifiable if its corresponding jitter matches the quantization noise. Nevertheless, jitter performance and noise filtering is highly appreciated. In this work, we propose an always-on network of ultra-low power oscillators that, coupled together, can generate a much cleaner reference than an independent oscillator, without the need to high quality (and power hungry) systems.

Due to area constrains, typically Ring Oscillators (RO) are used as TDC in imagers. Usually, they have power efficiency – FOM [4] – in the order of 145 - 160 dB, which is quite low. It depends on the strength of the stages (overall power consumption), number of stages, and on the topology. As an example, without any elaborate filtering (through a PLL/DLL, for instance), a 1 GHz RO consuming 200 μW and FOM of 150 dB produces an integrated RMS jitter of about 110 ps (from 1 MHz to 100 MHz integration window), which is prohibitively large for TOF applications with millimetre resolution requirements, usually requiring feedback loops for noise filtering, at the expense of power, area and complexity.

Multiple oscillator coupling is used in many fields and applications [5]. Due to uncorrelated phase noise in different oscillators – at roughly the same frequency –, when coupled, the phase noise of the system reduces by $10 \cdot \log_{10} M$ [6], where M is the number of coupled oscillators. Although the FOM of the system remains the same (since overall power also increased by M times, as the collective sum of individual oscillators), at each oscillator, the FOM appears to improve also by $10 \cdot \log_{10} M$.

Thus, the main idea of this work is to split a potential bulky and power hungry oscillator into a multiple weaker version of the same oscillator, over the whole array, and couple them by one of their differential phases. It will then induce a mutual coupling at fundamental frequency, synchronizing them in phase and frequency, as well as benefitting from noise filtering. The conceptual idea is shown at Fig. 1, where the oscillators are coupled via resistive elements.

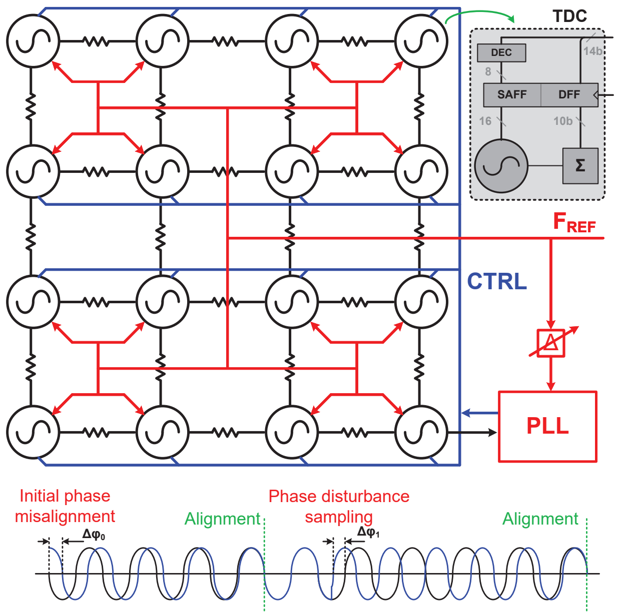

Fig. 1: 4 x 4 Mutually-coupled oscillators architecture and phase misalignment self-correction.

Another advantage of this implementation is shown at the bottom of Fig. 1. At the beginning of operation, the oscillators can have slightly different frequencies and completely random phases, but after coupling, phase alignment (and consecutively frequency) is reached. Similarly, when the phases of one of the oscillator are disturbed (due to a TOA sampling, for example), the neighbours help it get back to realignment, without propagating the error indefinitely, like in an open-loop case. The strength of the coupling depends on the coupling resistance between the oscillators, which influences largely the transient time, but less the phase noise reduction.

Moreover, to be able to enable/disable the coupling (for demonstration purpose), a transmission gate element is implemented as in Fig. 2, where a large array example is depicted. In this paper, a stacked technology is proposed, however, it is not at all necessary.

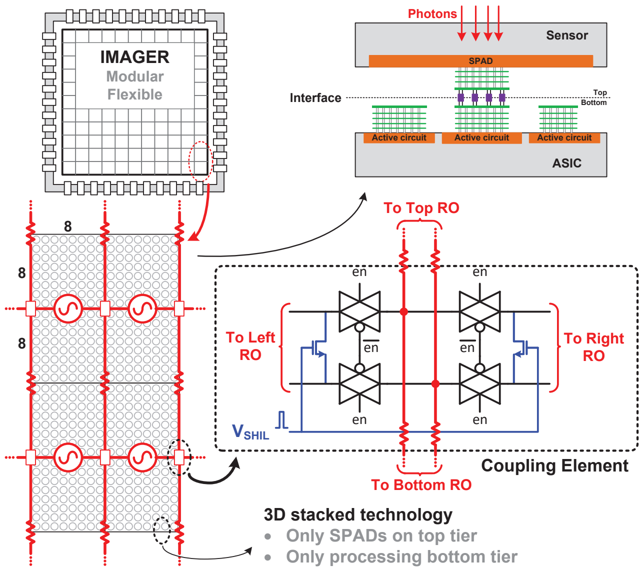

Fig. 2: Concept for TDC distribution over pixel groups and coupling elements.

To demonstrate the proposed mechanism, oscillators are coupled and the simulation results are depicted at Fig. 3. The phase noise reduction behaves as predicted (for the uncorrelated noise) when a different number of oscillators is used. For the correlated noise, as the thermal noise on the coupling elements (high offset frequencies), the benefit of the coupling is lower, which is, in principal, not an issue, since almost no jitter comes from that.

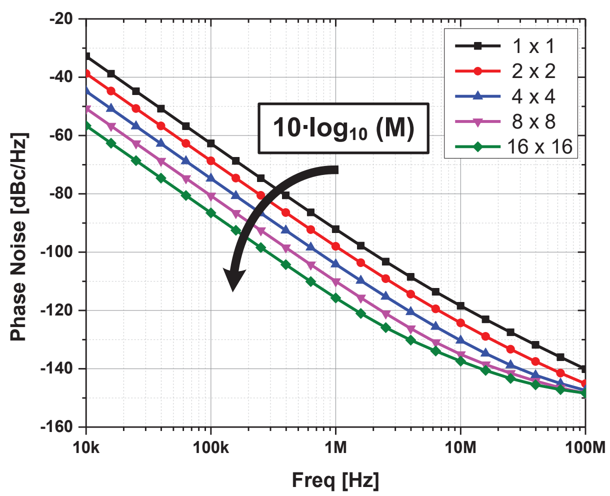

Fig. 3: Simulation of phase noise reduction from 1 (1 x 1) to 128 (16 x 16) coupled ROs.

As a proof-of-concept, 64 oscillators (8 x 8) were designed, where the simulation of the phase mismatch over time is shown at Fig. 4. Although there is still some phase misalignment (which is fixed and can be easily compensated for), coming mainly from individual performance variation (20% variation added in the simulation) and relatively large resistive coupling, after 20 ns the system is phase- and frequency-locked.

The proposed system provides lower phase noise without incurring any additional power consumption due to mutual coupling, since there is virtually no current flowing between the locked oscillators. Thus, the power efficiency increases by exactly $10 \cdot \log_{10} M$ as previously seen in section II.

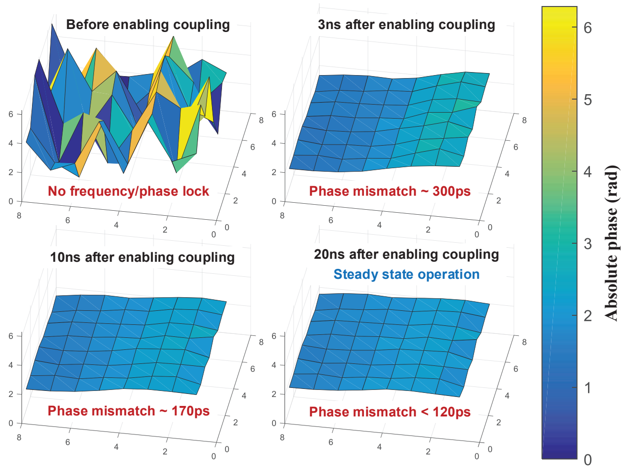

Fig. 4: Phase mismatch with 10% RO performance variation over 8 x 8 TDCs.

III. Circuit Description

The analysis performed in the section II is generic for any kind of oscillator. For TOF, however, the TDC range and resolution needs to be considered while choosing topology, frequency, etc. Apart from other system merits, for maximum power efficiency, the quantization noise of the TDC and its accumulated jitter should be in the same order.

Starting from a reasonable 150 dB FOM RO at 1 GHz – as the example at section II –, and coupling 64 of them (in an 8 x 8 structure), the effective FOM is reduced by $10 \cdot \log_{10} 64 \cong 18\ dB$, to a moderate 168 dB FOM, which produces an integrated RMS jitter (from 1 MHz to 100 MHz) of 13.75 ps. For the quantization noise in the TDC to correspond to 13.75 ps, it would be produced by an LSB in the order of 48 ps, as the standard deviation of the approximately uniform distributed, $\sigma = \Delta_{LSB}/\sqrt{12}$.

To reach 48 ps resolution, using a (pseudo-) differential RO at 1 GHz, it would require approximately 10 stages (and 20 phases). For the sake of simplicity, 8 stages (and 16 phases) were used, so binary code can be readily decoded. Fig. 5 shows the schematic of the pseudo-differential RO implemented, where the V_{DD} of the inverters are connected to a common pMOS current source, for frequency tuning. To further reduce the overall power consumption, the TDCs can be shared between two subgroups (subgroup 0 and subgroup 1) and its phases sampled by Sense-Amplifier Flip Flops (SAFF).

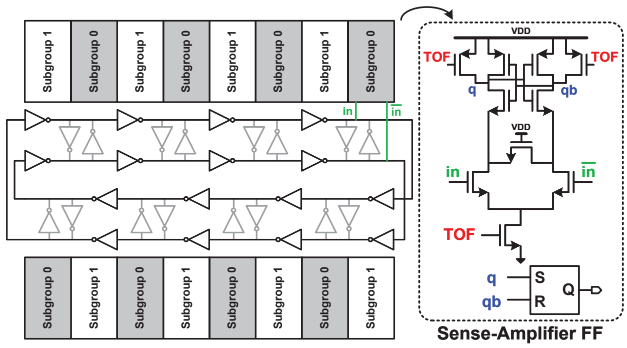

Fig. 5: 8-stage pseudo-differential RO and SAFF placement (subgroups) and detail.

IV. Experimental Results

The experimental results of the 64 RO (in an 8 x 8 fashion), under two conditions, coupled and uncoupled, were designed in standard CMOS 65nm are presented. Looking forward to mimicking a large sensor network, where the TDCs would be apart, such as in Fig. 2, the test structure was also made large. In our case, the TDCs are 78 x 5 µm^2 (already including a 10b counter) and are placed with pitch of 158 µm, to a total area of 1.1 x 1.1 mm^2. In this experiment, this area is left mostly empty, but it will be occupied by the rest of the processing unit to complete the sensor

As previously described, if the oscillators have similar frequencies, when coupled, they would reach phase and frequency locking. In our test chip, however, a large IR drop was present, due to low number of metal layers (3 + 1 thick), which influence can be seen at Fig. 6 a). To illustrate the effect of coupling, the individual frequencies of each of the oscillators, around the test frequency of 500 MHz, before and after coupling, are shown.

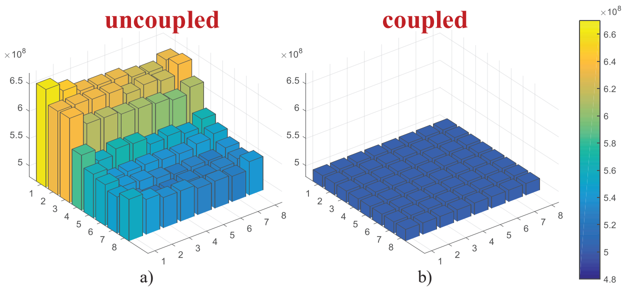

Fig. 6: Individual frequencies of all 8 x 8 ROs.

The effect of mutual coupling on different frequencies have also been measured. The result is presented on Fig. 7, where the average frequency and error bar are plotted. The frequency spread reduced from 22 to 26% (before coupling) to less than 0.11% (after coupling). From a slow frequency of 150 MHz (420 ps TDC_{LSB}) up to 750 MHz (83 ps TDC_{LSB}), the coupling effects behaves the same.

Since we use resistive coupling, which has bandwidth response from DC, the phases coupled are always being corrected (if any mismatch is present), reaching steady-state very quickly. A capacitive coupling could also be used instead of resistive, which has the advantage of supporting DC mismatches between oscillators, thus zero static current, but with the disadvantage of longer locking transient.

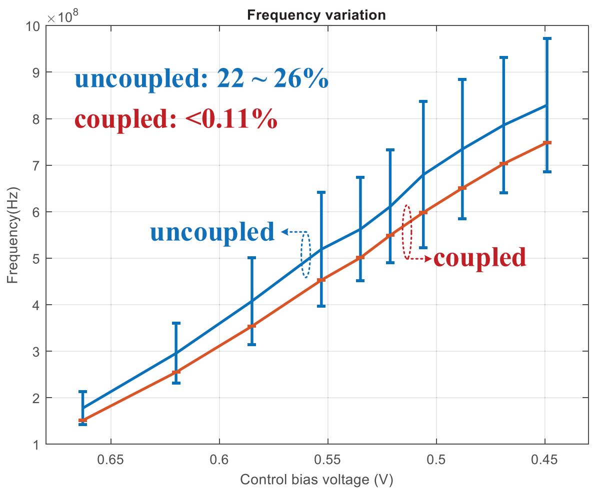

Fig. 7: Frequency variation of uncoupled and coupled 8 x 8 oscillators, for different average frequencies.

Fig. 8 shows the phase improvement provided by the coupling, even under large variation of individual frequencies (on the order of 100 MHz at 500 MHz), indicating a powerful tool for synchronization. For different frequencies, similar improvement is observed.

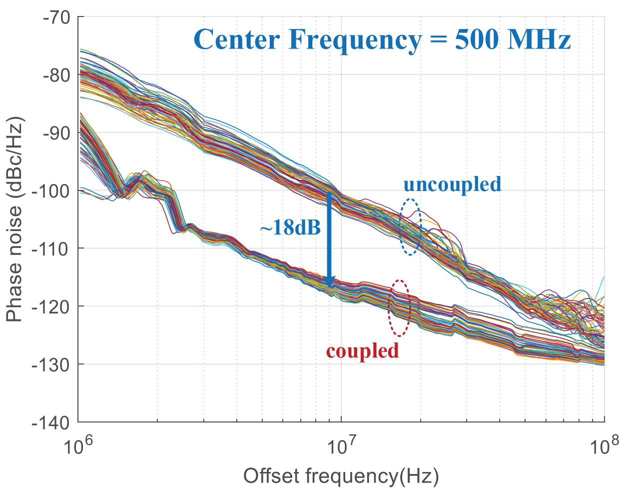

Fig. 8: Phase noise comparison at 500 MHz, for uncoupled and coupled modes, for all 64 ROs.

Fig. 9 shows the phase noise at 3 MHz and integrated RMS jitter, for all 64 ROs. As predicted, the phase noise gets improved by approximately 18 dB. Consecutively, the jitter also reduced from around 40 ps to 9 ps, an improvement of approximately 14 dB. Ideally, the jitter should also reduce by 18 dB, but the correlated noise, from coupling elements, multiplexers and buffers for the readout, limits the jitter improvement. The overall power consumption for all 64 ROs, without the power consumed on the multiplexers and buffers, was about 6.4mW at 500 MHz, leading to an average of 100 µW per TDC.

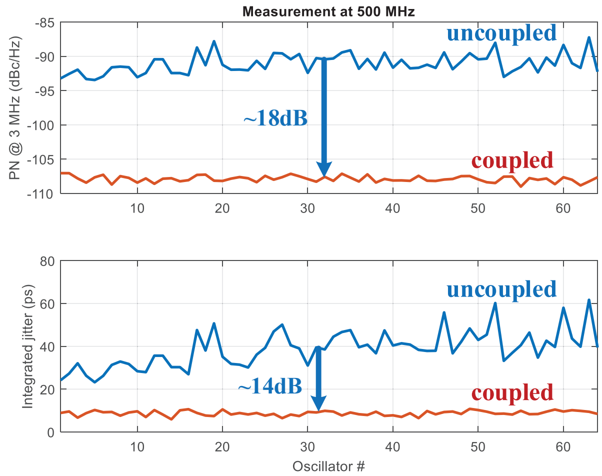

Fig. 9: Phase noise and integrated RMS jitter for uncoupled and coupled modes, for all 64 ROs, at 500 MHz.

V. Conclusion

A simple and robust mechanism for synchronization of multiple oscillators, to operate as TDCs, have been introduced and implemented. It has been demonstrated that, even at large frequency variations (from performance or temporary disturbances), the system is capable to provide frequency and phase locking, potentially suffering only from short range INL (since all the corresponding counters – to form a larger TDC – are clocked synchronously by the locked ROs), in case the oscillators have different performances. Thus, for best filtering and linearity, all identical ROs should be carefully connected and powered, so they can have similar individual frequency.

For monitoring purposes, each individual oscillator was connected via multiplexes and buffers, introducing imbalance and extra load to the ROs. Thus, the results presented here are slightly compromised than it is expected for the real sensor implementation. Nevertheless, it does not affect the technique (and in fact proves its robustness) that showed close relation with theory, with about 18 dB phase noise improvement at 3 MHz and 14 dB jitter improvement, as well as complete synchronization, under less than 100 µW/TDC at 500 MHz (125 ps resolution).

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