A Flexible 32x32 Dual-Side Single-Photon Image Sensor

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Abstract

We present the first flexible dual-side single-photon avalanche diode (SPAD) image sensor in array format. The image sensor comprises 32x32 pixels, whereas a special layout and fabrication flow were developed to fabricate the sensor. SPAD breakdown voltage, noise, sensitivity and crosstalk were thoroughly analyzed. The sensor is operated both in frontside- (FSI) and backside-illumination (BSI), whereas a dual-objective camera demo was built to simultaneously demonstrate the sensor in FSI and BSI modes.

Introduction

Photon-counting imaging technology has applications in many fields such as fluorescence lifetime imaging microscopy (FLIM), time-resolved Raman spectroscopy, 3D imaging via LIDAR, and even free-space (quantum) communications. The capability of detecting single photons with picosecond temporal resolution makes single-photon avalanche photodiodes (SPADs) a popular choice. Advanced biomedical imaging applications such as pill cameras, retinal prostheses, and implantable biocompatible monitoring sensors require a compact image system, which can be implanted into a living body [1-4]. To meet these requirements, novel single-photon image sensor solutions need to be developed, in which new substrate post-processing, backside-illumination or even dual-side illumination are core technologies, with inherent CMOS compatibility as a prerequisite.

In our previous work, we demonstrated the world's first flexible CMOS ultrathin-body SPAD [5, 6]. In this paper, we present the first flexible 32x32 dual-side SPAD image sensor chip fabricated in a class-100 cleanroom at Else Kooi Lab (TUDelft) and give thorough analysis on the characterizations.

The flexible chip shows consistent optical sensitivity, compared with previous single-pixel results in [6]. It shows high PDP uniformity and a reasonable yield. Negligible electrical and optical crosstalk were observed, thanks to good electrical and optical isolation. Furthermore, dual-side photon-counting imaging was achieved and tested, while by resolution enhancements could be achieved by multiple exposure.

Fabrication and Sensor Architecture

Based on the fabrication in [6], the flowchart of the 32x32 SPAD image sensor is shown in Fig. 1. It starts from silicon epitaxy on SOI wafer with lightly P-type doping, through front-end and back-end processes, ending with substrate transfer post-process. The front-end process includes CMOS transistor fabrication, SPAD junction implantation, trench isolation, and thermal annealing. Different from [6], back-end process parameters, such as spacer dimension, thickness of different passivation layers and metal layers are optimized according to the layout. After the back-end process, the chip is functional as SOI and followed by substrate transfer post-process.

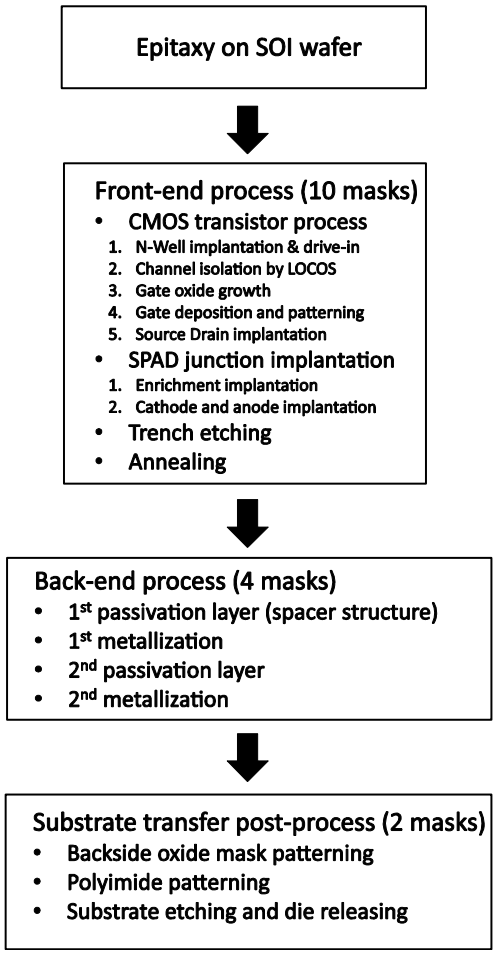

Fig.1. Flowchart of flexible CMOS SPAD sensor fabrication.

As shown in Fig. 2 (a) and (b), the pixel consists of a SPAD, a quenching resistor, and 4-transistor circuitry functioning as buffer and switch. SEM images of metallization topography and interconnection crossing are also shown in Fig. 2 (c) and (d), respectively.

The flexible chip was released by a reasonable mechanical force, after DRIE substrate etching, shown in Fig. 3 (a). To characterize the flexible chip, we mounted it onto a specially designed wire-bonded PCB. The front-side and back-side images are shown in Fig. 3 (b) and (c).

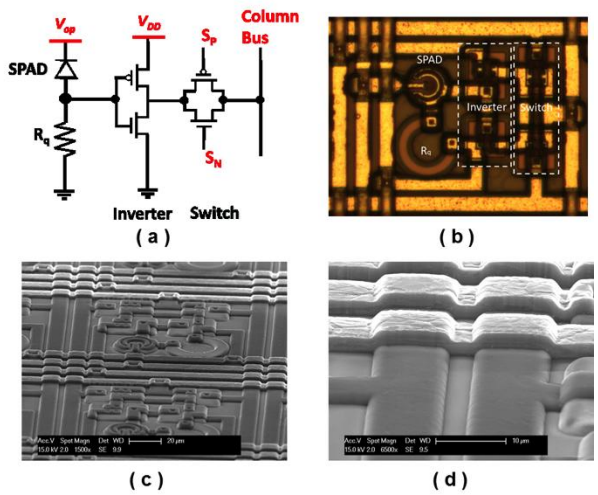

Fig.2. (a) Pixel schematic; (b) Microscopic image of pixel. (c) SEM microscopic image of chip. (d) SEM image of interconnect crossing.

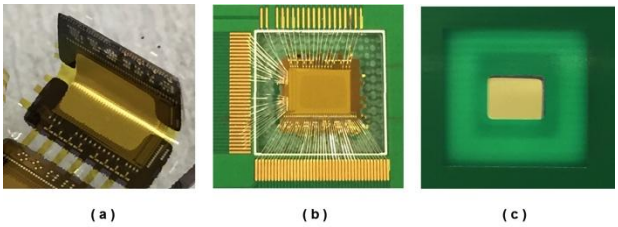

Fig.3. (a) bendable chip released after substrate etching; (b) front-side of flexible chip mounted onto PCB; (c) back-side of flexible chip mounted onto PCB;

Measurement and analysis

The diagram of the readout system is shown in Fig. 4. Imaging readout and signal processing are implemented on FPGA, owing to the digital nature of SPADs. DCR distribution histograms over an array under different operation voltages are shown in Fig. 5. In general, the DCR distribution was modeled and fitted with a Gaussian distribution, excluding the hot spots [7]. The mean value of DCR increases as the operation voltage increases and the histogram FWHM value of distribution becomes larger. By cooling down the flexible chip from 22.7ºC (room temperature) to -70ºC, the mean value of DCR with V_{eb} of 4V was reduced from 200kHz to 30kHz while the histogram FWHM value of DCR distribution became smaller as temperature reduced (Fig. 6).

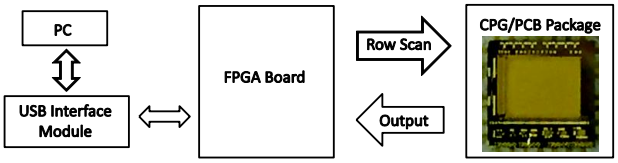

Fig.4. Diagram of the image readout and signal processing system.

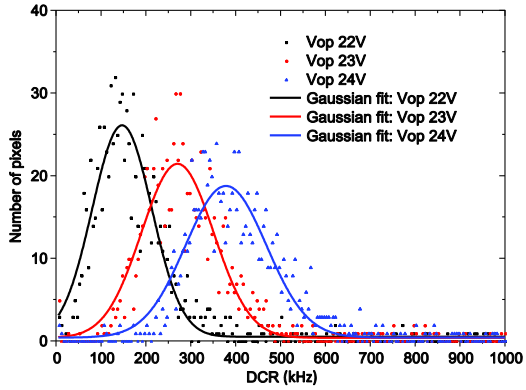

Fig. 5. DCR distribution histograms at different V_{OP}.

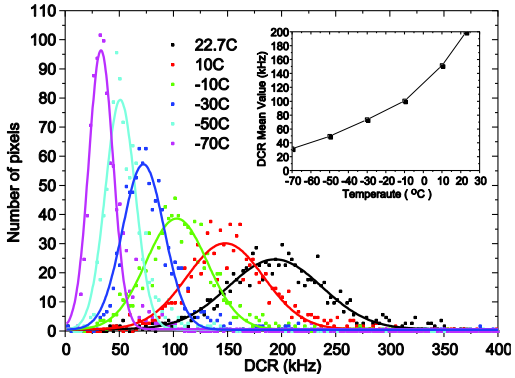

Fig. 6. DCR distribution histograms at different temperatures (Inset: DCR mean value at different temperatures)

The PDP of a single pixel from front-side and back-side illumination was analyzed in [6], while the PDP uniformity is studied here. A contour image of PDP non-uniformity across the 32x32 array is shown in Fig. 7 (a), together with a contour image of V_{BD} across the chip, shown in Fig. 7(b), whereas, as expected, PDP non-uniformity matches V_{BD} non-uniformity closely.

V_{BD} is further studied based on event count rate (ECR) statistical distribution under different V_{OP}, shown in Fig. 8. V_b, extracted from the cross point of fitting lines of saturated and non-saturated pixel distributions, which is defined as threshold value of breakdown voltages V_{BD} between saturated pixels and non-saturated pixels, decreases linearly as V_{OP} is reduced. For the non-saturated pixels, ECR decreases as V_{BD} increases while V_{OP} has a fixed value.

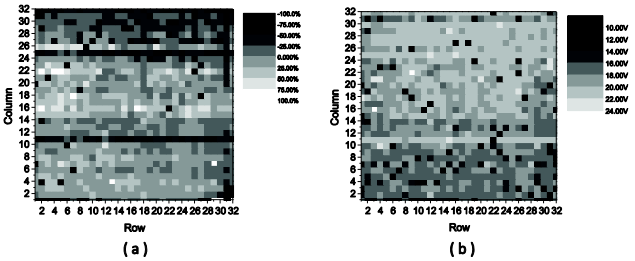

Fig. 7. (a) PDP non-uniformity across the sensor; (b) V_{BD} across the sensor.

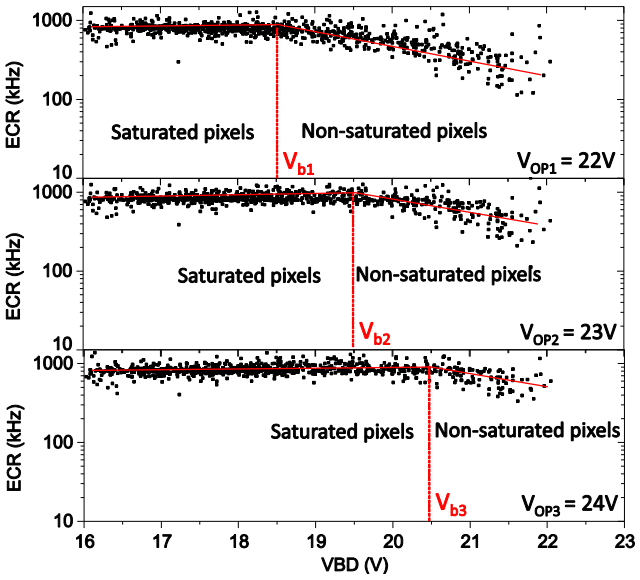

Fig. 8. ECR-V_{BD} distributions across the sensor under different V_{OP}. (V_{b1} - V_{b3}: values extracted from the cross point of fitting lines of saturated and non-saturated pixel distributions. Light source: 660nm-wavelength monochromatic light flux with power of 29μW/cm^2)

Crosstalk is negligible due to electrical and optical isolation in the flexible chip. Electrical isolation is achieved by SOI trench-isolation, while optical isolation is ensured by large pixel pitch, when compared with the multiplication region. It is further analyzed by gathering histogram information on inter-arrival times between both adjacent and non-adjacent pixels, showing a distribution fitted well with an exponential (Fig. 9), proving negligible crosstalk probability.

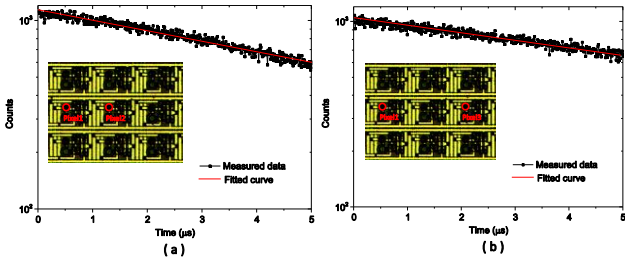

Fig. 9. Cross-inter-arrival time histogram measured from (a) two adjacent pixels; (b) two non-adjacent pixels.

Dual-side imaging camera

A compact signal-processing module was developed containing the chip board, a USB communication board, and a FPGA board. The detail setups of dual-side imaging camera are shown in Fig. 10.

The optical setup enables, for the first time, photon-counting images from both FSI and BSI mode using the same chip simultaneously, as shown in Fig. 11. The 32x32 chip was read at 32 fps by reading 32 columns in parallel. The images from both sides are comparable in terms of DCR, PDP, and DCR/PDP uniformity.

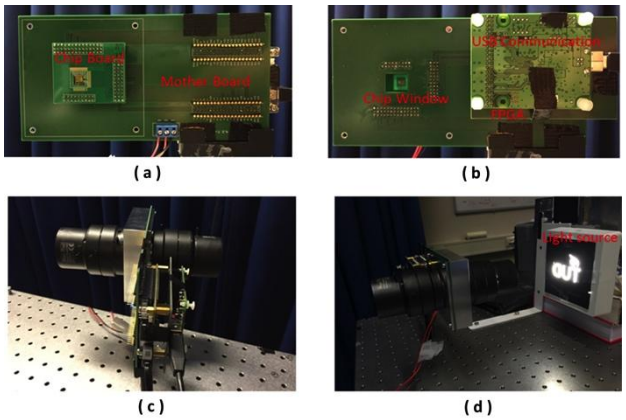

Fig. 10. (a) Front-side imaging signal processing module; (b) back-side of signal processing module; (c) dual-side imaging compact module; (d) imaging setup.

Fig. 11. “TUD” logo imaging on flexible 32x32 CMOS SPAD image sensor: (a) front-side imaging; (b) back-side imaging.

As shown in Fig. 12, by shifting the imaging object by half pixel dimension in X, Y and both X and Y directions, multiple frames could be integrated together to get an image with resolution enhanced by four both in X and Y directions [8].

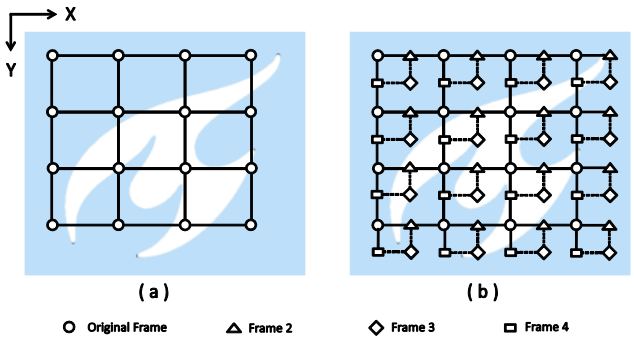

Fig. 12: Resolution enhancement method. Frame 2: shifting half pixel dimension in X direction. Frame 3: shifting half pixel dimension both in X and Y directions. Frame 4: shifting half pixel dimension in Y direction.

This method is applied in the imaging experiments with the flexible CMOS SPAD sensor chip and different resolutions such as 64x64 and 128x128 images are achieved, as shown in Fig. 13. Imaging results based on different exposure times are also compared.

Higher resolution and longer exposure time enable higher contrast and imaging quality. PDP non-uniformity, expressed as PRNU, could be reduced. Electrical and optical performance is summarized in Tab. 1.

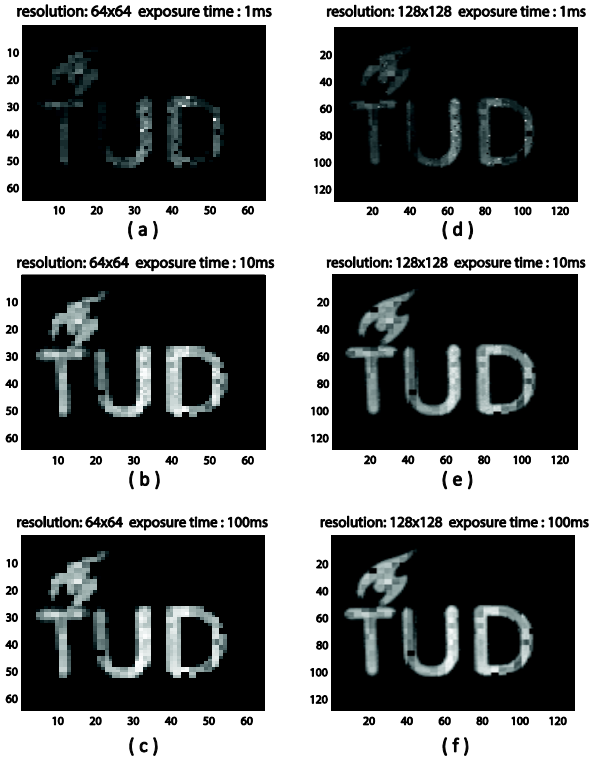

Fig. 13. Comparing of imaging based on different resolution and exposure times.

Tab. 1: Performance summary

Item	Min.	Typ.	Max.	Unit	Comments
Resolution	32x32		128x128		
Row rate		1k		fps	
Frame rate		30		fps	
Digital supply voltage		3.3		V	
SPAD V_{OP}	22		25	V	
Power dissipation			30	mW	Entire flexible chip
DCR		120		kHz	V_{OP} = 22V
DCR temperature dependence		1.5X/20°C			
V_{BD} non-uniformity		11%			
PDP non-uniformity		22.1%			@560nm; V_{OP} = 23V
PRNU		19.7%			
Signal-Noise Ratio		36		dB	
Dynamic range		25		dB	Estimated up to 52dB by active quenching at low temperature
Detectable light intensity	3.5			$\mu W/cm^2$	

Conclusions

We described a dual-side photon-counting image sensor implemented based on flexible SPAD technology. The statistical distribution of DCR and PDP shows reasonable uniformity, which mainly depends on the fabrication yield in the lab. It also shows negligible electrical and optical crosstalk thanks to good electrical and optical isolations.

Dual-side photon-counting imaging is achieved for the first time by a flexible SPAD image sensor. Sub-pixel resolution was achieved by multi exposures and X/Y shifting, showing an improved imaging quality resolution.

The imager can provide a suitable solution for advanced implantable photon-counting devices for retinal prosthesis and other localized therapeutic/diagnostic solutions.

Acknowledgements

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