Statistical Analysis of Random Telegraph Noise in Source Follower Transistors with Various Shapes

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ABSTRACT

In this paper, a statistical analysis of random telegraph noise (RTN) in source follower (SF) transistors with various shapes using an array test circuit is discussed. It is shown that a transistor without shallow trench isolation (STI) edge is effective for reducing RTN and the influence of traps at the source side on RTN is significant, from the evaluation of transistors with asymmetric gate width of source and drain.

INTRODUCTION

RTN is one of the most crucial problems in high-sensitivity CMOS image sensors. RTN occurs at in-pixel source follower amplifier of CMOS image sensors, and it causes deterioration of image quality, especially in low light scenes[1]. RTN in MOSFETs is caused by capture/emission of the carriers by/from traps in the gate insulator film[2]. RTN is a stochastic event and the influence of RTN becomes larger as the scale-down of CMOS circuits continues. It is difficult to reduce the effect of RTN by circuit technology only, therefore, it is necessary to introduce device and process technologies in a transistor level to reduce RTN. As methods to reduce RTN, for instance, introductions of buried channel transistor[3], atomically flat gate insulator film[4] and transistors with ring shaped gate[5-6] have been reported to be effective.

In this paper, a statistical analysis of RTN in SF transistors with various shapes (rectangle, trapezoid and octagon) using an array test circuit is discussed.

ARRAY TEST CIRCUIT STRUCTURE AND EVALUATION SYSTEM

Fig. 1 shows the block diagram of the array test circuit and Fig. 2 shows layout diagrams of the measured SF transistors with various gate sizes and gate shapes. The details of design specifications summarized in Table 1. In this research, besides general rectangular transistors, trapezoidal and octagonal transistors were also fabricated. Here, trapezoidal transistors are effective for the evaluation of influence of the trap location along source-drain direction[7]. Octagonal transistors are effective for the evaluation of the influence of the STI edge on carriers in the channel[5-6]. There are three rectangular transistors in Table 1. Here, Pix. 1 is a reference rectangular transistor. Pix. 2 and Pix. 3 are the rectangular transistors of the same area as trapezoidal and octagonal transistors, respectively. Each type of transistor was fabricated with a common gate length of 0.52 μm. These are all buried channel transistors[3]. There are 4608 pixels for each transistor type and these pixels are arranged in an array as a CMOS image sensor. In the column circuits, there are two readout paths used for different measurement modes. One path is connected to analog memories similar to conventional CMOS image sensor. The other path is directly connected to chip output buffer, it is used for high speed continuous signal sampling for selected pixels. Fig. 3 and Table 2 show the chip micrograph and the design specifications, respectively. There are $384^{H} \times 299^{V}$ pixels in this chip, including other SF transistors with different specifications in terms of gate insulator film thickness and carrier type in addition to the gate size and the gate shape. In this paper, we focus on the analysis of the gate sizes and the gate shapes. Fig. 4 shows a measurement board used to evaluate the RTN. In this measurement board, a low floor noise of 60 μV_{RMS} is obtained.

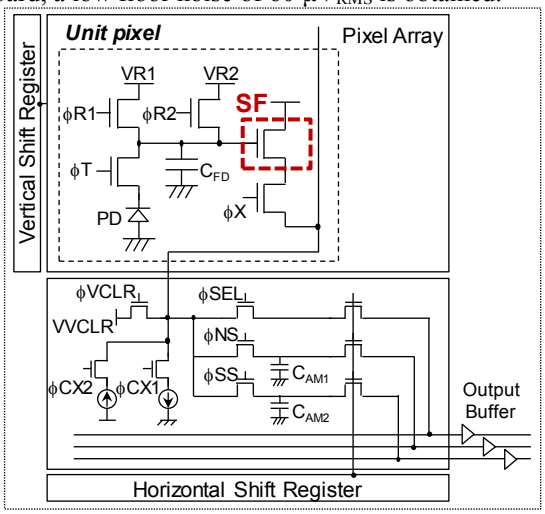

Fig. 1. Block diagram of the array test circuit.

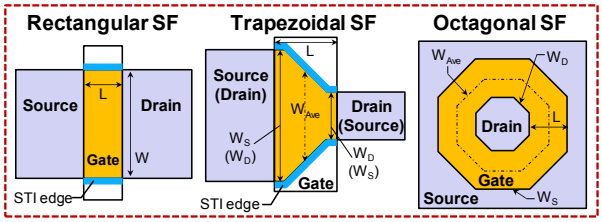

Fig. 2. Layout diagrams of the SF transistors.

Table 1
The measured SF transistor structures in pixel arrays.

Pixel No.	SF Type	SF Shape	L [μm]	W [μm]	W/L	Area [μm^2]	Number of Transistors	Targets
Pix. 1	3.3V nMOS (Buried Channel)	Rectangle	0.52	0.34	0.65	0.177	18048	Reference
Pix. 2			0.52	3.27	6.29	1.700	4608	Almost the same W/L as Pix. 6
Pix. 3			0.52	0.66	1.27	0.343	4608	Same W/L as Pix. 4 and Pix. 5
Pix. 4		Trapezoid	0.52	W_{Ave}:0.66 W_S/W_D:0.98/0.34	1.27	0.343	4608	Low current density at source side.
Pix. 5			0.52	W_{Ave}:0.66 W_S/W_D:0.34/0.98	1.27	0.343	4608	High current density at source side.
Pix. 6		Octagon	0.52	W_{Ave}:3.78 W_S/W_D:5.51/2.06	7.27	1.968	4608	Without STI

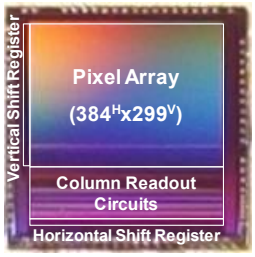

Fig. 3. Array test chip micrograph.

Table 2
Array test chip design specifications.

Technology	1P5M 0.18μm CMOS with Pinned Photodiode
Die Size	4800μm^H × 4800μm^V
Pixel Size	10μm^H × 10μm^V
Number of Pixels	384^H × 299^V Pixels

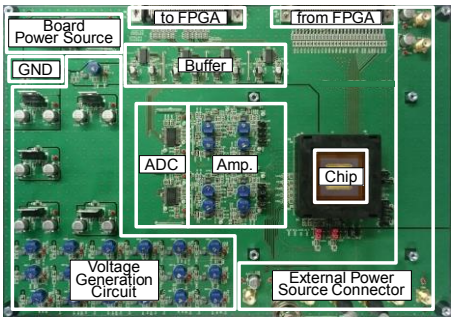

Fig. 4. Picture of measurement board.

RESULTS AND DISCUSSIONS

Fig. 5 shows the measured I_{DS}-V_{GS} characteristics of SF transistors used for Pix. 1~6. Here, typical transistors prepared on the wafer were measured. These are buried channel transistors, which is effective for reducing RTN[3]. In this graph, it is clear that the transistors with special shapes draw I_{DS}-V_{GS} curves differently from the normal (rectangular) transistors. The threshold voltages are negative due to the buried channel structure[3]. Table 3 shows the subthreshold swing factors (SS) and the SF gains of these transistors. For the trapezoidal transistors, there is a clear difference of the SS between the transistors with larger or smaller gate width at the source side. SS is the smallest in Pix. 6.

Fig. 6 shows the cumulative probability of V_{RMS} in the Gumbel plot. In this graph, the cumulative probability is calculated by 4608 pixels in the array test circuit and V_{RMS} is defined as the root mean square when output signals of each pixel are sampled for 100000 points at 1μs period. The output voltages were 1.9 V for each type of transistor. In Fig. 6(a), the measured results of transistors with different gate widths under constant drain current (1.0 μA) are shown. Under the constant drain current, the distribution of V_{RMS} is smaller for larger gate width. In Fig. 6(b), a comparison between the rectangular and octagonal transistors with nearly equal gate area under the drain current at 0.1 μA and 1.0 μA is shown. From the results, the appearance probability of RTN in octagonal transistors is less than the rectangular transistors with almost the same gate area under each drain current. Fig. 6(c) shows a comparison between the two trapezoidal transistors under the constant drain current density. The result shows that the trapezoidal transistors with the larger gate width at the source side tend to exhibit larger V_{RMS} values than the transistors with the smaller gate width at the source side.

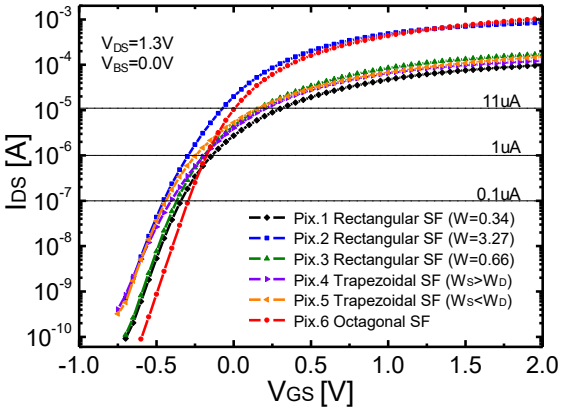

Fig. 5. I_{DS}-V_{GS} characteristics of SF transistors.

Table 3
Subthreshold swing factors and SF gains of transistors in Fig. 5.

Sample Names			SS (mV/decade)	SF gain
◆	Pix. 1	Rectangular SF (W=0.34)	118	0.84
■	Pix. 2	Rectangular SF (W=3.27)	112	0.84
▲	Pix. 3	Rectangular SF (W=0.66)	111	0.84
▶	Pix. 4	Trapezoidal SF (W_S>W_D)	141	0.83
◀	Pix. 5	Trapezoidal SF (W_S<W_D)	118	0.80
●	Pix. 6	Octagonal SF	100	0.84

- Subthreshold swing factors were extracted at a drain current range from 10^{-9} A to 10^{-7} A.
- SF gains were extracted at V_{DS}=1.3 V and I_{DS}=15 μA.

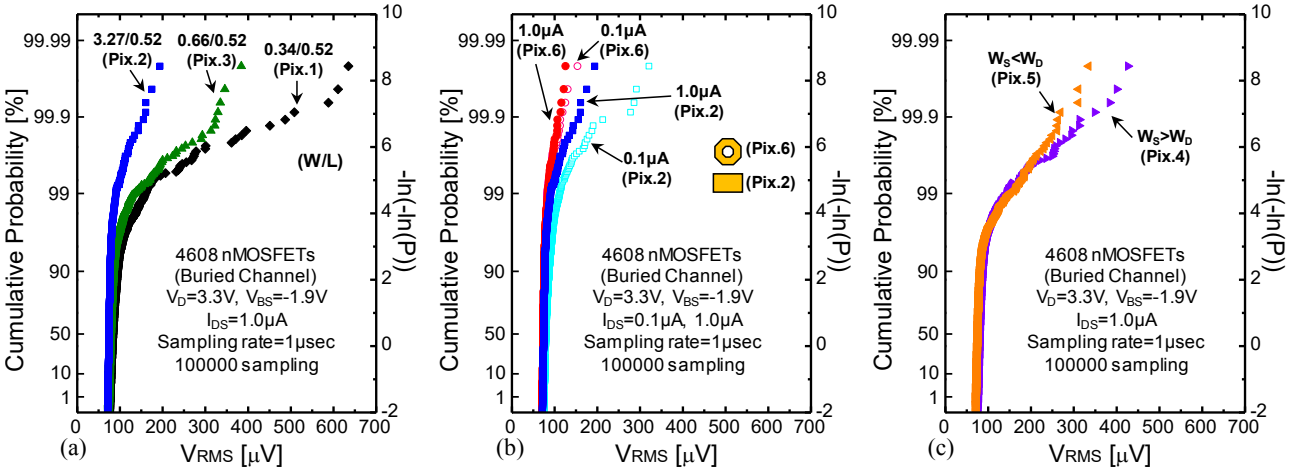

Fig. 6. Cumulative probability of the V_{RMS}. (a) Comparison of different gate width under constant drain current (I_{DS} = 1.0 μA), (b) Comparison between rectangular transistors and octagonal transistor with nearly equal gate area (I_{DS} = 1.0 μA, 0.1 μA), (c) Comparison between trapezoidal transistors under constant drain current (I_{DS} = 1.0 μA). The output voltages were at 1.9 V for each type of transistors.

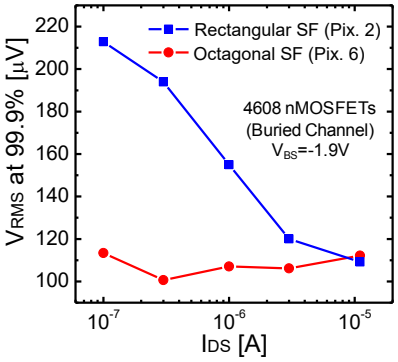

Fig. 7. V_{RMS} values at cumulative probability of 99.9% as a function of drain current (Pix. 2 and Pix. 6).

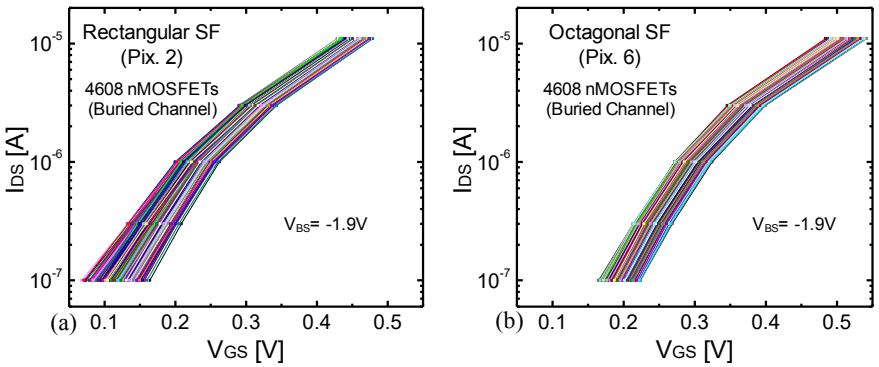

Fig. 8. I_{DS}-V_{GS} characteristics of all evaluated transistors (4608 pixels). (a) Rectangular transistors (Pix. 2), (b) Octagonal transistors (Pix. 6). The output voltages were at 1.9 V for each type of transistor.

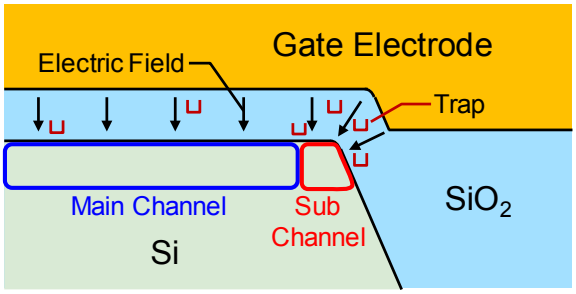

Fig. 9. The effect of parasitic transistor due to the sub-channel formed by electric field concentration around STI edge.

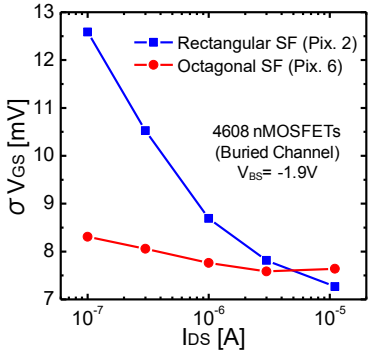

Fig. 10. Standard deviation of V_{GS} as a function of drain current (Pix. 2 and Pix. 6).

Fig. 7 shows V_{RMS} values of rectangular and octagonal transistors at the cumulative probability of 99.9% as a function of drain current. When the drain current is large, both V_{RMS}s are nearly equal. On the other hand, as the drain current becomes smaller, the V_{RMS} becomes larger in the rectangular transistors. Fig. 8 shows 4608 I_{DS}-V_{GS} curves of rectangular and octagonal transistors, respectively. The output voltages were at 1.9 V for each type of transistors. It is clear that for the octagonal transistors, the variation of V_{GS} at low drain current is smaller and the slopes of I_{DS}-V_{GS} curves in sub-threshold region is higher than those of the rectangular transistors. Furthermore, comparing Fig. 8(a) with (b) and from the I_{DS}-V_{GS} curves of Fig. 2, the drain current is larger in the rectangular transistors than the octagonal transistors at low V_{GS}. This is because, as shown in Fig. 9, when the V_{GS} is low in the rectangular transistors, the effect of the parasitic transistor due to the sub-channel formed by electric field concentration around the STI edge are greater. Fig. 10 shows the standard deviation of V_{GS} in the rectangular and the octagonal transistors as a function of the drain current. When the drain current becomes smaller, the σV_{GS} becomes larger in rectangular transistors, whereas it

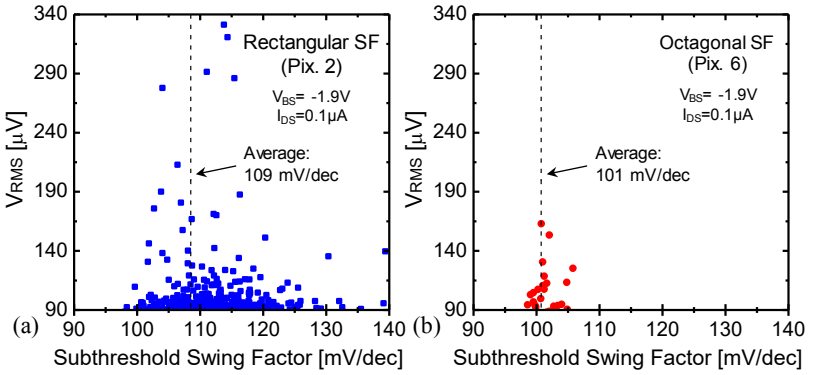

Fig. 11. Correlation between V_{RMS} and SS for (a) rectangular transistors (Pix. 2), (b) octagonal transistors (Pix. 6).

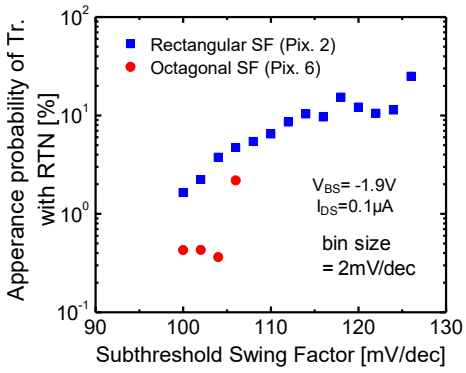

Fig. 12. Appearance probability of transistors with RTN as a function of SS.

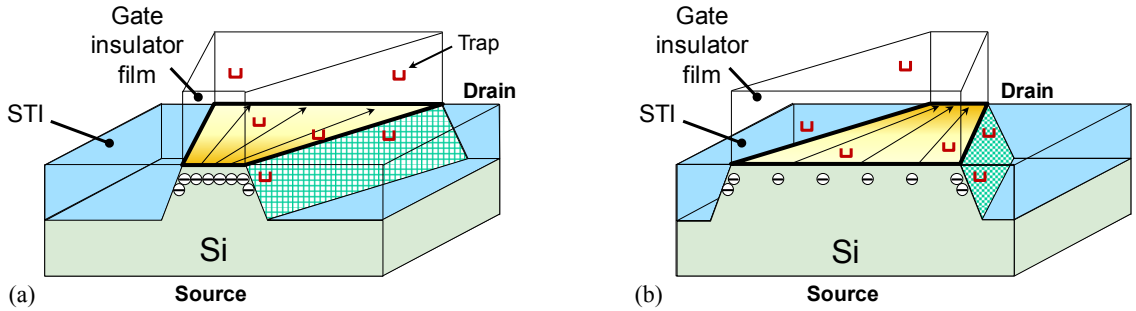

Fig. 13. Cross sectional views of trapezoidal transistors. (a) Trapezoidal transistor with shorter gate width at source side, (b) Trapezoidal transistor with longer gate width at source side.

does not change very much in octagonal transistors. Therefore, the transistor structure which does not have the influence of STI edge in the channel carriers is effective for reducing the threshold voltage variation. Fig. 11 shows the correlation between V_{RMS} and SS for the rectangular and the octagonal transistors, respectively. SS was extracted at current range of 10^{-7} A to 10^{-6} A. Here, the SS of transistors with V_{RMS} higher 90 μV showing RTN signals were plotted. It is clear that pixels where RTN is observed are often found in an area larger than the average SS value indicated by dotted lines in this figure. The obtained result shows that transistors with large SS lead to large V_{RMS}[8] in rectangular and octagonal transistors. Fig. 12 shows the appearance probability of transistors with RTN, defined by V_{RMS} of more than 90 μV as a function of the segmented SS regions for rectangular and octagonal transistors. Here, the bin size of SS was taken at 2 mV/decade. It is clear that when SS becomes larger, the appearance probability of transistors with large V_{RMS} becomes higher[8]. Comparing these two types of transistors, there are large SS values in rectangular transistors. It shows that the percolation of channel occurs due to the STI edge. Furthermore, the result suggests that the trap density at the STI edge is higher than that at the gate insulator film on main channel because the appearance probability of octagonal transistors is smaller than that of rectangular transistors at the same range of SS.

Fig. 13 shows the cross sectional views of the trapezoidal transistors. Comparing (a) with (b), the transistors with narrow gate width at source side induce higher carrier density at source side than transistors with narrow gate width at drain side under constant drain current operation. For this reason and from the distribution in Fig. 6(c), it is considered that the increase of current density at source side is effective for reducing RTN because the traps near source side are more influential to the RTN appearance probability[7], and higher drain current density operation reduces the effect of the parasitic transistor due to the sub-channel formed by electric field concentration around the STI edge.

CONCLUSION

In this paper, by evaluating the array test circuit with various shapes of SF transistors in pixels of a CMOS image sensor, it was demonstrated that transistor without STI edge is effective for reducing RTN because of the suppression of generating percolated channel around STI edge where the trap density is likely to be high. It was also shown that increasing carrier density at source side of the channel is effective to reduce RTN. These findings are important to the design of in-pixel SF transistors with small RTN for low noise CMOS image sensors.

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