Development of Low Noise Memory Node in a 2.8um Global Shutter Pixel with Dual Transfer

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***Abstract*— This paper describes a design of a storage-gate based memory node for low dark current in a 2.8um global shutter pixel with dual transfer. P-type implants and negative gate biasing are introduced to suppress generation of dark current at the surface of the memory node. Our developed memory node structure shows the world smallest dark current of 9.5ele/s at 60 degrees C.**

Introduction

Global Shutter (GS) pixels with smaller pitch below 4um are demanded for high quality images in industrial and automotive applications [1]. For small GS pixel, dual transfer GS pixels are suitable in the points of scalability, low read noise and low dark current. Their fewer components in pixels offer a better scalability compared to 8T voltage domain pixels [2]. In the dual transfer GS pixels, photo-generated charges are transferred to additional memory node. This allows a correlated double sampling (CDS) on a floating diffusion in the successive transfer, which can reduce pixel noise dramatically to below 1-2 electrons [3-5]. This read noise is much better than that of 5T charge transfer pixels without CDS [6]. Additionally such memory node shows much smaller dark current compared to a floating diffusion used as a memory node in the 5T-GS pixels [7].

As regards the memory node (MN) in the dual transfer GS pixels, a pinned memory node and a storage-gate based memory node have been reported [5, 7]. In the storage-gate based MN shown in Fig. 1, the storage-gate can control the depletion potential of the memory node. This offers better charge transfer from the photodiode to the memory node. Furthermore, using the same poly-Si gate as both a transfer gate and a storage gate can enhance potential controllability by its larger gate area. It makes the storage-gate based MN suitable for small GS pixels. Although the reported dark current of the storage-gate based MN is higher than that of the pinned MN due to dark current at the surface of the MN [5], its potential controllability can also improve dark current combined with negative gate biasing.

This paper reports on newly developed storage-gate based MN structures to drastically suppress dark current with negative gate biasing and surface p-type implants. The generation position of dark current identified by the test structures is also described.

Pixel Structure

The pixel was designed in 110nm node process for cmos image sensors (CIS) with dual micro-lens and W-shield [8]. Figure 2 shows the schematic diagram of pixel circuit and timing diagram. In order to increase the photodiode area and MN area, we used a 2x1 sharing scheme. The pixel has no row-select and the floating diffusion drive method is used [9]. TX1 is served as both a transfer gate from the photodiode to MN and a storage-gate over MN to reduce the control line for the storage-gate. TX1 and TX2 consist of n-type poly-Si gates for better charge transfer due to its low threshold voltages for TX1 and TX2. During the integration time of MN, TX1 and TX2 are kept negative bias for suppressing dark current, where accumulated holes at the surface occupy recombination centers and prevent carrier generation [7]. The fabricated pixel is shown in Fig. 3.

Development of Low Noise MN Structures

Figure 4(a) shows a conventional MN without p-type implants and its schematic potential diagram, and Figure 4(b) shows these of a proposed MN. In the conventional MN, the negative gate biasing can only accumulate hole weakly under poly-Si gates due to an n-type layer in the MN in the range of the negative voltage allowed by CIS operation. This causes larger V_{TX1} dependence of accumulated hole concentration and results in higher V_{TX1} dependence of dark current. And also the n-type layer in the MN prevents the formation of the hole accumulation layer under a gap between TX1 and TX2. These two factors are the major factors of dark current generation in the conventional MN.

The proposed MN has p-type implants both under the poly-Si gates and under the gap in order to accumulate hole at the surface with negative gate biasing. The surface p-type implant makes a threshold voltage of the MN higher and hole accumulation well with the negative gate biasing, and then stabilize V_{TX1} dependence of dark current. High p-type concentration of the gap p-type implant is required to accumulate hole under the gap because of less effectiveness of negative gate biasing in the region not under the poly-Si gates. Maximum P-type dosage for the gap implant should be determined considering the full well capacity and charge transfers.

For evaluating dark current of the proposed MN, we examined three MN structures for 2.8um GS pixels. One is the proposed MN and the rest two structures illustrated in Fig. 5 are test structures to identify generation positions of dark current. One of the test structures is the MN with only the surface-implant. The other of the test structures is the MN with only the gap-implant. Process flow is shown in Fig. 5(c). The gap p-type layer was formed by implantation in a self-aligned manner through TX1 and TX2 poly-Si gates. Low thermal budget after the gap implant results in shallow p-type profile. This allows usage of higher dosage for the gap-implant as required.

All three MNs were designed to satisfy targets of the full well capacity and image lag at the MN. Simulation results of hole concentration at the surface under the poly-Si gate and under the gap in the test structures are shown in Fig. 6. The gap-implanted MN has a higher hole concentration under the gap than that of the surface-implanted MN as expected. Little V_{TX1}=V_{TX2} dependence of hole concentration of the gap-implanted MN under the gap also indicates well-accumulated hole region under the gap in this MN. The hole concentration under the poly-Si gate in the surface-implanted MN shows smaller V_{TX1} dependence and higher hole concentration than these of the gap-implanted MN. It is expected to be smaller V_{TX1} dependence of dark current in the surface-implanted MN.

Experimental Results

Figure 7 shows the measured dark currents of developed MNs. The dark currents of our developed MNs are suppressed to 1/10 at 60 degrees C compared to the conventional MN without p-type implants when the full well capacities of the MNs are the same. The dark currents of the surface-implanted MN, the gap-implanted MN and the proposed MN at V_{TX1}=mid are 24.1ele/s, 12.9ele/s and 9.5ele/s, respectively. Figure 8 shows V_{TX1}=V_{TX2} dependence of dark current of each MN. Thanks to p-type implants, the dark currents of the newly developed MNs are smaller than that of the conventional MN in a measured range of V_{TX1}.

The dark current of the gap-implanted MN at V_{TX1}=high is higher than that of the surface-implanted MN. Comparing calculated hole concentration under the poly-Si gate shown in Fig. 6, this difference of the dark current comes from the surface under the poly-Si gate. This indicates negative bias is not enough for suppressing the gate voltage dependence of dark current and the p-type surface implant is required to stabilize the dark current in the storage-gated MN as expected.

At V_{TX1}=mid, the dark current of the gap-implanted MN is smaller than that of the surface implanted MN. This is because after accumulating holes enough under the poly-Si gate with low V_{TX1}, the carrier generation under the gap dominates dark current.

Figure 9 shows cumulative probabilities of dark current at V_{TX1}=mid and V_{TX1}=high. Only 0.1% potion of pixels in the gap-implanted MNs have dark current higher than 300ele/s at V_{TX1}=mid. Little V_{TX1} dependence of dark current of the proposed MN is clearly seen comparing cumulative probabilities of each MN. The generation position of dark current is again confirmed by comparing the cumulative probabilities at V_{TX1}=mid. The proposed MN and the gap-implanted MN has similar distribution. On the other hand, the surface-implanted MN has larger population of dark current over 20ele/s. Considering difference of implanted p-type layers, these outliers come from the surface under the gap.

Conclusion

To realize low noise small GS pixel, we analyzed and developed new MN structures. We verified high hole concentration under the gap between TX1-TX2 poly-Si gates is required to suppress dark current of the MN. Table 1 contains a list of pixel performance of the newly developed 2.8um GS pixel. Our developed MN structure shows the world smallest dark current of 9.5ele/s at 60 degrees C.

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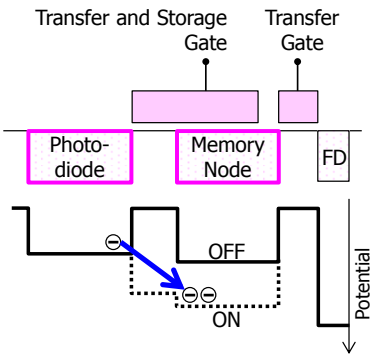

Figure 1 Schematic and potential diagram of storage-gate based memory node.

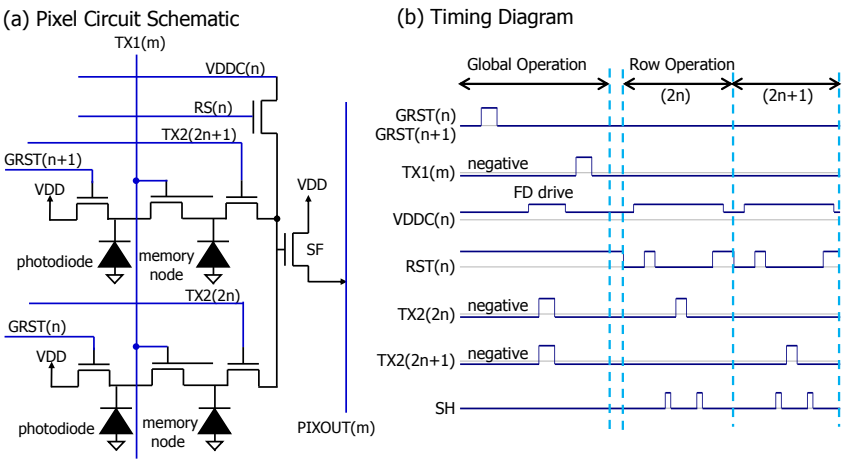

Figure 2 (a) Pixel circuit schematic and (b) timing diagram.

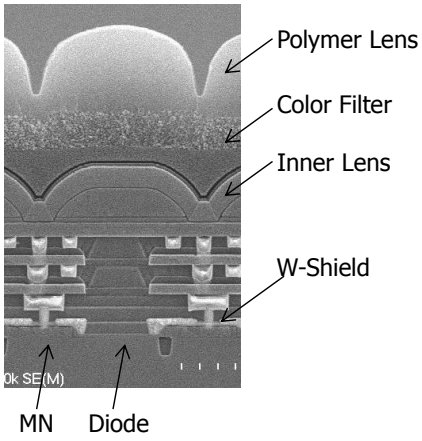

Figure 3 Cross-sectional view of developed 2.8um GS pixel.

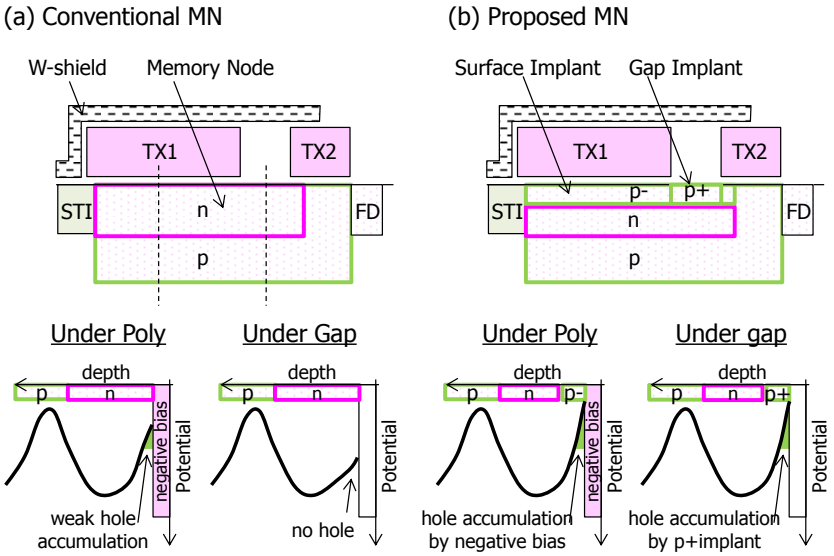

Figure 4 (a) Conventional and (b) proposed MN. Schematic (top) and potential diagram (bottom). Potential diagrams shown are these along dots lines in (a).

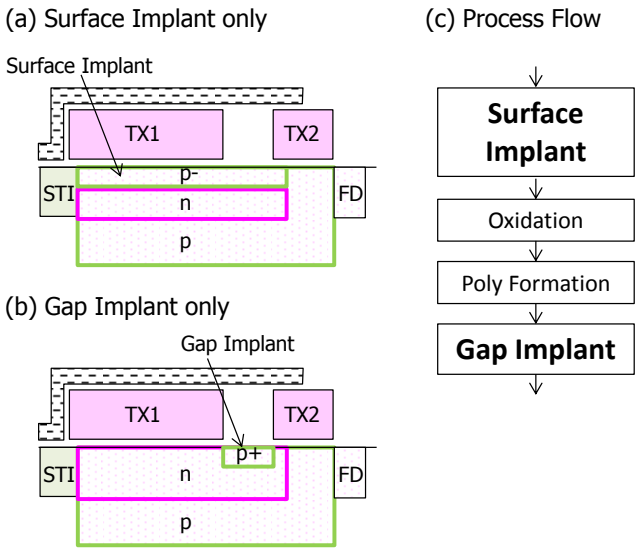

Figure 5 Test structures of the memory nodes for P-type implants and process flow.

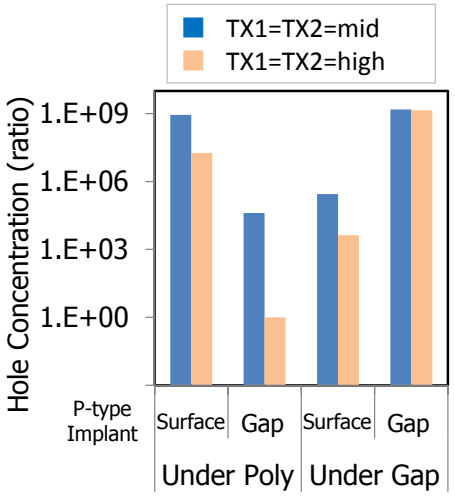

Figure 6 P-type implants and V_{TX1} dependencies of hole concentration at the surface of Si.

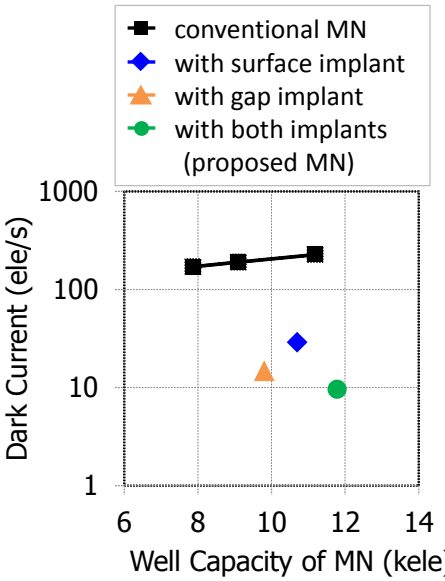

Figure 7 Relationships between well capacity and dark current of MN at 60 degrees C.

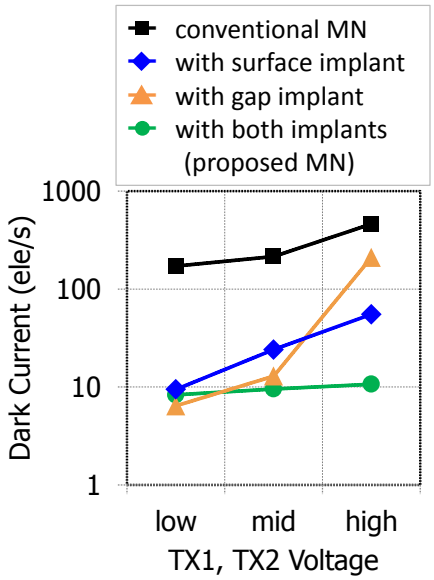

Figure 8 V_{TX1} dependencies of dark current of MN at 60 degrees C.

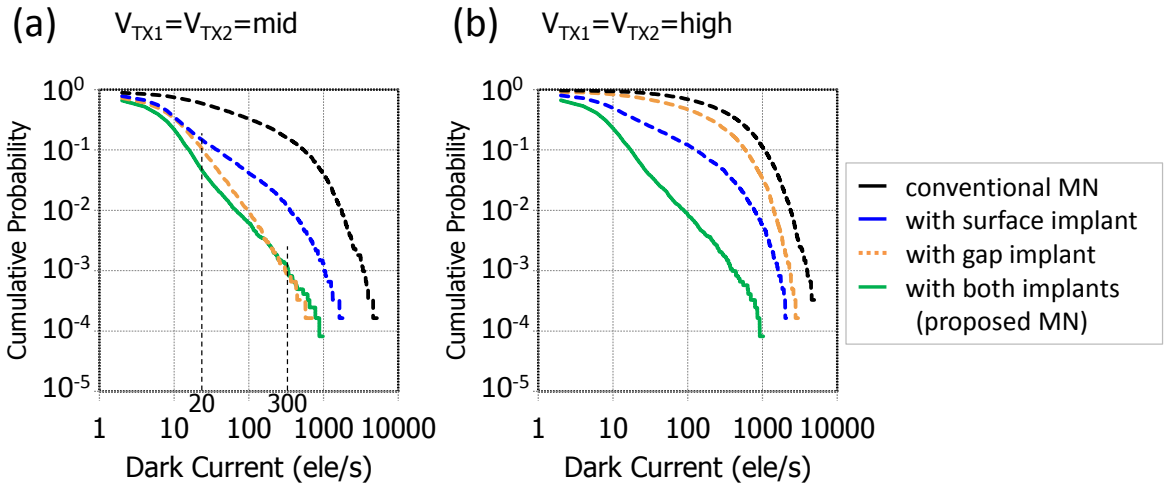

Figure 9 Cumulative probabilities of dark current of the developed memory nodes with (a) V_{TX1}=V_{TX2}=mid and (b) V_{TX1}=V_{TX2}=high at 60 degrees C.

Table 1 Pixel performance table of developed 2.8um GS pixel.

	This Work	[5]	Unit
Process Node	110nm CIS	-	-
Pixel Pitch	2.8um	2.8um	-
Linear Qsat	7	6	kele
Dark Current @PD, 60°C	14	-	ele/s
Dark Current @MN, 60°C	9.5	60	ele/s
Image Lag	none	-	ele
Pixel Noise@10fps	120	-	uV