1.0um pixel improvements with hybrid bond stacking technology

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Abstract

In this work, Omnivision's second-generation (Gen2), 1.0um CMOS image-sensor technology is presented. The key features of this Gen2 technology are hybrid-bond (HB) stacking, backside deep trench isolation (BS-DTI), a new backside composite metal-oxide grid (CMG), and improved gate oxide quality. The Gen2, 1.0-um pixel products achieve 20% higher full well capacitance, 12.5% higher sensitivity, 10-lux lower SNR10, 2x lower RTS noise and a 10% reduction in chip size. Results are demonstration on 16- and 20-MP array products.

Introduction

The first generation, stacked chip technology used oxide-oxide bonding and through-silicon vias to physically bond and electrically connect the sensor and logic wafers, respectively. With stacking technology, the logic circuitry is placed under the array, resulting in an overall smaller chip size than is possible with standard BSI-CIS; where the circuit is located on the same wafer. Stacking also allows for sensor-only processes that improve CIS performance which could have negative impacts on circuit performance in a BSI-only process, such as extra thermal steps, new materials, or gate-oxide optimization. In addition to the benefits that stacking offered, the first generation products further improved image quality with a buried color filter array and a tungsten BS-DTI, as detailed in Ref 1.

Gen2 architecture

The second generation, stacked chip technologies uses hybrid bonding, where wafers-to-wafer bonding occurs at both the oxide and metal interfaces, and water-to-wafer interconnection is made at the top metal bonding pad (Fig.1). This architecture offers a better interconnect pitch and more flexible interconnect placement than the previous Gen1 approach. For instance, bonding can occur closer to the array edge, or even within the array, as illustrated in Fig.1b. As a result, the overall chip size is significantly reduced using HB technology. The Gen2 1.0um, 16MP product achieves a 10% smaller chip size than the Gen1 product of the same pixel and array size.

In the Gen2 technology, the BS-DTI and BCFA are extended to further improve the CIS optical performance. Figure 2 compares the Gen1 and Gen2 BSI stack. The BS-DTI is deeper, with a narrower width, allowing for an increase in silicon thickness without degrading pixel-to-pixel crosstalk or electrical blooming. The increased silicon thickness and narrower BS-DTI width increases the light collection volume. In Gen2, the backside metal grid is replaced with a new metal-oxide composite grid design. The smaller grid width and light-guide features of the CMG aid in light collection (Ref.2). The gate-oxide and surface passivation are improved in the Gen2 sensor technology for improved source follower noise.

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Results

Figure 3a compares the quantum efficiency and angular response of the Gen1 and Gen2 technologies on 1.0-um, 16MP Omnivision products. The green and red peak QE increases 10% using the Gen2 optical stack, due to the CMG light-guide effect and large light collection volume. The deeper BS-DTI maintains a low optical cross talk and good angular response, Fig.3b. The higher QE and low cross talk improve the SNR10 by 10lux (table 1). The low light (5lux)

performance of the Gen2 and Gen2 technologies is compare in Fig. 4. Figure 5 shows the noise histogram of a Gen2 and Gen1, 1.0um pixel product. The Gen2 RTS noise is improved 2x over the same pixel design using the Gen1 technology; listed in Table1. A summary of performance parameters comparing the Gen2 and Gen1 technologies is shown in table 1. The Gen2 technology achieve 20% higher full well capacitance, 12.5% higher sensitivity, 10lux lower SNR10, 2x lower RTS noise and a 10% reduction in chip size.

Summary

Omnivision's second generation, 1.0um CMOS image-sensor technology features a hybrid bond stacking process and improved optical stack to achieve best in class performance while maintaining low cost (chip size). This technology is used in 1.0um, 16MP and 20MP CIS product designs and is also extended to 0.9um pixels.

References

1. V.C. Venezia et al, Stack Chip Technology: A New Direction for CMOS Imagers, Proc. IISW, 2015
2. Chi Han_Lin et al, 1.1um Back-Side Illuminated Image Sensor Performance Improvement, Proc. IISW, 2013

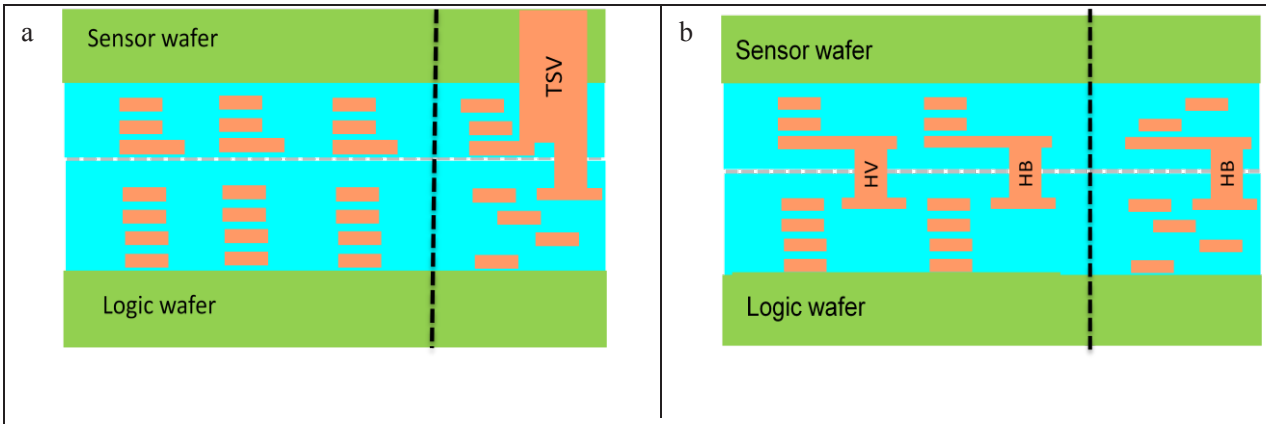

Figure 1 Schematic comparing (a) Gen1 stacking - oxide to oxide wafer bonding with TSV wafer interconnections outside the array and (b) Gen2 hybrid bond (HB) stacking with wafer connections within and outside the array

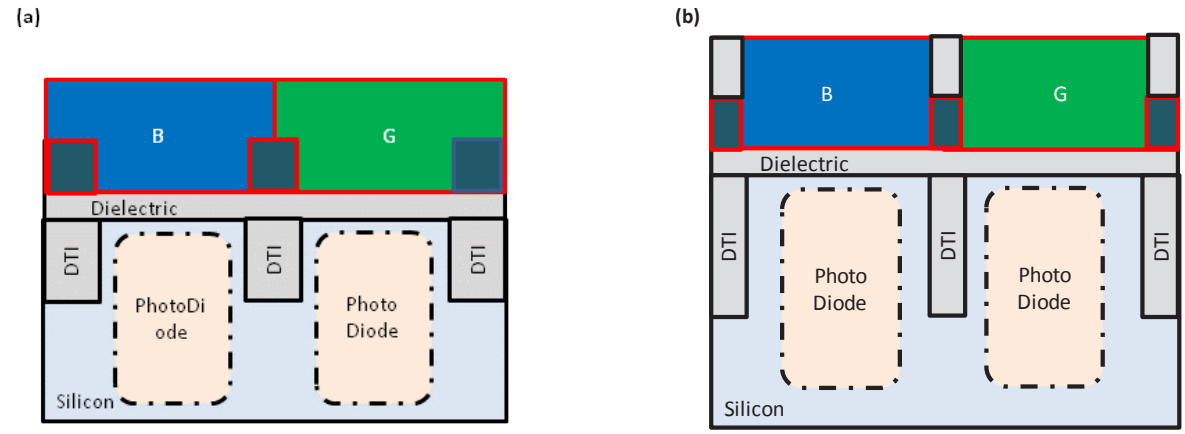

Figure 2 (a) Gen1 BSI stack (b) Gen2 BSI stack schematic; illustrating the Gen2 BSI stack has thicker silicon, deeper back side DTI, narrower DTI width and a composite metal-oxide backside grid.

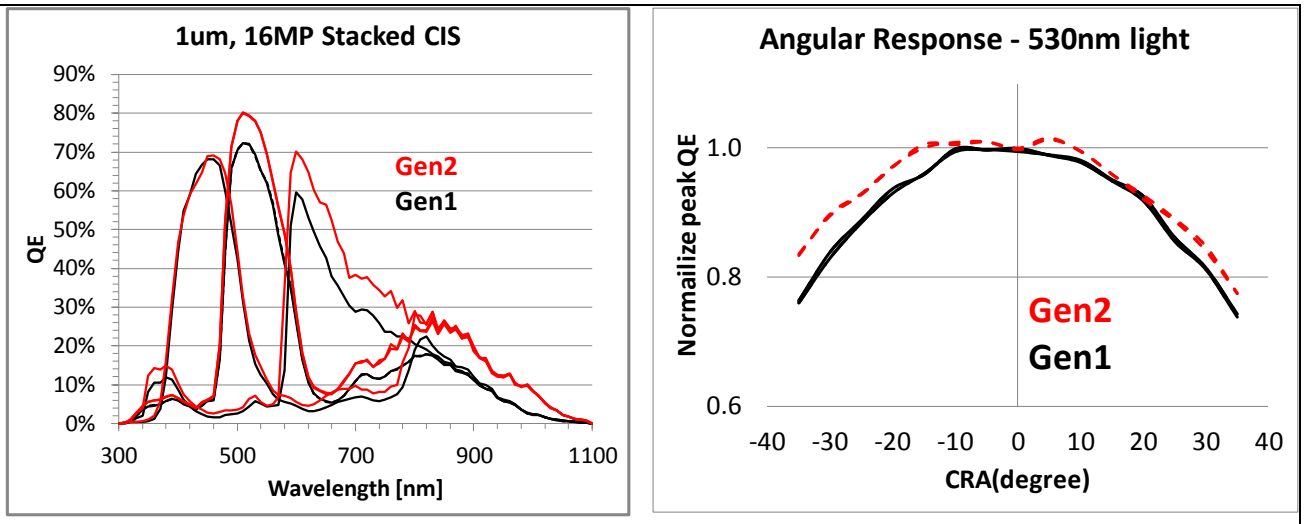

Figure 3 (a) QE and (b) sensitivity vs angle (normalized) comparing Gen1 and Gen2 1um, 16MP

Parameter	Units	Gen1	Gen2
Array		16MP	16MP
Pixel size	um	1.0	1.0
Full Well Capacity	e-	5000	6000
Sens - G (530nm)	e-/Lux.s	3150	3600
PRNU	%	0.8	0.8
SNR10	Lux	90	80
White pixel (T=60C)	ppm	300	200
Dark current (T=60C)	e-/s	4	2
Blooming	%	0%	0%
FPN	[e]	0.5	0.2
Read noise (16x gain)	[e]	2.0	1.4
RTS	ppm	500	200

Table 1. Key performance parameters for 1.0um, 16MP CIS using Gen1 and Gen2 technologies.

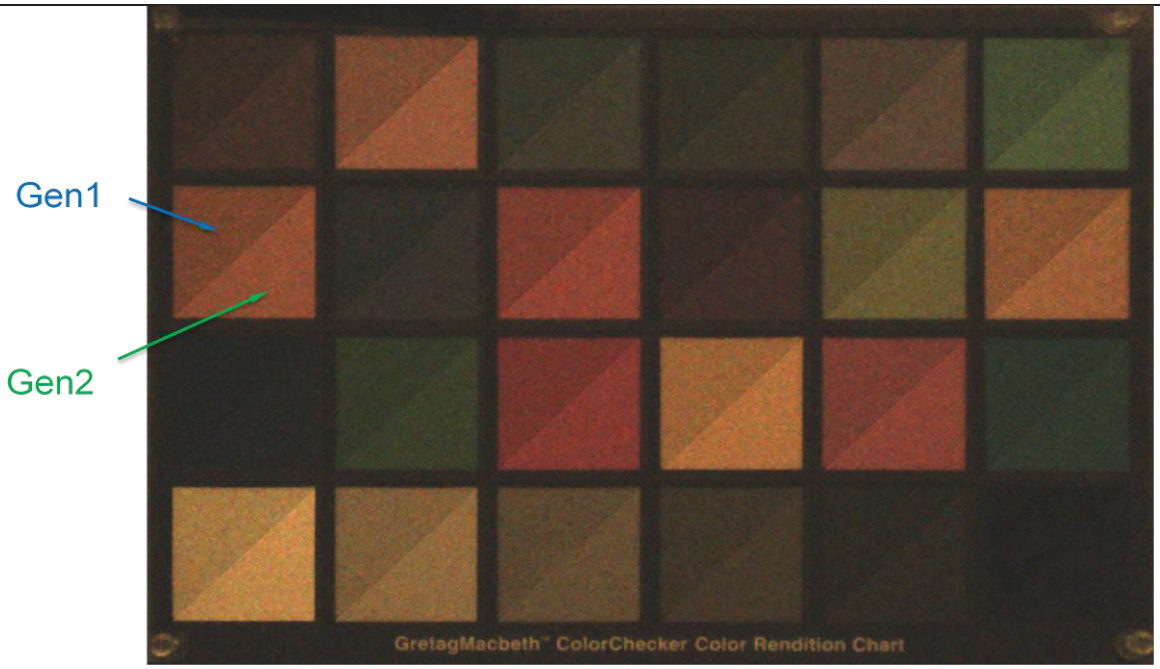

Figure 4. Gen-1/Gen-2 image comparison at 5 lux

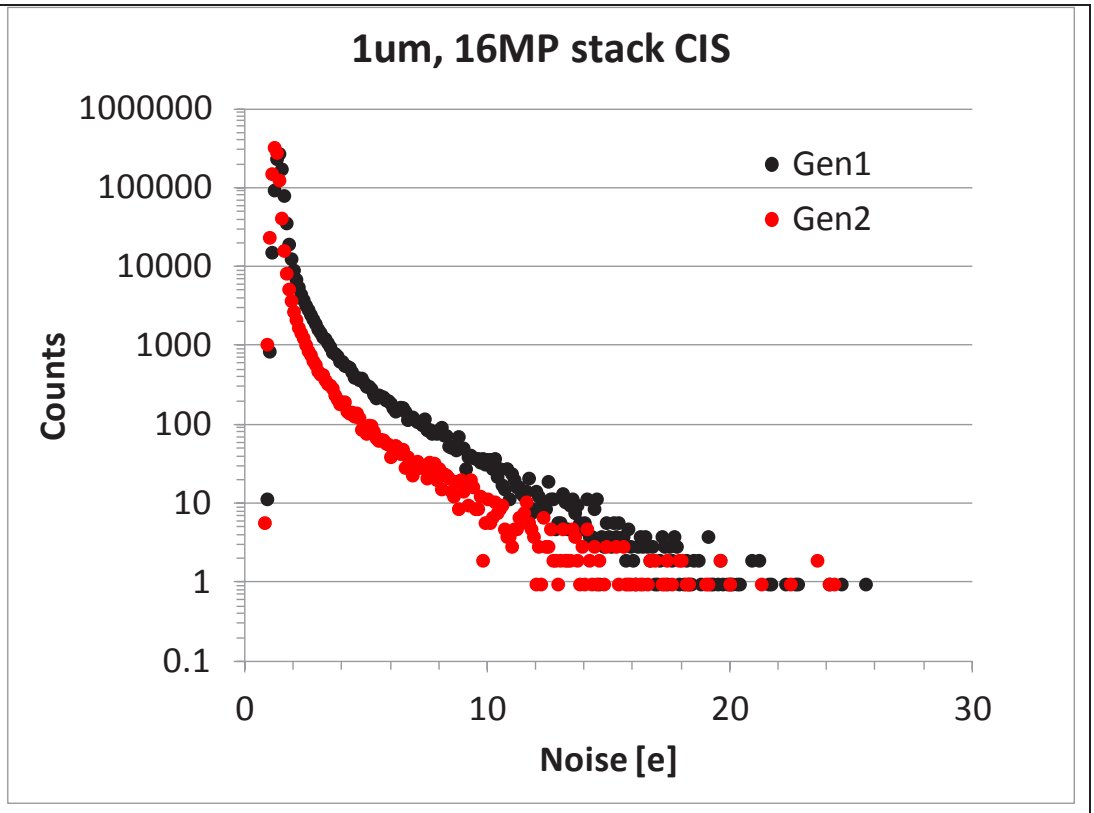

Figure 5. Noise histogram comparing the 1um, 16MP Gen1 and Gen2 process.