Three-transistor-pixel CMOS image sensor for 8K Super Hi-Vision stacked sensor with highly sensitive photoconversion layer

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***Abstract*—In a high-definition, high-frame-frequency CMOS image sensor for an 8K 120-Hz SHV camera system, the reduced pixel size of the sensor decreases the amount of light received per pixel, which degrades its sensitivity. Therefore, we have been researching and developing a CMOS image sensor overlaid with a photoconversion layer that can multiply signals to enhance its sensitivity. Because the pixels of this sensor are composed of three transistors, it is difficult to reduce the random noise compared to when using a conventional sensor with four-transistor pixels. In this study, the random noise characteristics and the noise reduction effect of digital correlated double sampling (CDS) were measured and evaluated by using a test chip, and the 33-Mpixel 8K SHV CMOS image sensor for a stacked sensor was designed on the basis of the evaluation results of the test chip.**

Keywords—photoconversion layer, stacked sensor, CMOS image sensor, 8K SHV, noise, CDS

I. INTRODUCTION

The demand for highly realistic video systems that improve viewing experience by conveying a "sense of being there" and "sensation of realness" through higher definition and higher frame frequency pictures has been increasing recently[1][2]. In the image sensor for the system, the required pixel size and storage period of the photogenerated charges has been decreasing as the number of pixels and frame frequency increases, which results in degrading the sensitivity. Therefore, technology to enhance the sensitivity of the image sensor of the system is highly desirable. To meet this demand, we have been researching and developing a 33-Mpixel 120-Hz 8K Super Hi-Vision (SHV) stacked sensor overlaid with a highly sensitive photoconversion layer. The sensor consists of a photoconversion layer in which the signal charges are multiplied in an avalanche multiplication mode[3][4] and CMOS image sensor to readout the signal charges from the layer, as shown in Fig. 1. The sensor has high sensitivity due to the multiplication function of the layer and high fill factor. To have a high signal-to-noise ratio, that is, a high image quality, it is also important to readout the signal from the layer

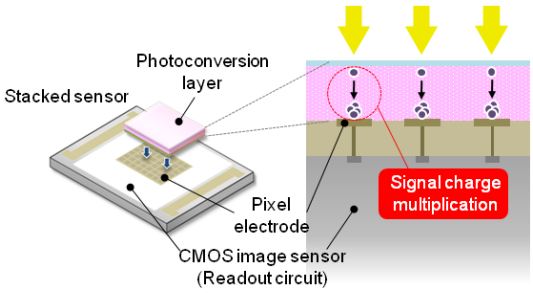

Fig. 1 Schematic diagram of stacked image sensor overlaid with photoconversion layer.

with low noise by using a CMOS image sensor that works as a readout circuit for signal charges from the layer. However, due to the typical three-transistor pixel configuration, the sensor suffers from reset noise that degrades the image quality, so a special readout technique to reduce the noise is needed. In this study, we evaluated the random noise characteristics in applying the noise reduction technique by using the test chip. Then, the 33-Mpixel 8K SHV CMOS image sensor for the stacked sensor was designed on the basis of the evaluation results of the test chip.

II. PIXEL CONFIGURATION AND SIGNAL READOUT

In the stacked sensor as shown in Fig. 1, the floating diffusion (FD) in the pixel is connected to the photoconversion layer by using a metal electrode[5], so the FD should not be fully depleted. It cannot achieve the complete charge transfer that is provided by four-transistor pixel configuration applied in a conventional CMOS image sensor. Hence, the sensor has the typical three-transistor pixel configuration consisting of a reset transistor (MR), an amplifying transistor (MA), and a select transistor (MS) as shown in Fig. 2. A source follower (SF) is composed of a load transistor (ML) arranged in each column and MA, and the signal

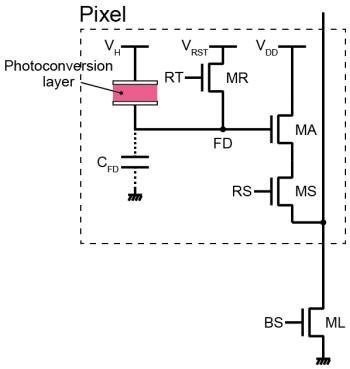

Fig. 2 Schematic diagram of pixel for stacked image sensor.

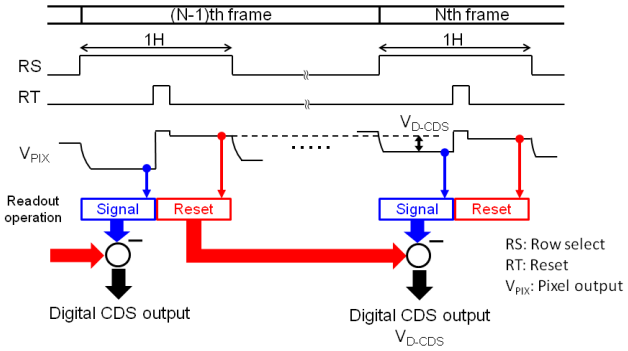

Fig. 3 Signal processing diagram of digital CDS for reducing random noise.

charges are readout into the vertical signal line as an output voltage of the SF.

In the three-transistor pixel, if the reset operation is processed in advance of the signal readout as is the case with the four-transistor pixel, the stored signal charges during one-frame period are lost. Therefore, because the reset phase follows the signal readout phase, there is no correlation between the noise included in the output in the signal readout phase and that in the reset phase in the same horizontal period, and it is difficult to reduce the reset noise by performing analog correlated double sampling (CDS) processing during one horizontal period. Hence, it is necessary to perform CDS digitally between the pixel output in the signal readout phase in the *Nth* frame and that in the reset phase in the (*N*−1)*th* frame as shown in Fig. 3. The digital CDS is subtraction processing over a two-frame period, so the frame memories for the outputs in both the signal readout phase and the reset phase are required. The ADC needs to operate twice as fast as it operates at the frame frequency because it operates twice during one horizontal period.

III. Evaluation of Noise Characteristics

The test chip was implemented in 0.18-µm 1P4M CMOS technology to evaluate the random noise characteristics and the effect of digital CDS on noise

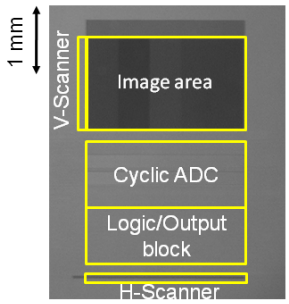

Fig. 4 Block diagram and micrograph of test chip.

reduction of the three-transistor-pixel CMOS image sensor. The sensor has an image area with 410 × 240 pixels, cyclic ADC with 12-bit resolution, horizontal and vertical scanner, and logic/output block, as shown in Fig. 4. The photoconversion layer is not overlaid on the sensor to focus on measuring the noise in the readout circuit, so the photoconversion is performed in the FD, that is, in the source layer of the MR. The pixel pitch and the column pitch are both 5.6 µm. The frame frequency can be selected to be 30, 60, or 80 Hz. The signal data is written into the frame memories to perform digital CDS processing by software.

We measured the random noise at dark as a function of frame frequency while varying the reset voltage (V_{RST}) with and without digital CDS processing, as shown in Fig. 5. Figure 6 shows the

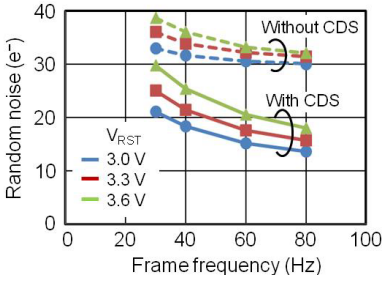

Fig. 5 Measured random noise as function of frame frequency with and without digital CDS processing.

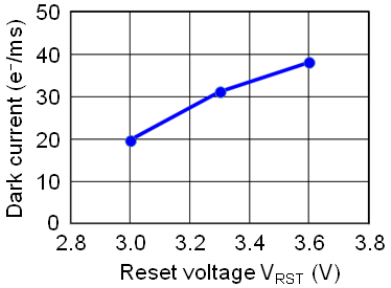

Fig. 6 Measured dark current as function of reset voltage.

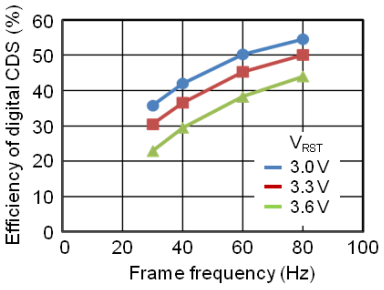

Fig. 7 Noise reduction efficiency of digital CDS as function of frame frequency.

measured dark current as a function of V_{RST}. The noise reduction efficiency of the CDS, which is defined as

$$NRE = \frac{Q_{rn\_woCDS} - Q_{rn\_wiCDS}}{Q_{rn\_woCDS}}$$

where Q_{rn_wiCDS} and Q_{rn_woCDS} are the random noise with and without the CDS respectively, is calculated, as shown in Fig. 7. The CDS reduces the random noise, but the efficiency is limited to below 60 %. The cause of this limit is the large dark current as shown in Fig. 6. The shot noise generated by the dark current degrades the correlation between the reset noise in the signal readout phase in the *Nth* frame and that in the reset phase in the (*N*−1)*th* frame.

IV. Design of 8K CMOS Image Sensor for Stacked Sensor

We have designed a 33-Mpixel 8K SHV CMOS image sensor for a stacked sensor on the basis of the evaluation results described above. One of the promising ways to reduce the dark current is lowering V_{RST} by amplifying the output of the SF. When an amplifier with a gain of G_0 is placed between the SF and the ADC, V_{RST} can be expressed as

$$V_{RST} = V_{in\_min} + \frac{V_{DR}}{\alpha}\frac{1}{G_0}$$

where V_{in_min} denotes the minimum input voltage of the SF in the range of the linear characteristics, V_{DR} denotes the dynamic range of the ADC, and α denotes the gain of the SF. Therefore, as the gain G_0 is set higher, V_{RST} can be lowered. Hence, a programmable gain amplifier (PGA) with capacitors has been designed and placed between the SF in the pixel and ADC, as shown in Fig. 8. The PGA amplifies the output of the SF in the signal readout phase and the reset phase individually to perform the digital CDS, as shown in Fig. 9. Theoretical operation of the PGA has been verified by SPICE simulation. Both amplified signals are introduced to the ADC individually, and digital CDS processing is performed. The reset noise reduction effect caused by introducing the PGA to lower the reset voltage V_{RST} is estimated roughly on the basis of the measured random noise of 15 e^- after digital CDS processing at 60 Hz and with a V_{RST} of 3V, as shown in Fig. 5. Random noise in the ADC was measured to be 3 e^-, so the reset noise of the test chip is calculated to be 14.7 e^-. If the dark current shot noise is the only noise that cannot be reduced by digital CDS, the reset noise after digital CDS processing at PGA gains of 1, 2, 3.5, and 8 is calculated as shown in Table 1. The reset noise is lowered to be 6.7 e^- at the gain of 8, which is about half of that at the gain of 1. In the standard pixel of the sensor, the transistors MA and MS are medium NMOS, that is, the threshold voltage is positive. Besides, we designed and arranged the test pixel in which the transistors MA and MS are all native NMOS, that is, threshold voltage is negative. The input-output

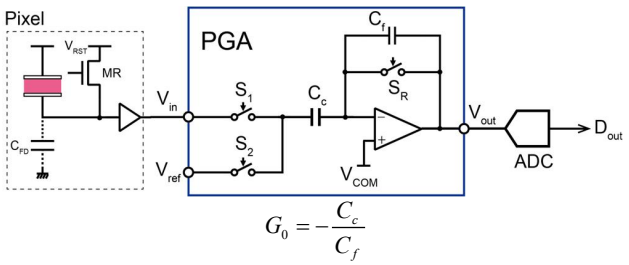

Fig. 8 Schematic diagram of PGA placed between pixel and ADC.

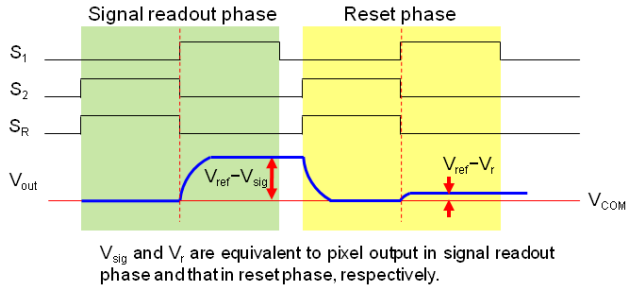

Fig. 9 Timing diagram of PGA operation.

Table 1 Estimated reset noise after digital CDS at PGA gain of 1, 2, 3.5, and 8.

PGA gain	Estimated reset noise (e^-)
1	11.9
2	8.6
3.5	7.5
8	6.7

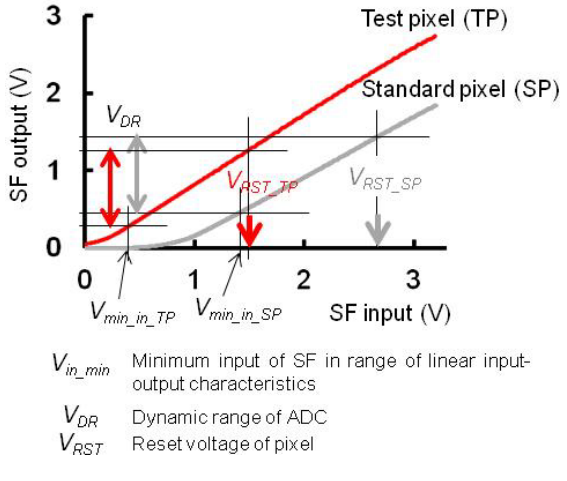

Fig. 10 Comparison between VRST of standard pixel and that of test pixel when gain of PGA is 1.

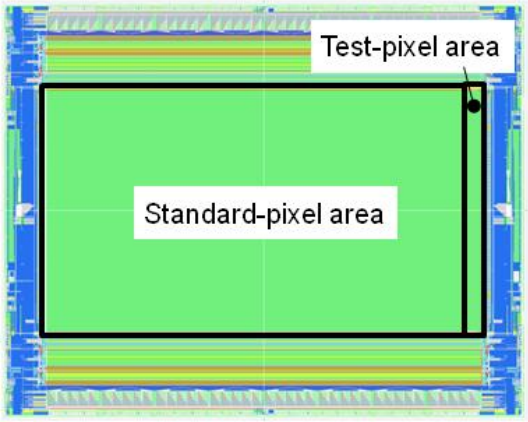

Fig. 11 Designed layout of 33-Mpixel 8K SHV CMOS image sensor.

Table 2 Specifications of designed 33-Mpixel 8K SHV CMOS image sensor.

Parameter	Value
Number of total pixels	7816 (H) × 4360 (V)
Pixel size	3.2 μm × 3.2 μm
Pixel type	3 transistors
ADC	2-stage cyclic
Resolution	12 bit
Frame frequency	60 Hz
Optical format	Super 35mm
Chip size	32 mm (H) × 25.76 mm (V)
Power consumption	3.0 W

characteristics of the SF in the test pixel move to the left side compared to those in the standard pixel, as shown in Fig. 10. Therefore, the reset voltage is further lowered as the PGA gain is set higher, which results in reduction of the dark current. Twenty-two kinds of test pixels in total with parameter variations are designed and arranged in the 208 columns at the right side of the image area. Figure 11 shows the designed layout of the 33-Mpixel 8K SHV CMOS image sensor, and its specifications are shown in Table 2.

V. SUMMARY

A CMOS image sensor with three-transistor-pixel configuration for a stacked sensor overlaid with a photoconversion layer suffers from reset noise that degrades the image quality. Therefore, we developed digital CDS processing over two frame periods and evaluated the noise reduction effect by using a test chip. The measurement results show that the CDS reduces the random noise, but the noise reduction efficiency is limited to below 60 %. The cause of this limit is the shot noise generated by the large dark current stored during one-frame period. Then, we have designed a 33-Mpixel 8K SHV CMOS image sensor for a stacked sensor on the basis of the evaluation results with the test chip. To lower the reset voltage to reduce the dark current, a PGA with capacitors has been designed and placed between the SF in the pixel and ADC. In addition to the standard pixel, 22 kinds of pixels that have parameter variations are also designed as test pixels for evaluation. Next, we are going to evaluate the dark current and random noise of the designed sensor and develop a signal readout technique for noise reduction to achieve a highly sensitive 8K SHV stacked sensor.

VI. ACKNOWLEDGMENT

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