Development of Vertical Thin Poly-Si Channel Transfer Gate Structured Pixel for 3D CIS Applications

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Abstract

This study proposes a new three-dimensional (3D) pixel transfer gate (TG) structure for CIS application, enabling the pixel to shrink towards sub-micron regime. We have fabricated two types of 3D pixels using vertical channel TG structure and verified their characteristics. Additionally, the pixel has been optimized using various control factors such as channel diffusion, junction formation between channel poly-Si and single-crystal silicon substrate, connectivity between photodiode to channel, etc. Vertical channel TG structured pixels have been realized on 5 Mpixel BSI at the 90nm technology node.

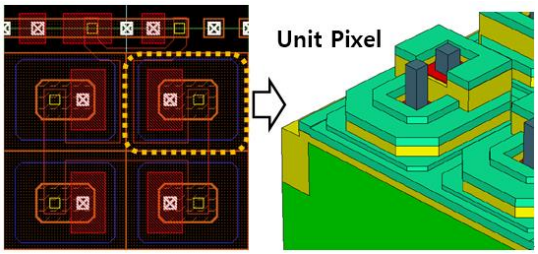
Keywords: 3D pixel, CMOS image sensor, vertical channel, poly-Si channel

Introduction

Recently, various types of 3D structures have been proposed for use in memory devices and system ICs to overcome the form factor limitations of existing 2D structures [1-3]. Research is ongoing into maximizing structure layout without incuring performance degradation. In the case of CMOS image sensors (CIS), a stacked-sensor structure is being used in which the pixel and logic are fabricated separately and then stacked with TSV technology [4-13]. However, implementing a 3D type pixel structure still needs to overcome many barriers.

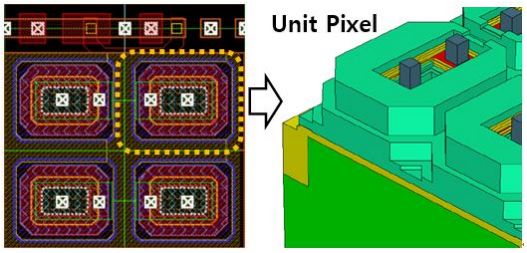
In order to cope with the continuous trend of shrinking the pixel, conventional TG requires many design optimizations to deliver products without lag or blooming but keep large full well capacity (FWC). At present, there are only a limited number of CIS manufacturing and application companies which have published their own type of high resolution 3D pixels for future CIS applications [14-20].

We propose two types of novel 3D pixel structures adopting the vertical thin poly-Si channel (VTPC) transistor structure which is widely being used in 3D NAND Flash memory devices [21]. The pixel structures use a vertical charge transfer scheme which is similar to previously presented 3D pixel structures. However, our vertical channel 3D TG pixel is the first CIS pixel design which utilizes a poly-Si channel. In this paper, we discuss two types of VTPC-TG pixels that are candidates for future 3D pixel architectures.



(a) (b)

Fig. 1. Bar type VTPC-TG pixel. (a) top view layout (b) 3D TCAD structure.



(a) (b)

Fig. 2. Donut type VTPC-TG pixel. (a) top view layout (b) 3D TCAD structure.

Novel 3D Pixel Proposal

Fig. 1 and 2 show technology computer aided design (TCAD) images of two types of novel 3D pixel structures adopting vertical poly-Si channel transistor structure. The structure was designed to improve FWC by increasing the effective PD area and to reduce image lag by enhancing TG performance. Since the TG length is defined by the vertical height of the channel, we can fully utilize PD area. Also, it is possible to increase the TG channel width, resulting in higher transfer current. We successfully fabricated two types of VTPC-TG constructed with different channel widths, one is bar type and the other is donut type, corresponding to their structural shapes. These two types of TG have different channel lengths and widths depending on their respective structures.

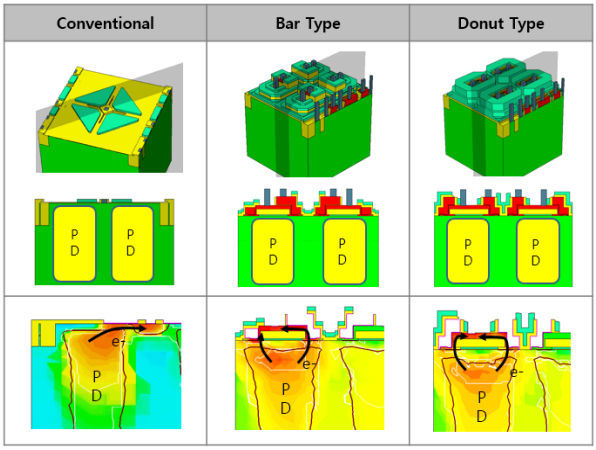


Fig. 3. 3D TCAD simulation and cross-section images of VTPC-TG pixel.

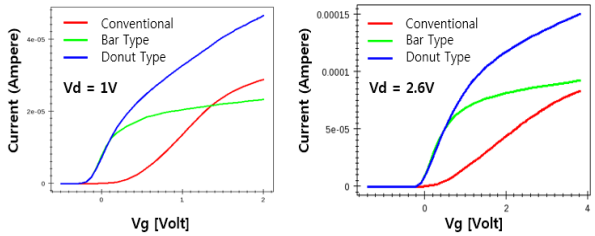


Fig. 4. Comparison of TCAD simulation results of VTPC-TG pixel. Donut type is advantageous to increase the saturation current.

As shown in Fig. 3 and 4, we verified the pixel operation for both types through 3D TCAD simulation and compared them to a conventional pixel structure.

3D VTPC-TG Structured Pixel Fabrication

Fig. 5 shows the fabrication process flow for VTPC-TG pixels. To maintain base pixel's photodiode (PD) doping profile, a unique process integration method using 5 additional masks is used. In this process flow, green color means an additional process for VTPC-TG pixel. The processing temperature for forming the VTPC-TG is minimized to prevent degradation of the characteristics of the base CIS product.

In Table I, the purpose of the additional mask steps for VTPC-TG fabrication are explained.

Table I. Additional photo masks for VTPC-TG Pixel

Add. mask	Purpose of mask step
1	Pillar oxide formation
2	Interface Ox removal between Si & Ch. Poly
3	Channel Poly patterning
4	Vertical Gate oxide formation
5	Pixel Tr. formation (TG, SG, SFG, RG)

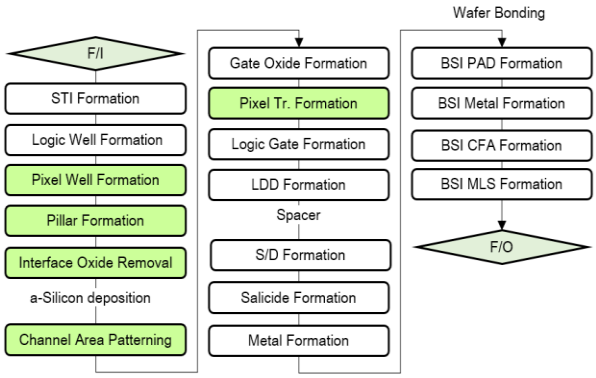


Fig. 5. VTPC-TG pixel fabrication process flow

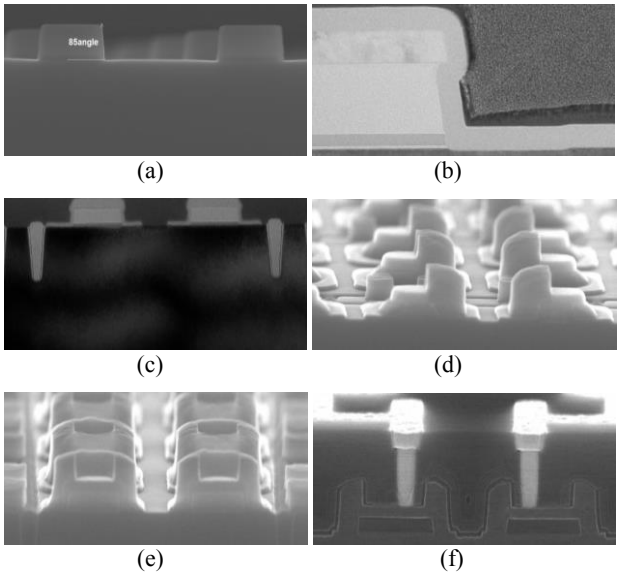


Fig. 6. SEM images of (a) after pillar formation, (b) contact point of channel poly and Si after interface oxide removal and channel poly-Si deposition, (c) after channel poly etch, (d) and (e) after TG etch step, and (f) shows the fabricated donut type pixel after Metal 1 etch. In these pictures, bar type and donut type pixels are mixed.

Fig. 6 displays the major process steps for VTPC-TG pixels. We used a process flow that is similar to 3D NAND fabrication with minor modifications for CIS pixel requirements.

Results and Discussion

To efficiently integrate VTPC-TG pixels in the base CIS process, additional processes and process changes should be minimized. Transistors characteristics should be monitored for any detrimental shifts. At the same time, to achieve adequate performance of vertical channel TG pixel, thin poly channel related process such as poly-Si thickness and doping level etc., should be also optimized. The fabricated VTPC-TGs exhibits degraded subthreshold slope characters compared to conventional TG. We believe that lower carrier mobility is attributed to grain boundaries in a thin poly channel coupled with

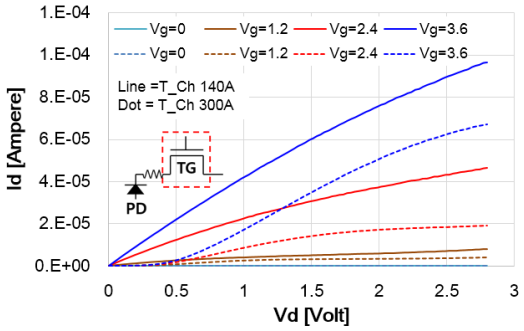


Fig. 7. Diode formation and high resistivity characteristic can be suppressed with thinner channel poly Si. Channel thickness indicates as-deposited a-Si thickness.

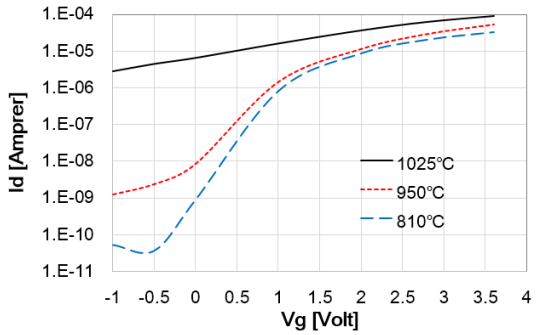


Fig. 8. Decreasing the temperature of source drain Rapid Thermal Annealing (SD-RTA) improves the leakage current because of suppressing dopant diffusion from FD region to poly-Si channel.

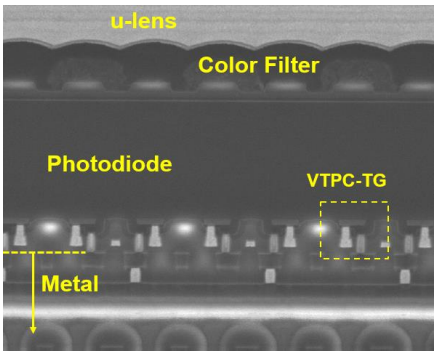


Fig. 9. Focused ion beam (FIB) cross-section of 5M BSI product. The chip used for the image acquisition is configured to u-lens, PD, VTPC-TG, and metal line from top to bottom sequentially.

an absence of the gate-all-around effect which results from the large radius of the vertical channel. Please note that we achieved better transfer performance than conventional TG structures by using 2 or 3 times wider channel width. The results of comparing VTPC-TG channel thicknesses are shown in Fig. 7. The thicker poly-Si channel leads to the delayed increase in current, indicating a parasitic diode or external resistance. However, the thinner poly-Si channel has eliminated the external diode and resistance effect, thus resulting in the higher current. This improvement is likely due to an

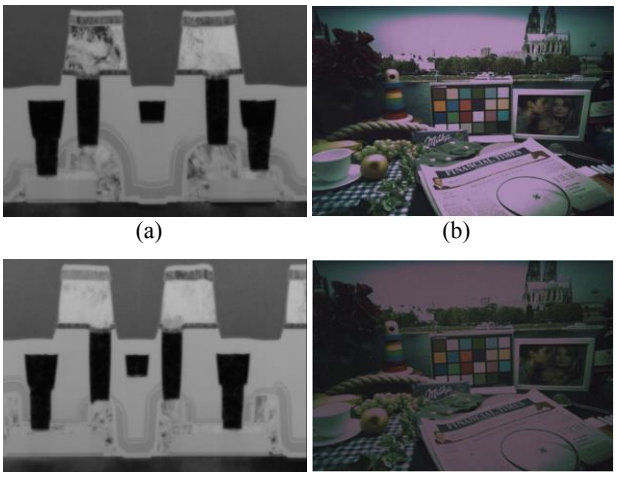


Fig. 10. (a) TEM cross-sectional view of bar type, (b) image of 5M BSI using a bar type pixel, (c) TEM cross-sectional view of donut type, (d) image of 5M BSI using a donut type pixel.

extension in the depletion region near the n-type PD area, such that the external diode or resistance effects are suppressed resulting in an ordinary I_d-V_d curve.

Fig. 8 shows the I_d-V_g characteristics of TG with respect to source/drain rapid thermal annealing (RTA) temperature. The plot indicates that source-drain punch-through can be prevented when RTA temperature is reduced. To minimize the logic transistor performance changes, the pixel source/drain implant is formed after the logic source/drain RTA step, and the pixel source-drain was formed at 950°C RTA. It is expected that further improvements to transistor characteristics will be obtained if process improvement such as a spike anneal is applied.

By adopting both of the proposed VTPC-TG pixel structures in a 5M BSI image sensor, we successfully demonstrate the feasibility of the VTPC-TG design in CIS. As part of this research we replaced the standard pixel in a 5M BSI product with the VTPG-TG architecture and compared the resultant images. Fig. 9 displays FIB images of VTPC-TG pixels applied in 5 M BSI product.

Fig. 10 shows a cross section of both types of VTPC-TG pixels that was fabricated in out 5M BSI test chip. Fig. 10 also shows the corresponding images of a test scene that each type of VTPC-TG produced. This test vehicle is based on a 5M BSI chip currently in mass production. Because this test chip is based on active product, we couldn't adjust the analog resistor's process parameters. The images in Fig. 10 are actual images obtained by interpolation and AWB without analog optimization tuning. Because the PD resistance could not be optimized and without a product design change needed for the VTPC-TG, the image was not as good as the production chip.

Nevertheless, by implementing the CIS image sensor using VTPC-TG for the first time, it verified the

possibility of using this 3D structure in the future to shrink the pixel beyond present limitations. Even though TG current of donut type is elevated, the bar type has better image quality. The difference in image quality implies that the TG current performance is not the dominant factor. Rather, we found that the quality of the picture depends more heavily on the analog chip Rs matching and defectivity in the PD interface area.

Conclusions

In this paper, we presented two types of VTPC-TG structured pixels and demonstrated a 5 Mpixel image on a proven production sensor.

A vertical channel TG is proposed as a 3D pixel structure for efficient pixel size reduction and fabricated a VTPC-TG by utilizing a similar fabrication scheme found in vertical channel 3D NAND Flash products.

In this study, 5 additional masks and several additional processes steps were added for fabrication of a functional VTPC-TG chip. By confirming the 5M resolution in a real image, using the VTPC-TG pixel, the possibility of future 3D pixels using a thin poly channel has been successfully demonstrated. We expect enhanced image characteristics on future small pixels when we can further optimize the PD layout and process for optimal poly channel resistance.

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