A 75.6μVrms Read Noise CMOS Image Sensor with Pixel Noise Reduction Using Noise-Coupled Amplifier

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Abstract
This paper presents a low-noise CMOS image sensor that reduces the intrinsic pixel noise using noise-coupled amplifier. Experimental results show that the proposed readout scheme achieves the input-referred noise of 75.6μVrms, which is 20% noise reduction compared to conventional SF readout with column amplifier. Without any process modification, the baseline 4T pixel is configured as common-source (CS) amplifier with column load and the source node of the CS amplifier is coupled with an auxiliary common-gate (CG) amplifier. The output difference between CS and CG amplifiers provides a signal gain of 10× achieves the noise reduction of the intrinsic 1/f noise and an improved peak non-linearity of 0.44%. The prototype VGA CMOS image sensor with 4μm pixel pitch has been fabricated in standard 0.11 μm CIS process.

I. Introduction

Due to growing demands for the low noise CMOS image sensors, the noise performance of readout chain has been optimized. The noise bandwidth can be controlled with a column-level amplifier [1], which is widely used for reducing the thermal noise of the pixel and the quantization noise of its following ADC. After mitigating the thermal noise with bandwidth control, the 1/f noise from the pixel source follower (SF) becomes dominant noise source. Correlated multiple sampling (CMS) can reduce the 1/f noise due to the noise-averaging effect, which is proportional to its sampling-rate [2]. Although the 1/f noise power of the pixel SF is reduced up to 44% when the sampling-rate is infinity [4], it was not enough to achieve sub-electron noise performance. Therefore, in-pixel optimization techniques have been investigated [1]-[3]. A buried channel SF with the reduction of sensing capacitor achieved the input-referred noise of 0.74e_rms, but associated process optimization is highly necessary. The PMOS in-pixel open-loop amplifier shows the input-referred noise level of 0.86e-rms [3], but this results in a reduced DR and higher PRNU. The thin-gate PMOS SF with column amplifier achieved the noise level of 0.5e_rms [1], but it reduces its fill factor significantly. To address these issues, a noise-coupled readout scheme has been explored to achieve the reduced 1/f noise and an improved PRNU without sacrificing the fill factor. The paper presents a low noise CMOS image sensor that achieves the input referred noise of 75.6e_rms without any process modification. The baseline 4T pixel is configured with a NMOS common-source (CS) amplifier, and its source node is coupled with a common-gate (CG) amplifier. The output difference between CG and CG amplifiers provides both reduced 1/f noise and an improved PRNU. The paper is organized as follows. Section II reviews the conventional noise reduction techniques. Section III describes the operating principle of the proposed readout scheme. Section IV shows the experimental result. Finally, the conclusion is addressed in Section V.

II. Conventional noise reduction techniques

Fig. 1(a) shows the schematic of a conventional readout chain, exploiting a column-level amplifier. Its noise density can be expressed as

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\bar{v}_{\text{in}}^2 = \bar{v}_{\text{thermal,pixel}}^2 + \bar{v}_{\text{thermal,VGA}}^2 + \bar{v}_{\text{1/f,pixel}}^2
\]

where \(g_{\text{m,CS}} = g_{\text{m,D}}\) and RTS noise of in-pixel SF and the 1/f noise of SF’s current bias. To deal with the 1/f noise of current bias, the current density can be reduced, but this causes settling time penalty, degrading the CDS effect [6]. Fig. 1(b) shows the schematic of in-pixel CS amplifier [3]. The 1/f noise is mitigated by the use of PMOS input.
A column-parallel single-slope (SS) ADC has been used. Fig. 2 shows the block diagram of the column readout circuit. Over an output range of 1V with a signal gain of 10×, the peak non-linearity of 0.44% has been achieved.

III. Proposed readout scheme

Fig. 2 shows the simplified schematic of the proposed readout scheme (10× gain mode is shown).

Fig. 2. Simplified schematic of the proposed readout scheme (10× gain mode is shown)

The prototype chip has been fabricated in a standard 0.11μm CIS process. Fig. 6 shows the chip microphotograph occupying an active area of 6.5×4.5mm². The VGA pixel array with 4μm pixel pitch is implemented.

IV. Experimental result

The prototype chip has been fabricated in a standard 0.11μm CIS process. Fig. 6 shows the chip microphotograph occupying an active area of 6.5×4.5mm². The VGA pixel array with 4μm pixel pitch is implemented.
V. Conclusion

In this paper, a low-noise CMOS image sensor is presented with revised 4T pixel and noise coupled gain amplifier using 0.11 μm CIS process. The proposed amplifier presents 38.3% reduction of 1/f noise power compared to SF readout without any process modification. Total input referred noise is reduced to 75.6 μVrms, and peak non-linearity of 0.44% is also achieved without sacrificing fill factor.

References


