A 75.6μV_{rms} Read Noise CMOS Image Sensor with Pixel Noise Reduction Using Noise-Coupled Amplifier

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Abstract

This paper presents a low-noise CMOS image sensor that reduces the intrinsic pixel noise using noise-coupled amplifier. Experimental results show that the proposed readout scheme achieves the input-referred noise of 75.6μV_{rms}, which is 20% noise reduction compared to conventional SF readout with column amplifier. Without any process modification, the baseline 4T pixel is configured as common-source (CS) amplifier with column load and the source node of the CS amplifier is coupled with an auxiliary common-gate (CG) amplifier. The output difference between CS and CG amplifiers providing a signal gain of 10× achieves the noise reduction of the intrinsic 1/*f* noise and an improved peak non-linearity of 0.44%. The prototype VGA CMOS image sensor with 4μm pixel pitch has been fabricated in standard 0.11 μm CIS process.

I. Introduction

Due to growing demands for the low noise CMOS image sensors, the noise performance of readout chain has been optimized. The noise bandwidth can be controlled with a column-level amplifier [1], which is widely used for reducing the thermal noise of the pixel and the quantization noise of its following ADC. After mitigating the thermal noise with bandwidth control, the 1/*f* noise from the pixel source follower (SF) becomes dominant noise source. Correlated multiple sampling (CMS) can reduce the 1/*f* noise due to the noise-averaging effect, which is proportional to its sampling-rate [2]. Although the 1/*f* noise power of the pixel SF is reduced up to 44% when the sampling-rate is infinity [4], it was not enough to achieve sub-electron noise performance. Therefore, in-pixel optimization techniques have been investigated [1]-[3]. A buried channel SF with the reduction of sensing capacitor achieved the input-referred noise of 0.74e^-_{rms}, but associated process optimization is highly necessary. The PMOS in-pixel open-loop amplifier shows the input-referred noise level of 0.86e-rms [3], but this results in a reduced DR and higher PRNU. The thin-gate PMOS SF with column amplifier achieved the noise level of 0.5e^-_{rms} [1], but it reduces its fill factor significantly. To address these issues, a noise-coupled readout scheme has been explored to achieve the reduced 1/*f* noise and an improved PRNU without sacrificing the fill factor. The paper presents a low noise CMOS image sensor that achieves the input referred noise of 75.6μV_{rms} without any process modification. The baseline 4T pixel is configured with a NMOS common-source (CS) amplifier, and its source node is coupled with a common-gate (CG) amplifier. The output difference between CG and CG amplifiers provides both reduced 1/*f* noise and an improved PRNU. The paper is organized as follows. Section II reviews the conventional noise reduction techniques. Section III describes the operating principle of the proposed readout scheme. Section IV shows the experimental result. Finally, the conclusion is addressed in Section V.

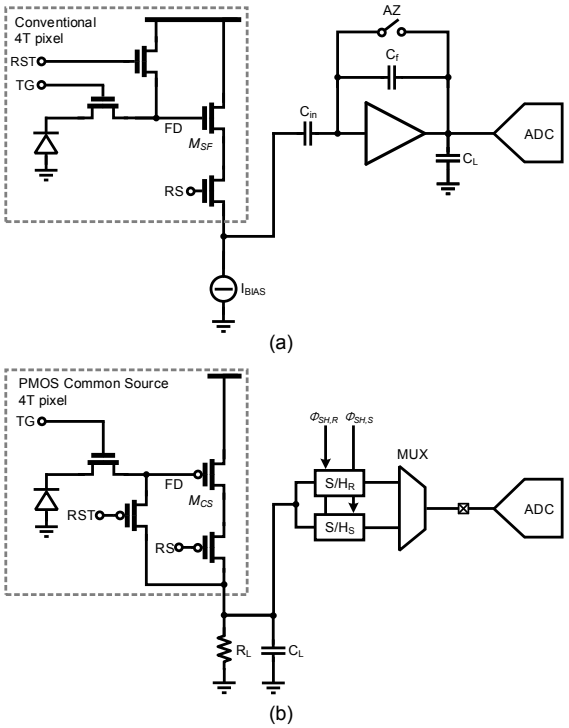

Fig. 1. (a) schematic of the conventional readout chain [1] and (b) schematic of in-pixel common source amplifier [3]

II. Conventional noise reduction techniques

Fig. 1(a) shows the schematic of a conventional readout chain, exploiting a column-level amplifier. Its noise density can be expressed as

$$\overline{V_n^2} = \overline{V_{n,thermal,pixel}^2} + \overline{V_{n,thermal,VGA}^2} + \overline{V_{n,1/f,pixel}^2}$$
$$= \overline{V_{n,thermal,SF}^2}\left(1+\frac{gm_{CS}}{gm_{SF}}\right) + \overline{V_{n,thermal,VGA}^2} + \overline{V_{n,1/f,pixel}^2}$$

where gm_{CS} = gm of current bias. With the help of column-level amplifier, the thermal noise can be mitigated with its bandwidth control. After CDS, the noise level is determined by the 1/*f* and RTS noise of in-pixel SF and the 1/*f* noise of SF's current bias. To deal with the 1/*f* noise of current bias, the current density can be reduced, but this causes settling time penalty, degrading the CDS effect [6]. Fig. 1(b) shows the schematic of in-pixel CS amplifier [3]. The 1/*f* noise is mitigated by the use of PMOS input

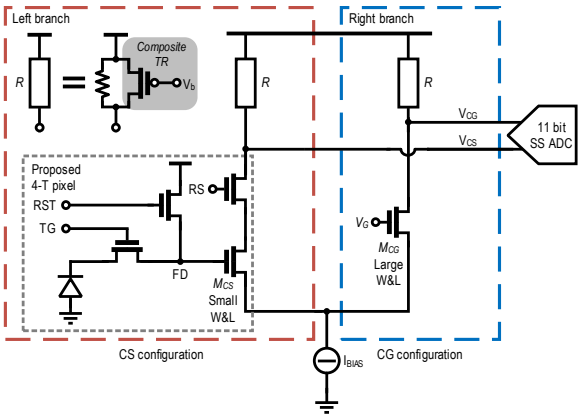

Fig. 2. Simplified schematic of the proposed readout scheme (10× gain mode is shown)

transistor, but its fill factor, especially for small pixel pitch (<5μm), can be drastically reduced when compared to the NMOS SF configuration. For the noise of current source, its noise contribution is reduced with the gain of CS amplifier. However, the PRNU is highly impaired up to a few percent due to the open-loop configuration of CS amplifier. Since the voltage gain with respect to input range is not well defined, it suffers gain variations as well.

III. Proposed readout scheme

Fig. 2 shows the simplified schematic of the proposed readout scheme. The left branch features CS amplifier with a NMOS input M_{CS} and a column load resistor R, offering moderate voltage gain of 5×. At the same time, the source voltage of M_{CS} is coupled with an auxiliary CG amplifier implemented in the column-level, and it provides the same voltage gain as CS amplifier with reverse polarity. The output difference between CS and CG amplifiers provides a voltage gain of 10×. Assuming the signal range of each amplifier is the same, the output signal range is doubled by subtracting one output from the other.

Here, it should be noted that the size of input transistor M_{CG} of CG amplifier is set to be much larger than the M_{CS} to minimize excess 1/f and thermal noise. When M_{CG} = 200M_{CS}, for instance, the 1/f noise power of 97% is caused by the M_{CS}. Since the source voltage of the CS amplifier is formed by the bias voltage V_G of the CG amplifier, the 1/f noise of M_{CS} can be suppressed with respect to V_G as shown in Fig. 3. Compared to SF configuration, 1/f noise reduction of 38.3% can be achieved in this work. Although the excess noise of current bias is quite severe in SF readout, it can be mitigated with the differential output of the composite amplifiers.

Fig. 4 shows the peak non-linearity comparison. The proposed composite amplifier provides 3.8× improvement on the peak non-linearity compared to conventional open-loop CS amplifier. This can be further improved with a composite load, which is implemented with a PMOS transistor parallel with a load resistor (1MΩ) in Fig. 2. As a result, the peak non-linearity of 0.44% has been achieved over an output range of 1V with a signal gain of 10×. Fig. 5 shows the block diagram of the column readout circuit. A column-parallel single-slope (SS) ADC has been used

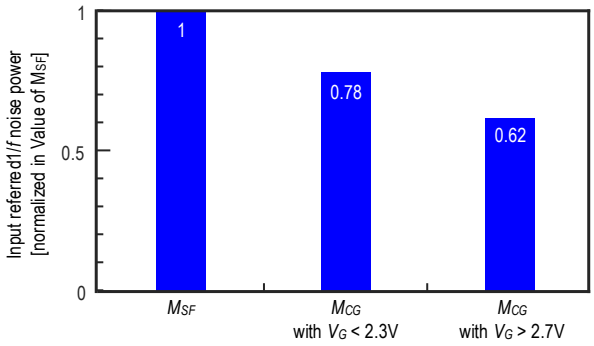

Fig. 3. Input referred 1/f noise power normalized in value of M_{SF}

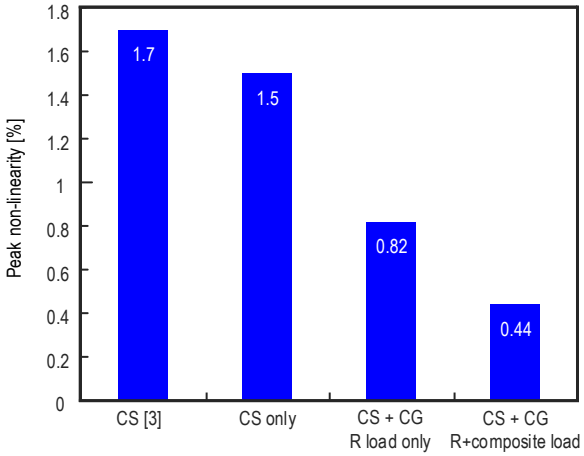

Fig. 4. Peak non-linearity comparison

for A/D conversion at the output of the proposed pixel. The pixel output can be reconfigured with SF mode by adding a switch around the load resistor, and this provides dual gain configurations, i.e. 1 and 10×. The CG output is sampled at one capacitor when the auto-zeroing (AZ) phase. At the same time, the reference signal is sampled at the other capacitor. During comparison phase, the CS output is sampled at the AZ capacitor, so the subtracted value V_{CG} - V_{CS} is sampled and then converted via 11bit SS ADC.

IV. Experimental result

The prototype chip has been fabricated in a standard 0.11μm CIS process. Fig. 6 shows the chip microphotograph occupying an active area of 6.5×4.5mm^2. The VGA pixel array with 4μm pixel pitch is implemented. Fig. 7 shows the layout comparison between baseline 4T pixel and the proposed pixel. A vertical line is used to connect the drain output of the row selection transistor with load resistor in the proposed pixel, resulting in a small reduction of the fill factor about 3.4%. The proposed pixel shows fill factor of 65%. Fig. 8 shows noise comparison with conventional techniques employing the same equivalent noise bandwidth and excess noise factor from CDS. The proposed readout scheme achieves the input-referred noise of 75.6μV_{rms}, which is 67% lower than that of SF readout. This work also achieves about 20% reduction compared to the SF readout with column-level amplifier, assuming the thermal noise of the amplifier is

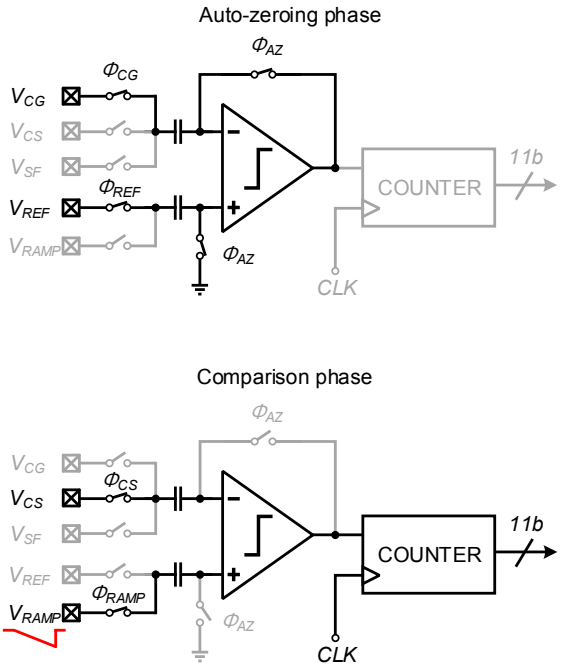

Fig. 5. Block diagram of the column readout circuit (10× gain mode is shown)

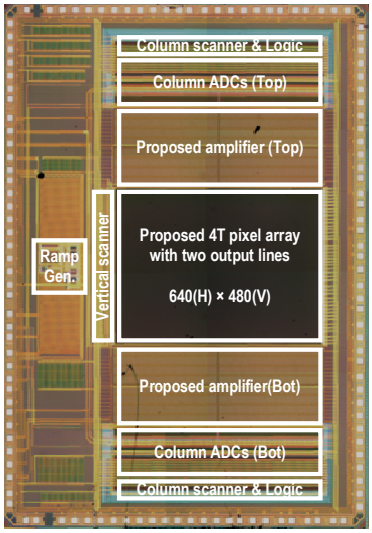

Fig. 6. Die photo of the prototype imager

equivalent to the pixel. The noise breakdown is also presented. The noise contribution of the 1/*f* noise is 62%. For the thermal noise, the noise from the M_{CS} is about 20%. The noise contributions of M_{CG} and load resistors are only 7% and 8%, respectively.

V. Conclusion

In this paper, a low-noise CMOS image sensor is presented with revised 4T pixel and noise coupled gain amplifier using 0.11 μm CIS process. The proposed amplifier presents 38.3% reduction of 1/*f* noise power compared to SF readout without any process modification. Total input referred noise is reduced to 75.6μV_{rms}, and peak non-linearity of 0.44% is also achieved without sacrificing fill factor.

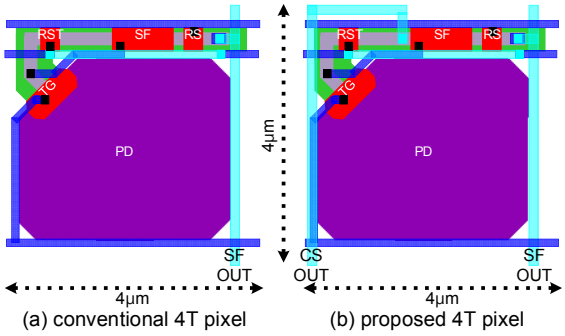

Fig. 7. The layout of the conventional 4T pixel (a) and the proposed 4T pixel (b)

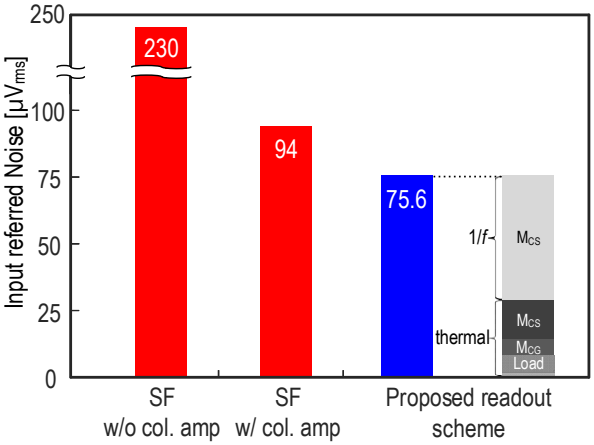

Fig. 8. Noise comparison with conventional technique and proposed readout scheme

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