A CMOS Front-end for GaN-based UV Imaging

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I. Introduction

The ultraviolet (UV) region in the electromagnetic spectrum is important in order to study about the stars, cosmos, galaxies along with the thin atmospheres in space. UV imaging spectrometry provides essential information of specific elements and compounds through their emission and absorption lines in the UV spectrum. Thus, the growing role of UV imaging in a variety of applications requires high-performance photodetectors. Further, it is necessary to provide single-photon counting capability for detection of distant objects along with visible blindness. Gallium nitride (GaN) and its alloys are used in solar blind avalanche photodiodes (APDs) due to their band gap nature (3.4 eV). In addition to providing visible blindness, the GaN APDs also have high gain and quantum efficiency in the UV spectral region. The readout in this work is designed for the APDs which have been developed at NASA- JPL. The APDs show about 60% external quantum efficiency at 360 nm. The photodiode is a p-i-n structure based on a n-type sapphire substrate, achieving a gain as high as 2.5×10^5 in the UV wavelengths [1][2]. Under a reverse bias, typically as high as 60-80 V, the GaN APDs generate an avalanche current on the order of hundreds of picoamperes as shown in Fig. 1. Beyond

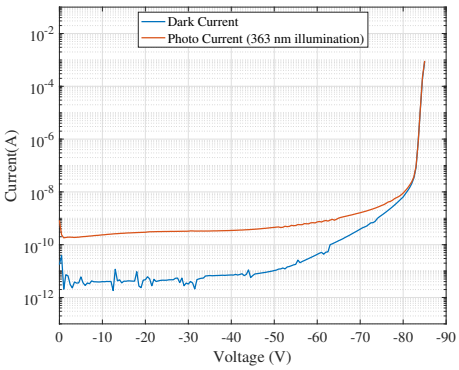

Fig. 1: Typical I-V characteristics for a GaN p-i-n APD (*Redrawn from [1],[2]*)

80 V, one can observe the abrupt increase in the photodiode current suggesting that GaN devices can be operated in Geiger mode. In this paper, a hybrid sensor with a CMOS front-end readout is demonstrated as a proof-of-concept with GaN APDs operating in proportional mode.

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II. CMOS readout design

A photodiode circuit model was derived from the GaN APD characteristics, comprising the APD capacitance and the equivalent APD current. A transimpedance amplifier was the first option for the readout, which would provide sufficient gain to amplify the low magnitude input currents from the APD. The major effort of this work was to develop a readout to better understand the timing performance of the GaN APDs, which was known with lesser certainty. With only the I-V characteristics established, a simple readout was preferred to track signals easily whenever necessary during measurement and testing. This approach helped us understand the readout requirements of the GaN devices and derive specifications for superior amplifier designs for the next version of the readout. Thus, in this work, a conventional capacitive transimpedance amplifier (CTIA) with a parallel reset, as shown in Fig. 2 was designed. The basic idea of the CTIA is to integrate the

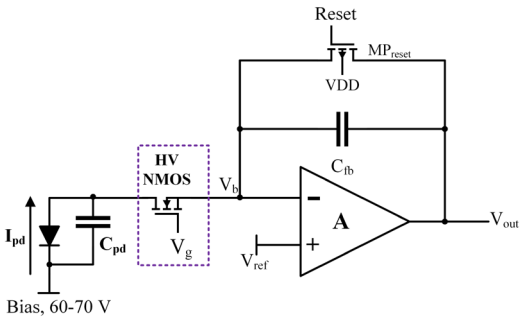

Fig. 2: Capacitive transimpedance amplifier (CTIA)

incoming photodiode current (I_{pd}) on the feedback capacitor (C_{fb}) and generate an equivalent observable output voltage such that the low-frequency DC gain would be set by the ratio of photodiode capacitance (C_{pd}) and the feedback capacitance (C_{fb}).

$$I_{pd}(s) + \frac{V_{out}(s)}{A}(sC_{fb} + sC_{pd}) = V_{out}(s)C_{fb} \qquad (1)$$

where A is open loop gain of the CTIA. When A $>>\frac{C_{pd}}{C_{fb}}$,

$$V_{out} = \frac{1}{C_{fb}} \int I_{pd} dt \qquad (2)$$

The operation of the CTIA begins with the reset of the feedback capacitor by the transistor MP_{reset} before every integration. As soon as the reset switch is released and the photodiode current starts to flow in, the voltage at the input node starts to rise, causing the output voltage to fall. The small rise at the input node is due to the finite gain (A) of the CTIA. The negative feedback of the amplifier however,

maintains the input node at virtual ground and the output of the amplifier starts to drop from the initial value set by the reset transistor. The choice of the amplifier topology was primarily derived from the characteristics of the GaN devices. The diode capacitance of approximately 1 pF provided freedom to choose C_{fb} based on the desired gain. In this design, variable gain is provided by 3 switches and 4 feedback capacitors. The operating bandwidth of the CTIA is limited to 1 MHz. A common-source stage is used as the core cell of the CTIA. The transistor-level schematic of a CTIA unit cell is shown in Fig. 3. The variable gain is provided by 4 effective feedback

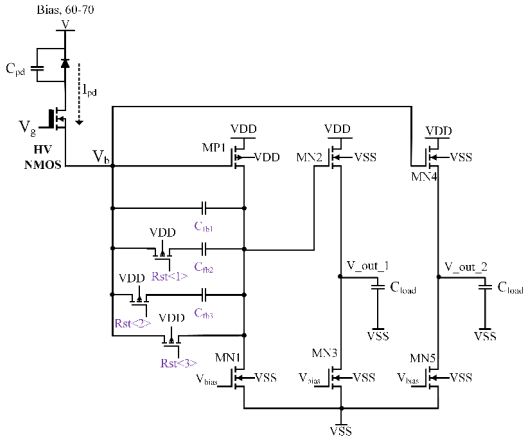

Fig. 3: CTIA- Transistor-level schematic

capacitances, obtained such that C1= C_{fb1}, C2= C_{fb1}+ C_{fb2}, C3= C_{fb1}+ C_{fb3}, C4= C_{fb1}+ C_{fb2}+ C_{fb3}. The relative values were chosen such that C2-C1 =100 fF, C3-C2 =200 fF, C4-C3 =100fF. Furthermore, since the GaN APD is a p-on-n type structure (with a n-type sapphire substrate), a PMOS input is used to integrate a positive current which flows into the CTIA [1]. Additionally, an NMOS source follower (MN2-MN3) is utilized as an output buffer ahead of the common-source stage to prevent any degradation at the output voltage level, shown in the schematic of Fig. 3. There is another source follower (MN4-MN5) provided to track the input node V_b; for example, to monitor any sudden current surge at the input. There is an advantage to tracking this node, the reason for which will be revisited in the next section. A PMOS transistor with Rst<3> pin to control its gate is used to reset the feedback capacitor and bias the CTIA transistors in the appropriate operating points. The bias voltage (V_{bias}) for the load is generated from a simple current mirror. The CTIA was designed in 0.35 µm HV CMOS technology. Performance characteristics of the PMOS and NMOS transistors in this technology were derived by conducting simulations on Cadence software. Transistor parameters like the intrinsic gain of the transistor g_m/g_{ds}, the transconductance-to-drain current ratio g_m/I_d, the overdrive voltage V_{dsat} and their relationships were obtained to size the transistors with appropriate width (W) and length (L).

III. Design Challenge

Apart from the integration of the input current, the readout also needs to accommodate very high reverse bias voltages applied to the GaN APD and prevent any damage to the low voltage CMOS circuitry. Additionally, under such a bias, due to the presence of high electric fields in the device, hot carriers are produced whenever a photon is detected. However, carrier multiplication must be eventually quenched to avoid damage to the APD. For the same reason, a high voltage (HV) NMOS transistor was used as a clamp in order to circumvent both the challenges (outlined in a purple box in Fig. 2, also denoted as HV NMOS in Fig. 3). Initially, the bias voltage at the gate of the HV NMOS is set such that it is in its ohmic region of operation. Under this condition, the detector sees full bias since there is little voltage drop across the HV NMOS. As the CTIA saturates upon the completion of integration, the input voltage, V_b begins to rise as the incoming current can no longer integrate on the feedback capacitance. The rising input voltage can exceed damaging levels if this condition is left unattended. However, in this design, the increasing voltage level at node V_b, in turn reduces the gate-to-source voltage of the HV NMOS and eventually shutting off the transistor. One can observe the rising input voltage in Fig. 7, verified during measurement. When this happens, the incoming photodiode current will cease to flow through the HV NMOS and charge the photodiode capacitance C_{pd}. This action results in the reduction of the bias across the photodiode, especially useful in case of sudden current surge due to avalanche. This is another reason to provide the source follower to track the input node. In conclusion, whenever there is an avalanche breakdown, the following will take place in the readout circuit- integration of the photodiode current, saturation of the CTIA, shutting-off of the HV NMOS, reduction in the diode bias and eventually, quenching. The high voltage bias applied on the APD will directly appear at the drain of the HV NMOS. However, the high voltage CMOS technology used in this circuit permits us to exploit the HV NMOS for this purpose. Finally, after the HV NMOS shuts off, the CTIA should be reset again which sets the appropriate bias conditions for all the transistors in the CTIA to begin another integration cycle.

IV. Measurement Results

Fig. 4 shows the photomicrograph of the chip. As can be seen, the fabricated chip contains a linear array of eight CTIA unit cells. The chip was laid out so that the inputs connected to the high voltage side on the APD are isolated from the low voltage CMOS outputs. In the recent test setup,

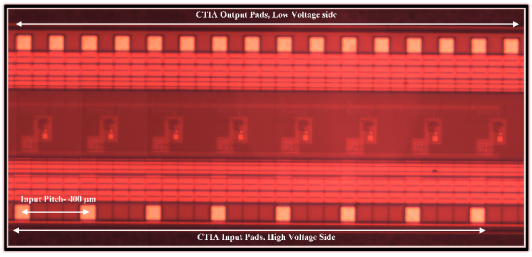

Fig. 4: Chip photomicrograph

the CTIA was independently characterized for gain using a number of transient measurements with a constant current source. Additionally, the readout was also bonded with several

GaN APDs and the I-V characteristics of the APDs were derived from the measurement.

A. CTIA characterization results

A constant current was generated using a voltage source connected to a 20 MΩ resistor. The input voltage source was swept from 2.8-20 V, generating equivalent input currents ranging from 20 nA - 0.8 µA. The CTIA output voltage was measured on an oscilloscope for the entire sweep range. The slope (dV/dt) was then extracted from the oscilloscope waveform data by differentiating the output voltage waveform with respect to time, shown in Fig 5. Differentiating Eq. (2)

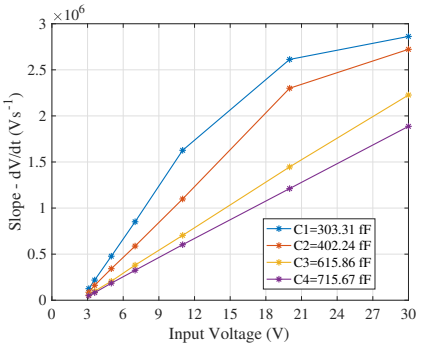

Fig. 5: Slope versus input voltage

with respect to time gives the slope (dV/dt) which is directly proportional to the photodiode current I_{pd} and inversely, to the feedback capacitance C_{fb}. As can be seen in Fig. 5, the obtained slope increases with increasing input currents (as input voltage increases) and decreases for increasing C_{fb} (C1-C4). It can also be observed that for lower feedback capacitances (C1 and C2), the output from the source follower saturates for higher input currents and for C3 and C4, the slope is linear for the entire sweep range. The CTIA was measured for even higher input currents (from 1 µA- 10 µA) to determine the limitation of the readout. Higher currents were generated by connecting the input voltage source to a 4 MΩ resistor. It was observed that for input currents approximately above 1.5 µA, the slopes obtained for all the feedback capacitances saturated to the same value, ≈ 2.8 V/µs. This slope also provides an estimate on the slew rate of the CTIA which is limited mainly by the speed of the output source follower which cannot draw input currents beyond 1.5 µA.

B. Measurement of effective feedback capacitance

The extracted output slope values were utilized along with corresponding input currents to measure the actual feedback capacitances based on Eq. (2). As can be seen from the bar chart on Fig. 6, the relative differences between the measured feedback capacitances (C2-C1, C3-C2, C4-C3) align well with the design as described in Section II. In principle, the extracted capacitances for changing input conditions should result in the same value. One can already observe this condition in the figure below where the measured values showed minimal variation with a standard deviation of about 10.6 fF for the smallest feedback capacitance (≈ 300 fF). The capacitances obtained in this measurement were further used in order to

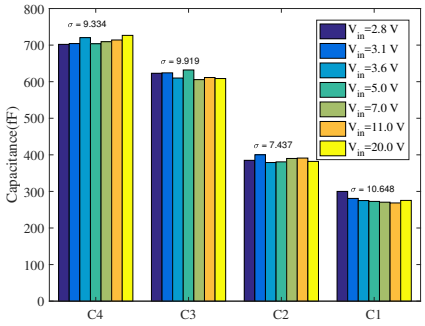

Fig. 6: Variation in measured feedback capacitances as a function of input voltage V_{in}

derive the I-V characteristics of the GaN detectors in Section IV-D.

C. Voltage limiter functionality

The voltage limiter in the readout was also tested for increasing input currents and verified for its functionality as explained in Section III. In Fig. 7, the input node (V_b) waveform from the oscilloscope is plotted. The HV NMOS is biased with 4.5 V, making V_{gs} approximately 1 V above the threshold voltage (V_{gs}-V_{th} ≈ 1 V). As can be seen, there is a rise in the voltage after the CTIA saturates. The rise continues until the point where V_{gs}<V_{th} and the node V_b saturates and HV NMOS stops conducting; in this case, it occurs at ≈ 3.8 V.

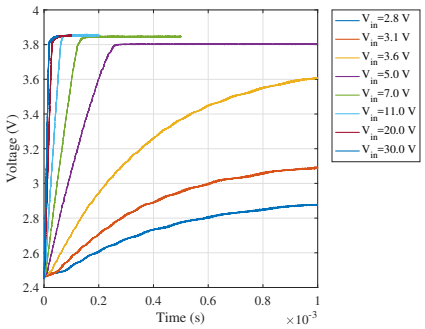

Fig. 7: Rise in CTIA input node voltage after CTIA saturates (measured with C_{fb} ≈ 715 fF)

D. Characterization of GaN+CMOS combination

In addition to the CTIA characterization, several GaN devices were bonded to the readout chip and transient measurements were performed on the CTIA with the GaN APD at its input. I-V characteristics were extracted for reverse bias voltages of up to 100 V. The obtained results showed the expected exponential increase in the current as the device entered into the breakdown region beyond 80 V. This can be seen below in Fig. 8.

Different colors in Fig. 8 (and also in Fig. 10) indicate results from different data sets with the same input condition. This was done in order to confirm reproducibility of the measurement. Additionally, another GaN detector was illuminated using an available UV LED and the I-V characteristics

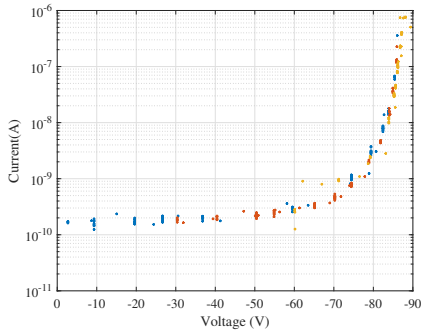

Fig. 8: Extracted I-V curve from the CTIA

were obtained under dark and illuminated environments. The

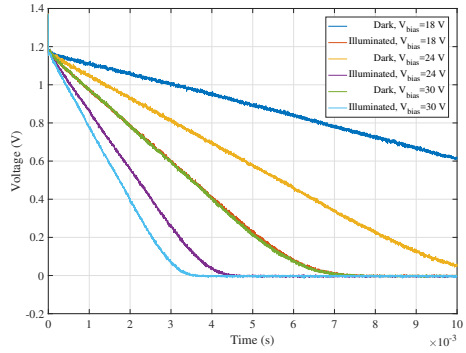

Fig. 9: CTIA output voltage waveform
(*At node V_out_1 in Fig. 3)*

measurement results for both the conditions are clearly distinguishable. The CTIA output signal, directly measured on the oscilloscope is plotted at various LED bias voltages in Fig. 9 above. At a bias voltage of 18 V, the ratio of the slope under illuminated (shown in orange colour in Fig. 9) and dark (shown as blue) is about 2. This ratio is found to be uniform over the 3 bias voltages plotted in the figure above. From the CTIA

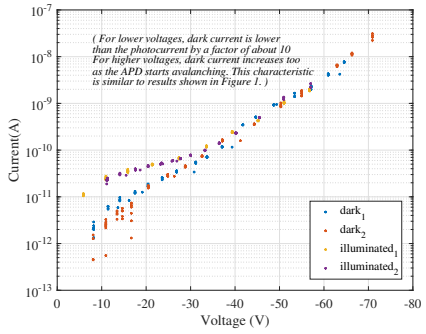

Fig. 10: Measurement under UV illumination

output waveforms, the slope was extracted and the I-V curve for the GaN device was obtained and plotted against increasing reverse bias voltages, shown above in Fig. 10. The optical gain is also estimated from Fig. 10 using a method described in [2] and the results are plotted in Fig. 11. At lower bias voltages, the dark current extracted was measured to be almost 1/10th of the photocurrent. At higher bias voltages, the optical gain of the APD increased to about 10^3 at 70 V.

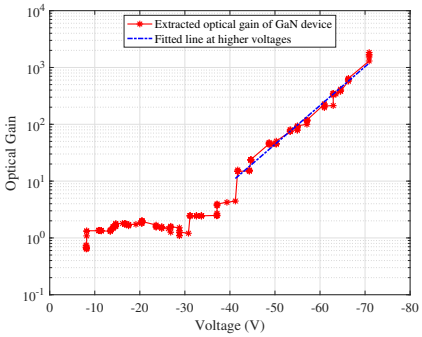

Fig. 11: Optical gain estimated from Fig. 10

V. Conclusion

The obtained measurement results provide a guideline towards more precise specification for noise, bandwidth and power dissipation for future versions of the readout. Some of the possible recommendations would be as follows. Firstly, a programmable reset can be implemented since the required integration time is now known with more certainty from the measurement results. It was observed from the results shown in Section IV-A that the output source follower cannot draw input currents beyond 1.5 µA. In order to test the GaN sensor beyond breakdown, it will be interesting to provide a more powerful CTIA without saturating the output for higher input currents. A differential topology for the amplifier can be explored instead of the current single-stage common-source cell with a focus on minimizing the input-referred noise. Focusing on space applications, one of the future tasks in terms of measurements is to test the GaN+CMOS combination under radiation and study the behaviour under dark environment. This work is a proof-of-concept to envision the integration of GaN APDs with CMOS readouts. The current design is not optimized and the obtained results demonstrate the feasibility of our approach, whereas higher optical gains will be possible in future. With GaN photodiodes operating in Geiger mode, single-photon counting circuits can also be explored in a variety of imaging applications.

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